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MECL Data

ON Semiconductor

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Sales Representative.

This book presents technical data for a broad line of MECL integrated circuits. Complete specifications for the individual circuits are provided in the form of data sheets. In addition, selector guides are included to simplify the task of choosing the best combination of circuits for optimum system architecture. For the most up–to–date information, please visit our website at:
http://onsemi.com

Table of Contents

Deleted Devices

The following list of devices have been deleted since the last publication of this book.

DATA SHEETS DELETED

MC10137	MC1648	MC1650	MC1651
MC1658	MC1660	MC1662	MC1670
MC1692			

End-of-Life (EOL) Devices

The following list of devices have been placed on EOL and are not recommended for new designs, since the last publication of this book.

END OF LIFE DEVICES

MC10H145	MC10H660

Numeric Data Sheet Listing

MECL 10H Data Sheets

MECL 10H Data Sheets

MECL 10K Data Sheets

MECL 10K Data Sheets

MECL 10K Data Sheets

Carrier Band Modem Data Sheet

CHAPTER 1
General Information

High speed logic is used whenever improved system performance would increase a product's market value. For a given system design, high–speed logic is the most direct way to improve system performance and Emitter–Coupled Logic (ECL) is one of today's fastest forms of digital logic. Emitter– coupled logic offers both the logic speed and logic features to meet the market demands for higher performance systems.

MECL PRODUCTS

Motorola, now ON Semiconductor, introduced the original monolithic emitter–coupled logic family with MECL I (1962) and followed this with MECL II (1966). These two families are now obsolete and have given way to the MECL III (MC1600 series), MECL 10K, PLL (MC12000 series) and the new MECL 10H families.

Chronologically the third family introduced, MECL III (1968) is a higher power, higher speed logic. Typical 1 ns edge speeds and propagation delays along with greater than 500 MHz flip–flop toggle rates, make MECL III useful for high–speed test and communications equipment. Also, this family is used in the high–speed sections and critical timing delays of larger systems. For more general purpose applications, however, trends in large high–speed systems showed the need for an easy–to–use logic family with propagation delays on the order of 2 ns. To match this requirement, the MECL 10,000 Series was introduced in 1971.

An important feature of MECL 10K is its compatibility with MECL III to facilitate using both families in the same system. A second important feature is its significant power economy – MECL 10K gates use less than one–half the power of MECL III.

ON Semiconductor introduced the MECL 10H product family in 1981. This latest MECL family features 100% improvements in propagation delay and clock speeds while maintaining power supply currents equal to MECL 10K. MECL 10H is voltage compensated allowing guaranteed dc and switching parameters over a ±5% power supply range. Noise margins have been improved by 75% over the MECL 10K series.

Compatibility with MECL 10K and MECL III is a key element in allowing users to enhance existing systems by increasing the speed in critical timing areas. Also, many MECL 10H devices are pin out/functional duplications of the MECL 10K series devices. The emphasis of this family will be placed on more powerful logic functions having more complexity and greater performance. With 1.0 ns propagation delays and 25 mW per gate, MECL 10H is one of the best speed–power families of any ECL logic family available today.

MECL at +5V (PECL – Positive ECL)

Any single supply ECL device is also a PECL device, making the PECL portfolio as large as the existing ECL one. (Note: The dual supply translator devices cannot operate at +5V and ground and cannot be considered PECL devices.)

ECL devices in the PECL mode, must have the input/output DC specifications adjusted for proper operation. ECL levels (DC) are referenced from the V_{CC} level. To calculate the PECL DC specifications, ECL levels are added to the new V_{CC}.

EXAMPLE:

PECL V_{OH} = New V_{CC} + ECL V_{OH}, 5.0V + (–0.81V) = 4.190V and is the max V_{OH} level at 25°C for a PECL device. Follow the same procedure to calculate all input/output DC specifications for a device used in a PECL mode. The V_{TT} supply used to sink the parallel termination currents is also referenced from the V_{CC} supply and is V_{CC}–2.0V. The PECL V_{TT} supply = +5V – 2V = +3.0V and should track the V_{CC} supply one–to–one for specified operation.

Since ECL is referenced from the V_{CC} rail, any noise on the V_{CC} supply will be reflected on the output waveshape at a one–to–one ratio. Therefore, noise should be kept as low as possible for best operation. Devices in a PECL system cannot have V_{CC} vary more than 5% to assure proper AC operation. See ON Semiconductor Application Note AN1406/D "*Designing With PECL (ECL at +5.0V)*" for more details.

AC performance in the PECL mode is equal to the AC performance in the ECL mode, if the pitfalls set forth in Application Note (AN1406/D) are avoided.

MECL FAMILY COMPARISONS

Feature	MECL 10H	MECL 10K	
		10,100 Series	10,200 Series
1. Gate Propagation Delay	1.0 ns	2.0 ns	1.5 ns
2. Output Edge Speed*	1.0 ns	3.5 ns	2.5 ns
3. Flip–Flop Toggle Speed	250 MHz min	125 MHz min	200 MHz min
4. Gate Power	25 mW	25 mW	25 mW
5. Speed Power Product	25 pJ	50 pJ	37 pJ

*Output edge speed: MECL 10K/10H measured 20% to 80%.

Figure 1 – GENERAL CHARACTERISTICS

Ambient Temperature Range	MECL 10H	MECL 10K
0° to 75°C	MC10H100 Series	
–30°C to +85°C		MC10100 Series MC10200 Series

Figure 2 – OPERATING TEMPERATURE RANGE

MECL IN PERSPECTIVE

In evaluating any logic line, speed and power requirements are the obvious primary considerations. Figure 1 and Figure 2 provide the basic parameters of the MECL 10H, MECL 10K, and MECL III families. But these provide only the start of any comparative analysis, as there are a number of other important features that make MECL highly desirable for system implementation. Among these:

Complementary Outputs cause a function and its complement to appear simultaneously at the device outputs, without the use of external inverters. It reduces package count by eliminating the need for associated invert functions and, at the same time, cuts system power requirements and reduces timing differential problems arising from the time delays introduced by inverters.

High Input Impedance and Low Output Impedance permit large fan out and versatile drive characteristics.

Insignificant Power Supply Noise Generation, due to differential amplifier design which eliminates current spikes even during signal transition period.

Nearly Constant Power Supply Current Drain simplifies power–supply design and reduces costs.

Low Cross–Talk due to low–current switching in signal path and small (typically 850 mV) voltage swing, and to relatively long rise and fall times.

Wide Variety of Functions, including complex functions facilitated by low power dissipation (particularly in MECL 10H and MECL 10K series). A basic MECL 10K gate consumes less than 8 mW in on–chip power in some complex functions.

Wide Performance Flexibility due to differential amplifier design which permits MECL circuits to be used as linear as well as digital circuits.

Transmission Line Drive Capability is afforded by the open emitter outputs of MECL devices. No “Line Drivers” are listed in MECL families, because *every* device is a line driver.

Wire–ORing reduces the number of logic devices required in a design by producing additional OR gate functions with only an interconnection.

Twisted Pair Drive Capability permits MECL circuits to drive twisted–pair transmission lines as long as 1000 feet.

Wire–Wrap Capability is possible with the MECL 10K family because of the slow rise and fall time characteristic of the circuits.

Open Emitter–Follower Outputs are used for MECL outputs to simplify signal line drive. The outputs match any line impedance and the absence of internal pulldown resistors saves power.

Input Pulldown Resistors of approximately 50 kΩ permit unused inputs to remain unconnected for easier circuit board layout.

MECL APPLICATIONS

ON Semiconductor’s MECL product lines are designed for a wide range of systems needs. Within the computer market, MECL 10K is used in systems ranging from special purpose peripheral controllers to large mainframe computers. Big growth areas in this market include disk and communication channel controllers for larger systems and high performance minicomputers.

The industrial market primarily uses MECL for high performance test systems such as IC or PC board testers. However, the high bandwidths of MECL 10H and MECL 10K are required for many frequency synthesizer systems using high speed phase lock loop networks. MECL has

continued to grow in the industrial market through complex medical electronic products and high performance process control systems.

BASIC CONSIDERATIONS FOR HIGH–SPEED LOGIC DESIGN

High–speed operation involves only four considerations that differ significantly from operation at low and medium speeds:

1. Time delays through interconnect wiring, which may have been ignored in medium–speed systems, become highly important at state–of–the–art speeds.
2. The possibility of distorted waveforms due to reflections on signal lines increases with edge speed.
3. The possibility of “crosstalk” between adjacent signal leads is proportionately increased in high–speed systems.
4. Electrical noise generation and pick–up are more detrimental at higher speeds.

In general, these four characteristics are speed– and frequency–dependent, and are virtually independent of the type of logic employed. The merit of a particular logic family is measured by how well it compensates for these deleterious effects in system applications.

The interconnect–wiring time delays can be reduced only by reducing the length of the interconnecting lines. At logic speeds of two nanoseconds, an equivalent “gate delay” is introduced by every foot of interconnecting wiring. Obviously, for functions interconnected within a single monolithic chip, the time delays of signals travelling from one function to another are insignificant. But for a great many externally interconnected parts, this can soon add up to an appreciable delay time. Hence, the greater the number of functions per chip, the higher the system speed. *MECL circuits, particularly those of the MECL 10K and MECL 10H Series are designed with a propensity toward complex functions to enhance overall system speed.*

Waveform distortion due to line reflections also becomes troublesome principally at state–of–the–art speeds. At slow and medium speeds, reflections on interconnecting lines are not usually a serious problem. At higher speeds, however, line lengths can approach the wavelength of the signal and improperly terminated lines can result in reflections that will cause false triggering (see Figure 3 and Figure 4). The solution, as in RF technology, is to employ “transmission–line” practices and properly terminate each signal line with its characteristic impedance at the end of its run. *The low–impedance, emitter–follower outputs of MECL circuits facilitate transmission–line practices without upsetting the voltage levels of the system.*

The increased affinity for crosstalk in high–speed circuits is the result of very steep leading and trailing edges (fast rise and fall times) of the high–speed signal. These steep wavefronts are rich in harmonics that couple readily to adjacent circuits. *In the design of MECL 10K and MECL 10H, the rise and fall times have been deliberately slowed. This reduces the affinity for crosstalk without compromising other important performance parameters.*

From the above, it is evident that the MECL logic line is not simply capable of operating at high speed, but has been specifically designed to reduce the problems that are normally associated with high–speed operation.

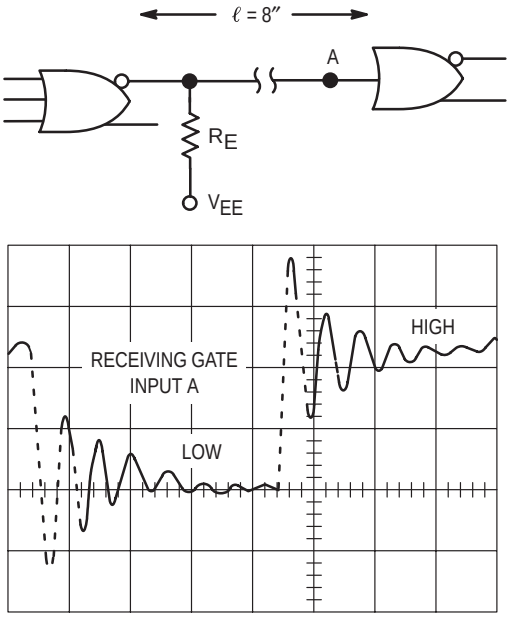


Figure 3 – UNTERMINATED TRANSMISSION LINE (No Ground Plane Used)

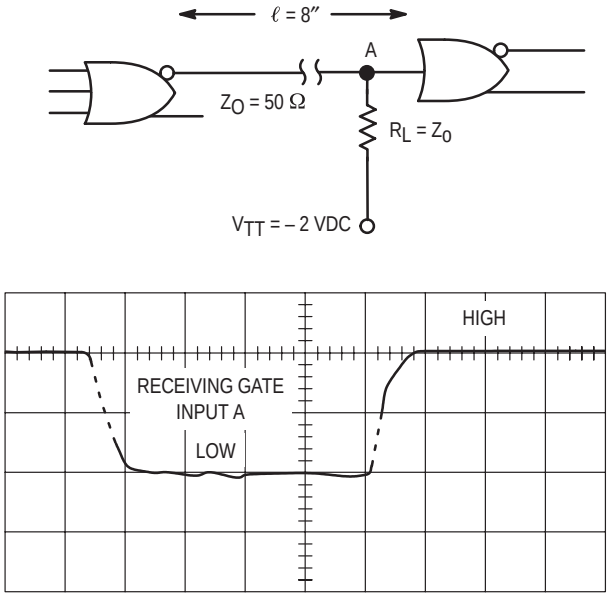


Figure 4 – PROPERLY TERMINATED TRANSMISSION LINE (Ground Plane Added)

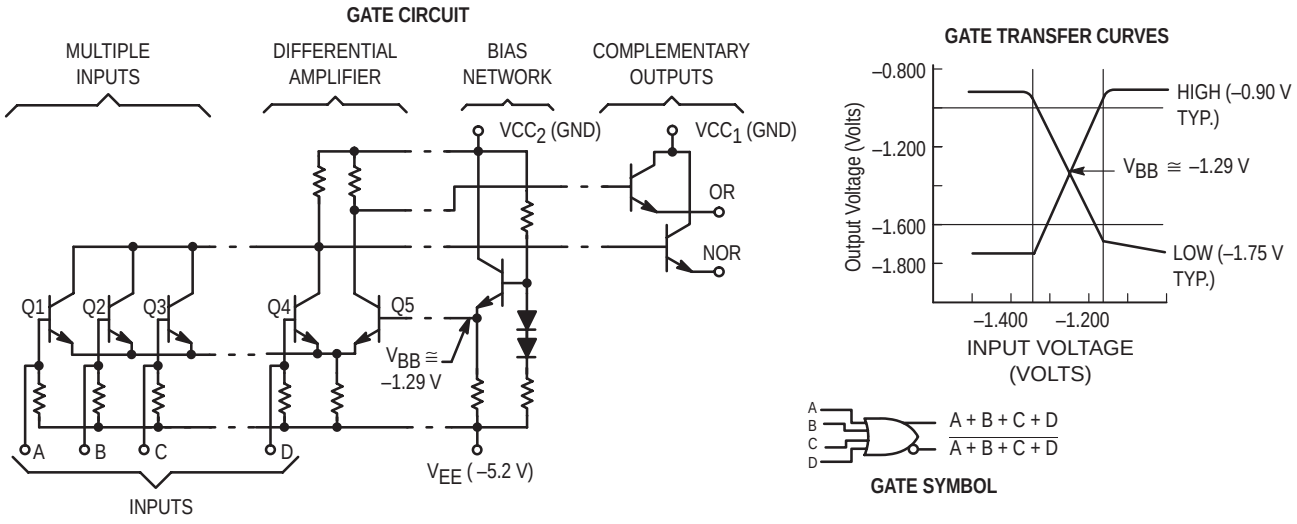


Figure 5 – MECL 10K GATE STRUCTURE AND SWITCHING BEHAVIOR

CIRCUIT DESCRIPTION

The typical MECL 10K circuit, Figure 5, consists of a differential–amplifier input circuit, a temperature and voltage compensated bias network, and emitter–follower outputs to restore dc levels and provide buffering for transmission line driving. High fan–out operation is possible because of the high input impedance of the differential amplifier input and the low output impedance of the emitter follower outputs. Power–supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the OR function and its complement, the NOR function. The design of the MECL 10H gate is unchanged, with two exceptions. The bias network has been replaced with a voltage regulator, and the differential amplifier source resistor has been replaced with a constant current source. (See section 2 for additional MECL 10H information.)

Power–Supply Connections – Any of the power supply levels, V_{TT}, V_{CC}, or V_{EE} may be used as ground; however, the use of the V_{CC} node as ground results in best noise immunity. In such a case: V_{CC} = 0, V_{TT} = –2.0 V, V_{EE} = –5.2 V.

System Logic Specifications – The output logic swing of 0.85 V, as shown by the typical transfer characteristics curve, varies from a LOW state of V_{OL} = –1.75 V to a HIGH state of V_{OH} = –0.9 V with respect to ground.

Positive logic is used when reference is made to logical “0’s” or “1’s.” Then

“0” = –1.75 V = LOW

typical

“1” = –0.9 V = HIGH

Circuit Operation – Beginning with all logic inputs LOW (nominal –1.75 V), assume that Q1 through Q4 are cut off because their P–N base–emitter junctions are not conducting, and the forward–biased Q5 is conducting. Under these conditions, with the base of Q5 held at –1.29 V by the V_{BB} network, its emitter will be one diode drop (0.8 V) more negative than its base, or –2.09 V. (The 0.8 V differential is a characteristic of this P–N junction.) The base–to–emitter differential across Q1 – Q4 is then the difference between the common emitter voltage (–2.09 V) and the LOW logic level (–1.75 V) or 0.34 V. This is less than the threshold voltage of Q1 through Q4 so that these transistors will remain cut off.

When any one (or all) of the logic inputs are shifted upward from the –1.75 V LOW state to the –0.9 V HIGH state, the base voltage of that transistor increases beyond the threshold point and the transistor turns on. When this happens, the voltage at the common–emitter point rises from –2.09 V to –1.7 (one diode drop below the –0.9 V base voltage of the input transistor), and since the base voltage of the fixed–bias transistor (Q5) is held at –1.29 V, the base–emitter voltage Q5 cannot sustain conduction. Hence, this transistor is cut off.

This action is reversible, so that when the input signal(s) return to the LOW state, Q1 – Q4 are again turned off and Q5 again becomes forward biased. The collector voltages resulting from the switching action of Q1 – Q4 and Q5 are transferred through the output emitter–follower to the output terminal. Note that the differential action of the switching transistors (one section being off when the other is on) furnishes simultaneous complementary signals at the output. This action also maintains constant power supply current drain.

DEFINITIONS OF LETTER SYMBOLS AND ABBREVIATIONS

Current:

I_{CC} Total power supply current drawn from the positive supply by a MECL unit under test.

I_{CBO} Leakage current from input transistor on MECL devices without pulldown resistors when test voltage is applied.

I_{CCH} Current drain from V_{CC} power supply with all inputs at logic HIGH level.

I_{CCL} Current drain from V_{CC} power supply with all inputs at logic LOW level.

I_E Total power supply current drawn from a MECL test unit by the negative power supply.

I_F Forward diode current drawn from an input of a saturated logic–to–MECL translator when that input is at 0.4V.

I_{in} Current into the input of the test unit when a maximum logic HIGH ($V_{IH\ max}$) is applied at that input.

I_{INH} HIGH level input current into a node with a specified HIGH level ($V_{IH\ max}$) logic voltage applied to that node. (Same as I_{in} for positive logic.)

I_{INL} LOW level input current, into a node with a specified LOW level ($V_{IL\ min}$) logic voltage applied to that node.

I_L Load current that is drawn from a MECL circuit output when measuring the output HIGH level voltage.

I_{OH} HIGH level output current: the current flowing into the output, at a specified HIGH level output voltage.

I_{OL} LOW level output current: the current flowing into the output, at a specified LOW level output voltage.

I_{OS} Output short circuit current.

I_{out} Output current (from a device or circuit, under such conditions mentioned in context).

I_{OZL} Output off current LOW – The current flowing out of a disabled 3–state output with a specified LOW output voltage applied.

I_{OZH} Output off current HIGH – The current flowing into a disabled 3–state output with a specified HIGH output.

I_R Reverse current drawn from a transistor input of a test unit when V_{EE} is applied to that input.

$I_{R'}$ Reverse current leakage into an input of a saturated logic MECL/PECL translator when that input is at V_{CC}.

I_{SC} Short–circuit current drawn from a translator saturating output when that output is at ground potential.

Voltage:

V_{BB} Reference bias supply voltage.

V_{BE} Base–to–emitter voltage drop of a transistor at specified collector and base currents.

V_{CB} Collector–to–base voltage drop of a transistor at specified collector and base currents.

V_{CC} General term for the most positive power supply voltage to a MECL device (usually ground, except for translator and interface circuits).

V_{CC1} Most positive power supply voltage (output devices). (Usually ground for MECL devices.)

V_{CC2} Most positive power supply voltage (current switches and bias driver). (Usually ground for MECL devices.)

V_{CMR} The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –5.2V. Note for PECL operation, the V_{CMR}(min) will be fixed at 5.0V – |V_{CMR}(min)|.

V_{EE} Most negative power supply voltage for a circuit (usually –5.2 V for MECL devices).

V_F Input voltage for measuring I_F on TTL interface circuits.

V_{IH} Input logic HIGH voltage level (nominal value).

$V_{IH\ max}$ Maximum HIGH level input voltage: The most positive (least negative) value of high–level input voltage, for which operation of the logic element within specification limits is guaranteed.

V_{IHA} Input logic HIGH threshold voltage level.

$V_{IHA\ min}$ Minimum input logic HIGH level (threshold) voltage for which performance is specified.

$V_{IH\ min}$ Minimum HIGH level input voltage: The least positive (most negative) value of HIGH level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} Input logic LOW voltage level (nominal value).

$V_{IL\ max}$ Maximum LOW level input voltage: The most positive (least negative) value of LOW level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{ILA} Input logic LOW threshold voltage level.

$V_{ILA\ max}$ Maximum input logic LOW level (threshold) voltage for which performance is specified.

$V_{IL\ min}$ Minimum LOW level input voltage: The least positive (most negative) value of LOW level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{in} Input voltage (to a circuit or device).

V_{max} Maximum (most positive) supply voltage, permitted under a specified set of conditions.

V_{OH} Output logic HIGH voltage level: The voltage level at an output terminal for a specified output current, with the specified conditions applied to establish a HIGH level at the output.

t_{AA} Address Access Time

Voltage (cont.):

V_{OHA}	Output logic HIGH threshold voltage level.
$V_{OHA\ min}$	Minimum output HIGH threshold voltage level for which performance is specified.
$V_{OH\ max}$	Maximum output HIGH or high–level voltage for given inputs.
$V_{OH\ min}$	Minimum output HIGH or high–level voltage for given inputs.
V_{OL}	Output logic LOW voltage level: The voltage level at the output terminal for a specified output current, with the specified conditions applied to establish a LOW level at the output.
V_{OLA}	Output logic LOW threshold voltage level.
$V_{OLA\ max}$	Maximum output LOW threshold voltage level for which performance is specified.
$V_{OL\ max}$	Maximum output LOW level voltage for given inputs.
$V_{OL\ min}$	Minimum output LOW level voltage for given inputs.
V_{TT}	Line load–resistor terminating voltage for outputs from a MECL device.

Time Parameters:

t+	Waveform rise time (LOW to HIGH), 10% to 90%, or 20% to 80%, as specified.
t–	Waveform fall time (HIGH to LOW), 90% to 10%, or 80% to 20%, as specified.
t_r	Same as t+
t_f	Same as t–
t+–	Propagation Delay, see Figure 12 on page 24.
t–+	Propagation Delay, see Figure 12 on page 24.
t_{pd}	Propagation delay, input to output from the 50% point of the input waveform at pin x (falling edge noted by – or rising edge noted by +) to the 50% point of the output waveform at pin y (falling edge noted by – or rising edge noted by +). (Cf Figure 12 on page 24.)
$t_{x\pm y\pm}$	
t_{x+}	Output waveform rise time as measured from 10% to 90% or 20% to 80% points on waveform (whichever is specified) at pin x with input conditions as specified.
$t_{x–}$	Output waveform fall time as measured from 90% to 10% or 80% to 20% points on waveform (whichever is specified) at pin x, with input conditions as specified.
f_{Tog}	Toggle frequency of a flip–flop or counter device.
f_{shift}	Shift rate for a shift register.

Temperature:

T_{stg}	Maximum temperature at which device may be stored without damage or performance degradation.
T_J	Junction (or die) temperature of an integrated circuit device.
T_A	Ambient (environment) temperature existing in the immediate vicinity of an integrated circuit device package.
θ_{JA}	Thermal resistance of an IC package, junction to ambient.
θ_{JC}	Thermal resistance of an IC package, junction to case.
lfpm	Linear feet per minute.
θ_{CA}	Thermal resistance of an IC package, case to ambient.

Miscellaneous:

e_g	Signal generator inputs to a test circuit.
TP_{in}	Test point at input of unit under test.
TP_{out}	Test point at output of unit under test.
D.U.T.	Device under test.
C_{in}	Input capacitance.
C_{out}	Output capacitance.
Z_{out}	Output impedance.
P_D	The total dc power applied to a device, not including any power delivered from the device to a load.
R_L	Load Resistance.
R_T	Terminating (load) resistor.
R_p	An input pull–down resistor (i.e., connected to the most negative voltage).
P.U.T.	Pin under test.

MECL Logic Surface Mount

WHY SURFACE MOUNT?

Surface Mount Technology is now being utilized to offer answers to many problems that have been created in the use of insertion technology.

Limitations have been reached with insertion packages and PC board technology. Surface Mount Technology offers the opportunity to continue to advance the State-of-the-Art designs that cannot be accomplished with Insertion Technology.

Surface Mount Packages allow more optimum device performance with the smaller Surface Mount configuration. Internal lead lengths, parasitic capacitance and inductance that placed limitations on chip performance have been reduced.

The lower profile of Surface Mount Packages allows more boards to be utilized in a given amount of space. They are stacked closer together and utilize less total volume than insertion populated PC boards.

Printed circuit costs are lowered with the reduction of the number of board layers required. The elimination or reduction of the number of plated through holes in the board, contribute significantly to lower PC board prices.

Surface Mount assembly does not require the preparation of components that are common on insertion technology lines. Surface Mount components are sent directly to the assembly line, eliminating an intermediate step.

Automatic placement equipment is available that can place Surface Mount components at the rate of a few thousand per hour to hundreds of thousands of components per hour.

Surface Mount Technology is cost effective, allowing the manufacturer the opportunity to produce smaller units and offer increased functions with the same size product.

MECL AVAILABILITY IN SURFACE MOUNT

ON Semiconductor is now offering MECL 10K and MECL 10H in the PLCC (Plastic Leaded Chip Carrier) packages.

MECL in PLCC may be ordered in conventional plastic rails or on Tape and Reel. Refer to the Tape and Reel section for ordering details.

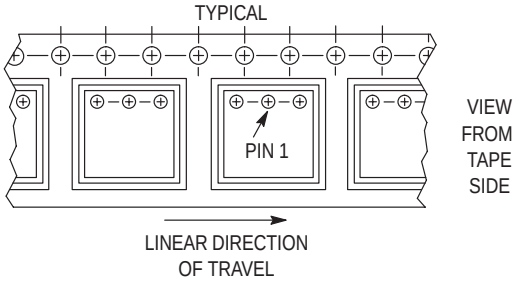
TAPE AND REEL

ON Semiconductor has now added the convenience of Tape and Reel packaging for our growing family of standard Integrated Circuit products. The packaging fully conforms to the latest EIA RS-481A specification. The antistatic embossed tape provides a secure cavity sealed with a peel-back cover tape.

GENERAL INFORMATION

- Reel Size 13 inch (330 mm) Suffix: R2
- Tape Width 16 mm
- Units/Reel 1000

MECHANICAL POLARIZATION



ORDERING INFORMATION

- Minimum Lot Size/Device Type = 3000 Pieces.
- No Partial Reel Counts Available.
- To order devices which are to be delivered in Tape and Reel, add the appropriate suffix to the device number being ordered.

EXAMPLE:

ORDERING CODE	SHIPMENT METHOD
MC10101FN	Magazines (Rails)
MC10101FNR2	13 inch Tape and Reel
MC10H101FN	Magazines (Rails)
MC10H101FNR2	13 inch Tape and Reel
MC12015D	Magazines (Rails)
MC12015DR2	13 inch Tape and Reel

DUAL-IN-LINE PACKAGE TO PLCC PIN CONVERSION DATA

The following tables give the equivalent I/O pinouts of Dual-In-Line (DIL) packages and Plastic Leaded Chip Carrier (PLCC) packages.

Pin Conversion Tables

8–Pin DIL to 20–Pin PLCC

8 PIN DIL	1	2	3	4	5	6	7	8
20 PIN PLCC	2	5	7	10	12	15	17	20

14–Pin DIL to 20–Pin PLCC

14 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14
20 PIN PLCC	2	3	4	6	8	9	10	12	13	14	16	18	19	20

16–Pin DIL to 20–Pin PLCC

16 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
20 PIN PLCC	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20

20–Pin DIL to 20–Pin PLCC

20 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
20 PIN PLCC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

24–Pin DIL to 28–Pin PLCC

24 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
28 PIN PLCC	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	23	24	25	26	27	28

MECL POSITIVE AND NEGATIVE LOGIC

INTRODUCTION

The increasing popularity and use of emitter coupled logic has created a dilemma for some logic designers. Saturated logic families such as TTL have traditionally been designed with the NAND function as the basic logic function, however, the basic ECL logic function is the NOR function (positive logic). Therefore, the designer may either design ECL systems with positive logic using the NOR, or design with negative logic using the NAND. Which is the more convenient? On the one hand the designer is familiar with positive logic levels and definitions, and on the other hand, he is familiar with implementing systems using NAND functions. Perhaps a presentation of the basic definitions and characteristics of positive and negative logic will clarify the situation and eliminate misunderstanding.

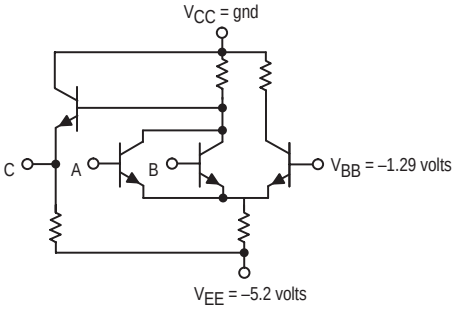


Table 1

INPUTS		OUTPUT
A	B	C
LO	LO	HI
LO	HI	LO
HI	LO	LO
HI	HI	LO

HI = –0.9 volts
LO = –1.7 volts

Table 2

NEGATIVE LOGIC

INPUTS		OUTPUT
A	B	C
1	1	0
1	0	1
0	1	1
0	0	1

$C = \overline{A \bullet B}$

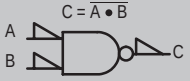


Table 3

POSITIVE LOGIC

INPUTS		OUTPUT
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

$C = \overline{A + B}$

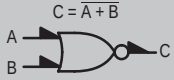


Figure 6 – Basic MECL Gate Circuit and Logic Function In Positive and Negative Nomenclature.

LOGIC EQUIVALENCIES

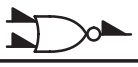
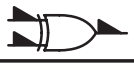
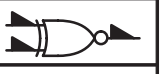
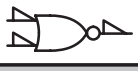
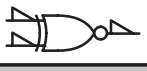
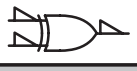
Binary logic must have two states to represent the binary 1 and 0. With ECL the typical states are a high level of –0.9 volts and a low level of –1.7 volts. Two choices are possible then to represent the binary 1 and 0. Positive logic defines the 1 or "true" state as the most positive voltage level, whereas negative logic defines the most negative voltage level as the 1 or "true" state. Because of the difference in definition of states, the basic ECL gate is a NOR function in positive logic and is a NAND function in negative logic.

Figure 6 more clearly shows the above comparison of functions. Table 1 lists the output voltage level as a function of input voltage levels of the MECL gate circuit shown. Table 2 translates the voltage levels into the appropriate negative logic levels which show the function to be $C = \overline{A \bullet B}$; that is, the circuit performs the NAND function. Table 3 translates the equivalent positive logic function into $C = \overline{A + B}$, the NOR function.

Similar comparisons could be made for other positive logic functions. As an example, the positive OR function translates to the negative AND function. Figure 7 shows a comparison of several common logic functions.

Any function available in a logic family may be expressed in terms of positive or negative logic, bearing in mind the definition of logic levels. The choice of logic definition, as previously stated, is dependent on the designer. ON Semiconductor provides both positive and negative logic symbols on data sheets for the popular MECL 10,000 logic series.

Figure 7 – Comparative Positive and Negative Logic Functions.

		POSITIVE LOGIC					
INPUTS							
A	B	AND	OR	NAND	NOR	EXOR	EXNOR
LO	LO	LO	LO	HI	HI	LO	HI
LO	HI	LO	HI	HI	LO	HI	LO
HI	LO	LO	HI	HI	LO	HI	LO
HI	HI	HI	HI	LO	LO	LO	HI
A	B	OR	AND	NOR	NAND	EXNOR	EXOR
INPUTS							
		NEGATIVE LOGIC					

SUMMARY

Conversion from one logic form to another or the use of a particular logic form need not be a complicated process. If the designer uses the logic form with which he is familiar and bears in mind the previously mentioned definition of levels, problems arising from definition of logic functions should be minimized.

REFERENCE

Y. Chu, Digital Computer Design Fundamentals
New York, McGraw–Hill, 1962

TECHNICAL DATA

GENERAL CHARACTERISTICS AND SPECIFICATIONS

(See pages 15 through 16 for definitions of symbols and abbreviations.)

In subsequent sections of this Data Book, the important MECL parameters are identified and characterized, and complete data provided for each of the functions. To make this data as useful as possible, and to avoid a great deal of repetition, the data that is common to all functional blocks in a line is not repeated on each individual sheet. Rather, these common characteristics, as well as the application information that applies to each family, are discussed in this section.

In general, the common characteristics of major importance are:

Maximum Ratings, including both dc and ac characteristics and temperature limits;

Transfer Characteristics, which define logic levels and switching thresholds;

DC Parameters, such as output levels, threshold levels, and forcing functions.

AC Parameters, such as propagation delays, rise and fall times and other time dependent characteristics.

In addition, this section will discuss general layout and design guides that will help the designer in building and testing systems with MECL circuits.

LETTER SYMBOLS AND ABBREVIATIONS

Throughout this section, and in the subsequent data sheets, letter symbols and abbreviations will be used in discussing electrical characteristics and specifications. The symbols used in this book, and their definitions, are listed on the preceding pages.

MAXIMUM RATINGS

The limit parameters beyond which the life of the devices may be impaired are given in Table 4. In addition, Table 5 provides certain limits which, if exceeded, will not damage the devices, but could degrade the performance below that of the guaranteed specifications.

Table 4 – LIMITS BEYOND WHICH DEVICE LIFE MAY BE IMPAIRED

Characteristic	Symbol	Unit	MECL 10H	MECL 10K
Power Supply	V_{EE}	Vdc	–8.0 to 0	–8.0 to 0
Input Voltage (V_{CC} = 0)	V_{in}	Vdc	0 to V_{EE}	0 to V_{EE}
Output Source Current Continuous	I_{out}	mAdc	50	50
Output Source Current Surge	I_{out}	mAdc	100	100
Storage Temperature	T_{stg}	°C	–65 to +150	–65 to +150
Junction Temperature Ceramic Package	T_J	°C	165	165
Junction Temperature Plastic Package	T_J	°C	140	140

NOTES: 1. Maximum T_J may be exceeded ($\leq$ 250°C) for short periods of time ($\leq$ 240 hours) without significant reduction in device life.
2. For long term ($\geq$ 10 yrs.) max T_J of 110°C required. Max T_J may be exceeded ($\leq$ 175°C) for short periods of time ($\leq$ 240 hours) without significant reduction in device life.

Table 5 – LIMITS BEYOND WHICH PERFORMANCE MAY BE DEGRADED

Characteristics	Symbol	Unit	MECL 10H	MECL 10K
Operating Temperature Range Commercial	T_A	°C	0 to +75	–30 to +85
Supply Voltage (V_{CC} = 0)	V_{EE}	Vdc	–4.94 to –5.46	–4.68 to –5.72
Output Drive Commercial	–	Ω	50 Ω to –2.0 Vdc	50 Ω to –2.0 Vdc

NOTES: 1. With airflow $\geq$ 500 lfpm.
2. Functionality only. Data sheet limits are specified for –5.2 V ± 0.010 V.
3. Except MC1648 which has an internal output pulldown resistor.
4. Functional and Data sheet limits.

MECL TRANSFER CURVES and SPECIFICATION TEST POINTS

Figure 8 – MECL 10K

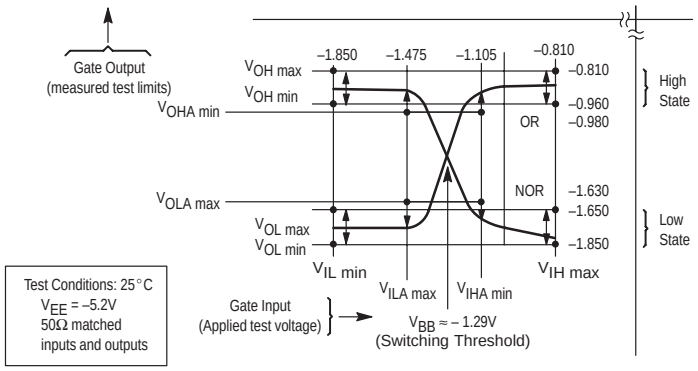
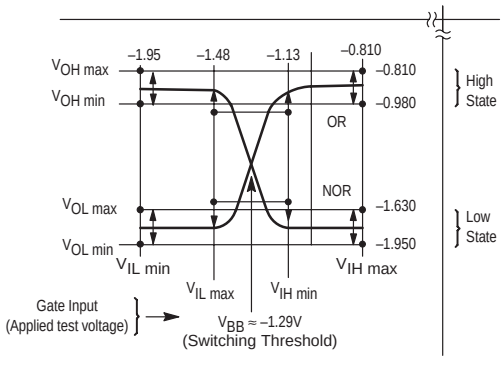


Figure 9 – MECL 10H



MECL TRANSFER CURVES

For MECL logic gates, the dual (complementary) outputs must be represented by two transfer curves: one to describe the OR switching action and one to describe the NOR switching action. Typical transfer curves and associated data for the MECL 10K/10H family are shown in Figure 8 and Figure 9, respectively.

It is not necessary to measure transfer curves at all points of the curves. To guarantee correct operation it is sufficient merely to measure two sets of min/max logic level parameters.

The first set is obtained for 10K by applying test voltages, $V_{IL\ min}$ and $V_{IH\ max}$ (sequentially) to the gate inputs, and measuring the OR and NOR output levels to make sure they are between $V_{OL max}$ and $V_{OL min}$, and $V_{OH max}$ and $V_{OH min}$ specifications.

The second set of logic level parameters relates to the switching thresholds. This set of data is distinguished by an "A" in symbol subscripts. A test voltage, $V_{ILA\ max}$, is applied to the gate and the NOR and OR outputs are measured to see that they are above the $V_{OHA\ min}$ and below the $V_{OLA\ max}$ levels, respectively. Similar checks are made using the test input voltage $V_{IHA\ min}$.

The result of these specifications insures that:

(a) The switching threshold ($\approx V_{BB}$) falls within the darkest rectangle; i.e. switching does not begin outside this rectangle;

(b) Quiescent logic levels fall in the lightest shaded ranges;

(c) Guaranteed noise immunity is met.

As shown in Figure 10, MECL 10K outputs rise with increasing ambient temperature. All circuits in each family have the same worst–case output level specifications regardless of power dissipation or junction temperature differences to reduce loss of noise margin due to thermal differences.

All of these specifications assume –5.2 V power supply operation. Operation at other power–supply voltages is possible, but will result in further transfer curve changes. Table 6 gives rate of change of output voltages as a function of power supply.

Figure 10 – TYPICAL TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE (MECL 10K)

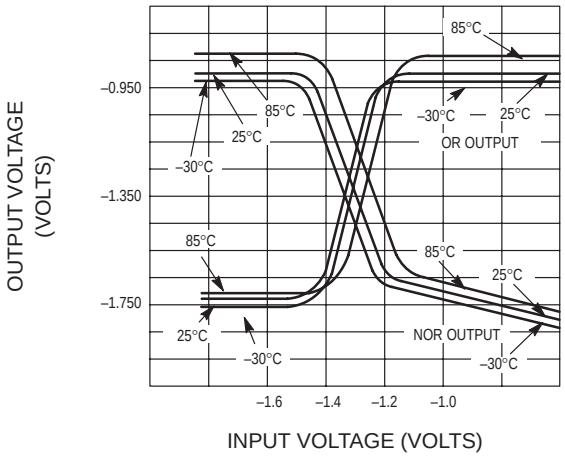


Table 6 – TYPICAL LEVEL CHANGE RATES / 1V

Voltage	MECL 10H	MECL 10K
$\Delta V_{OH}/\Delta V_{EE}$	0.008	0.016
$\Delta V_{OL}/\Delta V_{EE}$	0.020	0.250
$\Delta V_{BB}/\Delta V_{EE}$	0.010	0.148

NOISE MARGIN

"Noise margin" is a measure of logic circuit's resistance to undesired switching. MECL noise margin is defined in terms of the specification points surrounding the switching threshold. The critical parameters of interest here are those designated with the "A" subscript ($V_{OHA\ min}$, $V_{OLA\ max}$, $V_{IHA\ min}$, $V_{ILA\ max}$) in the transfer characteristic curves. MECL 10H is specified and tested with:

$$V_{OHA\ min} = V_{OH\ min}$$
$$V_{OLA\ max} = V_{OL\ max}$$
$$V_{IHA\ min} = V_{IH\ min}$$

and

$$V_{ILA\ max} = V_{IL\ max}$$

Guaranteed noise margin (NM) is defined as follows:

$$NM_{HIGH\ LEVEL} = V_{OHA\ min} - V_{IHA\ min}$$
$$NM_{LOW\ LEVEL} = V_{ILA\ max} - V_{OLA\ max}$$

To see how noise margin is computed, assume a MECL gate drives a similar MECL gate, Figure 11.

At a gate input (point B) equal to $V_{ILA\ max}$, MECL gate #2 can begin to enter the shaded transition region.

This is a "worst case" condition, since the $V_{OLA\ max}$ specification point guarantees that no device can enter the transition region before an input equal to $V_{ILA\ max}$ is reached. Clearly then, $V_{ILA\ max}$ is one critical point for noise margin computation, since it is the edge of the transition region.

To find the other critical voltage, consider the output from MECL gate #1 (point A). What is the most positive value possible for this voltage (considering worst case specifications)? From Figure 11 it can be observed that the $V_{OLA\ max}$ specification insures that the LOW state OR output from gate #1 can be no greater than $V_{OLA\ max}$.

Note that $V_{OLA\ max}$ is more negative than $V_{ILA\ max}$. Thus, with $V_{OLA\ max}$ at the input to gate #2, the transition region is not yet reached. (The input voltage to gate #2 is still to the left of $V_{ILA\ max}$ on the transfer curve.)

In order to ever run the chance of switching gate #2, we would need an additional voltage, to move the input from $V_{OLA\ max}$ to $V_{ILA\ max}$. This constitutes the "safety factor" known as noise margin. It can be calculated as the magnitude of the difference between the two specification voltages, or for the MECL 10K levels shown:

$$NM_{LOW} = V_{ILA\ max} - V_{OLA\ max}$$
$$= -1.475\ V - (-1.630\ V)$$
$$= 155\ mV.$$

Similarly, for the HIGH state:

$$NM_{HIGH} = V_{OHA\ min} - V_{IHA\ min}$$
$$= -0.980\ V - (-1.105\ V)$$
$$= 125\ mV$$

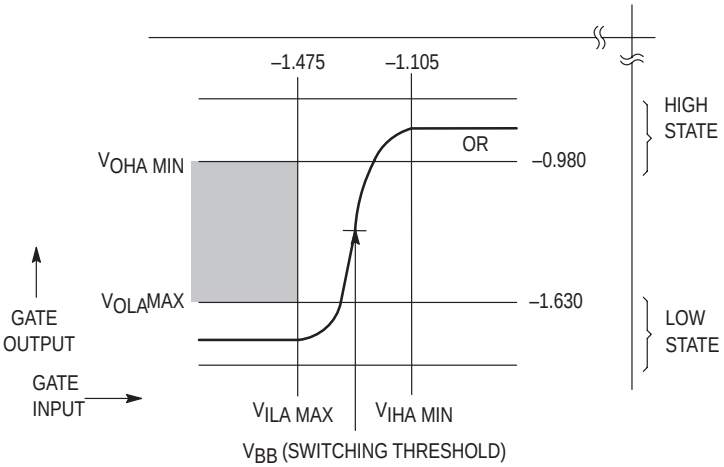
Analogous results are obtained when considering the "NOR" transfer data.

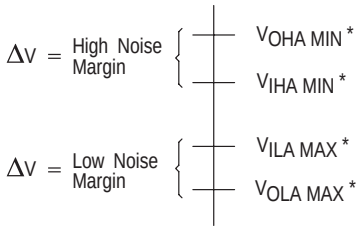
Note that these noise margins are absolute worst case conditions. The lessor of the two noise margins is that for the HIGH state, 125 mV. This then, constitutes the guaranteed margin against signal undershoot, and power or thermal disturbances.

As shown in the table, typical noise margins are usually better than guaranteed – by about 75 mV. For MECL 10H the "noise margin" is 150 mV for NM low and NM high. (See Section 3 for details.)

Noise margin is a dc specification that can be calculated, since it is defined by specification points tabulated on MECL data sheets. However, by itself, this specification does not give a complete picture regarding the noise immunity of a system built with a particular set of circuits. Overall system noise immunity involves not only noise–margin specifications, but also other circuit–related factors that determine how difficult it is to apply a noise signal of sufficient magnitude and duration to cause the circuit to propagate a false logic state. In general, then, noise immunity involves line impedances, circuit output impedances, and propagation delay in addition to noise–margin specifications. This subject to discussed in greater detail in the MECL System Design Handbook, HB205/D.

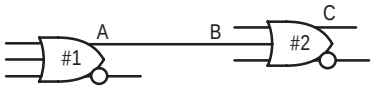
Figure 11 – MECL Noise Margin Data





*$V_{OHA\ min} = V_{OH\ min}$, $V_{OLA\ max} = V_{OL\ max}$, $V_{IHA\ min} = V_{IH\ min}$ and $V_{ILA\ max} = V_{IL\ max}$ for MECL 10H.

Specification Points for Determining Noise Margin



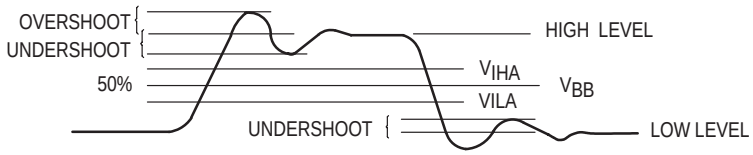
Noise Margin Computations

Family	Guaranteed Worst–Case dc Noise Margin (V)	Typical dc Noise Margin (V)
MECL 10H	0.150	0.270
MECL 10K	0.125	0.210

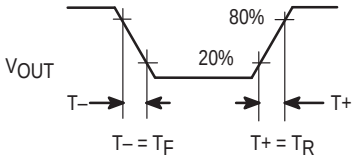
AC OR SWITCHING PARAMETERS

Time–dependent specifications are those that define the effects of the circuit on a specified input signal, as it travels through the circuit. They include the time delay involved in changing the output level from one logic state to another. In addition, they include the time required for the output of a circuit to respond to the input signal, designated as propagation delay, MECL waveform and propagation delay terminologies are depicted in Figure 12. Specific rise, fall, and propagation delay times are given on the data sheet for each specific functional block, but like the transfer characteristics, ac parameters are temperature and voltage dependent. Typical variations for MECL 10K are given in the curves of Figure 13 through Figure 16.

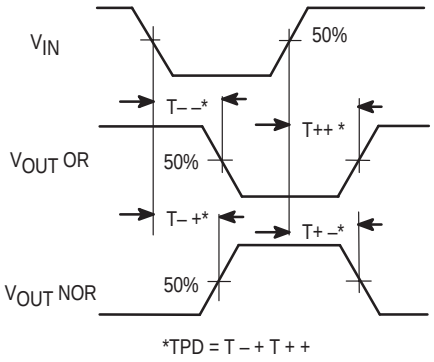
Figure 12 – TYPICAL LOGIC WAVEFORMS



MECL WAVEFORM TERMINOLOGY



MECL 10K and MECL 10H Rise and Fall Times



MECL Propagation Delay

Figure 13 – TYPICAL PROPAGATION DELAY t– – versus V_{EE} AND TEMPERATURE (MECL 10K)

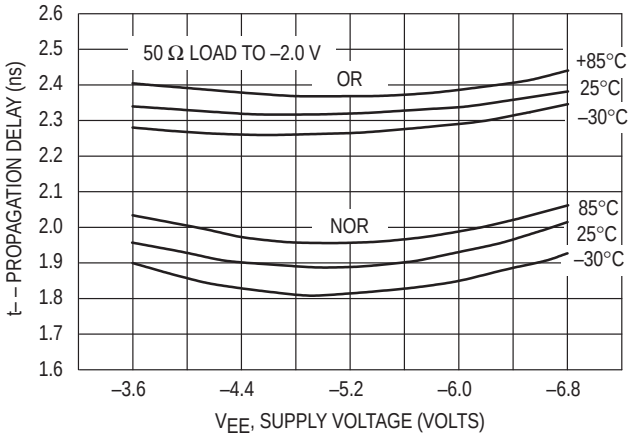


Figure 14 – TYPICAL PROPAGATION DELAY t+ + versus V_{EE} AND TEMPERATURE (MECL 10K)

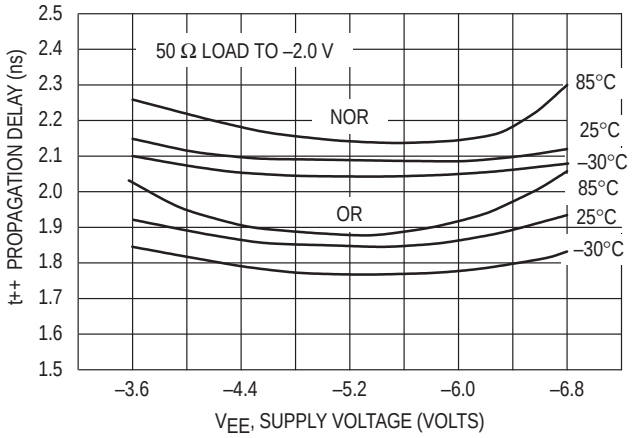


Figure 15 – TYPICAL FALL TIME (90% to 10%) versus TEMPERATURE AND SUPPLY VOLTAGE (MECL 10K)

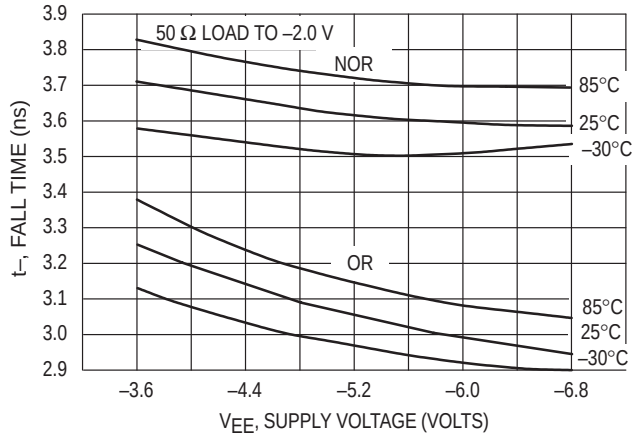
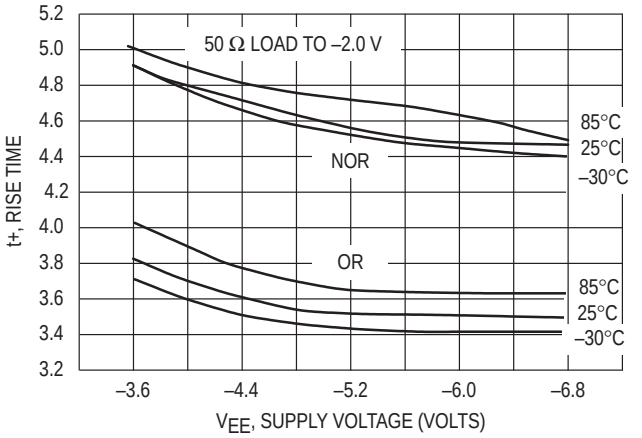


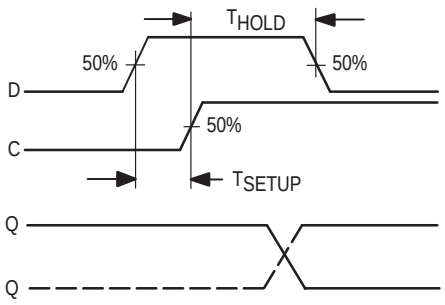
Figure 16 – TYPICAL FALL TIME (10% to 90%) versus TEMPERATURE AND SUPPLY VOLTAGE (MECL 10K)



SETUP AND HOLD TIMES

Setup and hold times are two ac parameters which can easily be confused unless clearly defined. For MECL logic devices, t_{setup} is the minimum time (50% – 50%) before the positive transition of the clock pulse (C) that information must be present at the Data input (D) to insure proper operation of the device. The t_{hold} is defined similarly as the minimum time after the positive transition of the clock pulse (C) that the information must remain unchanged at the Data input (D) to insure proper operation. Setup and hold waveforms for logic devices are shown in Figure 17.

Figure 17 – SETUP AND HOLD WAVEFORMS FOR MECL LOGIC DEVICES



TESTING MECL 10H AND MECL 10K

To obtain results correlating with ON Semiconductor circuit specifications certain test techniques must be used. A schematic of a typical gate test circuit is shown in Figure 18. This test circuit is the standard ac test configuration for most MECL devices. (Exceptions are shown with device specification.)

A solid ground plane is used in the test setup, and capacitors bypass V_{CC1}, V_{CC2}, and V_{EE} pins to ground. All power leads and signal leads are kept as short as possible.

The sampling scope interface runs directly to the 50–ohm inputs of Channel A and B via 50–ohm coaxial cable. Equal–length coaxial cables must be used between the test set and the A and B scope inputs. A 50–ohm coax cable such as RG58/U or RG188A/U, is recommended.

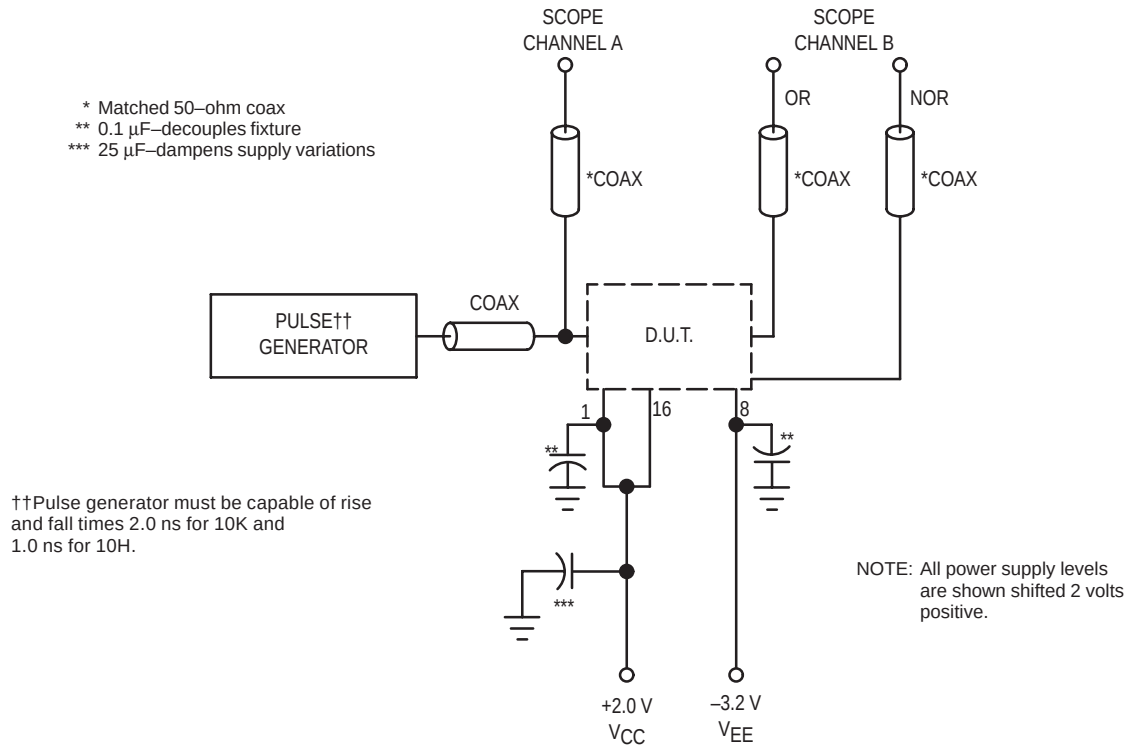
Interconnect fittings should be 50–ohm GR, BNC, Sealectro Conhex, or equivalent. Wire length should be < ¼ inch from TP_{in} to input pin and TP_{out} to output pin.

The pulse generator must be capable of 2.0 ns rise and fall times for MECL 10K and 1.5 ns for MECL 10H and MECL III. In addition, the generator voltage must have an offset to give MECL signal swings of ≈ ±400 mV about a threshold of ≈ +0.7 V when V_{CC} = +2.0 and V_{EE} = –3.2 V for ac testing of logic devices.

The power supplies are shifted +2.0 V, so that the device under test has only one resistor value to load into the precision 50–ohm input impedance of the sampling oscilloscope. Use of this technique yields a close correlation between ON Semiconductor and customer testing. Unused outputs are loaded with a 50–ohm resistor (100–ohm for MC105XX devices) to ground. The positive supply (V_{CC}) should be decoupled from the test board by RF type 25 μF capacitors to ground. The V_{CC} pins are bypassed to ground with 0.1 μF, as is the V_{EE} pin.

Additional information on testing MECL 10K and understanding data sheets is found in Application Note AN701/D and the MECL System Design Handbook, HB205/D.

Figure 18 – MECL LOGIC SWITCHING TIME TEST SETUP



OPERATIONAL DATA

POWER SUPPLY CONSIDERATIONS

MECL circuits are characterized with the V_{CC} point at ground potential and the V_{EE} point at –5.2 V. While this MECL convention is not necessarily mandatory, it does result in maximum noise immunity. This is so because any noise induced on the V_{EE} line is applied to the circuit as a common–mode signal which is rejected by the differential action of the MECL input circuit. Noise induced into the V_{CC} line is not cancelled out in this fashion. Hence, a good system ground at the V_{CC} bus is required for best noise immunity. Also, MECL 10H circuits may be operated with V_{EE} at –4.5 V with a negligible loss of noise immunity.

Power supply regulation which will achieve 10% regulation or better at the device level is recommended. The –5.2 V power supply potential will result in best circuit speed. Other values for V_{EE} may be used. A more negative voltage will increase noise margins at a cost of increased power dissipation. A less negative voltage will have just the opposite effect. (Noise margins and performance specifications of MECL 10H are unaffected by variations in V_{EE} because of the internal voltage regulation.)

On logic cards, a ground plane or ground bus system should be used. A bus system should be wide enough to prevent significant voltage drops between supply and device and to produce a low source inductance.

Although little power supply noise is generated by MECL logic, power supply bypass capacitors are recommended to handle switching currents caused by stray capacitance and asymmetric circuit loading. A parallel combination of a 1.0 μF and a 100 pF capacitor at the power entrance to the board, and a 0.01 μF low–inductance capacitor between ground and the –5.2 V line every four to six packages, are recommended.

Most MECL 10H, MECL 10K and MECL III circuits have two V_{CC} leads. V_{CC1} supplies current to the output transistors and V_{CC2} is connected to the circuit logic transistors. The separate V_{CC} pins reduce cross–coupling between individual circuits within a package when the outputs are driving heavy loads. Circuits with large drive capability, similar to the MC10110, have two V_{CC1} pins. All V_{CC} pins should be connected to the ground plane or ground bus as close to the package as possible.

For further discussion of MECL power supply considerations to be made in system designing, see MECL System Design Handbook, HB205/D.

POWER DISSIPATION

The power dissipation of MECL functional blocks is specified on their respective data sheets. This specification does not include power dissipated in the output devices due to output termination. The omission of internal output pulldown resistors permits the use of external terminations designed to yield best system performance. To obtain total operating power dissipation of a particular functional block in a system, the dissipation of the output transistor, under load, must be added to the circuit power dissipation.

Table 7 lists the power dissipation in the output transistors plus that in the external terminating resistors, for the more commonly used termination values and circuit configurations. To obtain true package power dissipation, one output–transistor power–dissipation value must be added to the specified package power dissipation for each external termination resistor used in conjunction with that package. To obtain system power dissipation, the stated dissipation in the external terminating resistors must be added as well. Unused outputs draw no power and may be ignored.

Table 7 – AVERAGE POWER DISSIPATION IN OUTPUT CIRCUIT WITH EXTERNAL TERMINATING RESISTORS

Terminating Resistor Value	Output Transistor Power Dissipation (mW)	Terminating Resistor Power Dissipation (mW)
150 ohms to –2.0 Vdc	5.0	4.3
100 ohms to –2.0 Vdc	7.5	6.5
75 ohms to –2.0 Vdc	10	8.7
50 ohms to –2.0 Vdc	15	13
2.0 k ohms to V_{EE}	2.5	7.7
1.0 k ohm to V_{EE}	4.9	15.4
680 ohms to V_{EE}	7.2	22.6
510 ohms to V_{EE}	9.7	30.2
270 ohms to V_{EE}	18.3	57.2
82 ohms to V_{CC} and 130 ohms to V_{EE}	15	140

LOADING CHARACTERISTICS

The differential input to MECL circuits offers several advantages. Its common–mode–rejection feature offers immunity against power–supply noise injection, and its relatively high input impedance makes it possible for any circuit to drive a relatively large number of inputs without deterioration of the guaranteed noise margin. Hence, dc fanout with MECL circuits does not normally present a design problem.

Graphs showing typical output voltage levels as a function of load current for MECL 10H, MECL 10K and MECL III shown in Figure 19. These graphs can be used to determine the actual output voltages for loads exceeding normal operation.

While dc loading causes a change in output voltage levels, thereby tending to affect noise margins, ac loading increases the capacitances associated with the circuit and, therefore, affects circuit speed, primarily rise and fall times.

MECL circuits typically have a 7 ohm output impedance and a relatively unaffected by capacitive loading on a positive–going output signal. However, the negative–going edge is dependent on the output pulldown or termination resistor. Loading close to a MECL output pin will cause an additional propagation delay of 0.1 ns per fanout load with a 50 ohm resistor to –2.0 Vdc or 270 ohms to –5.2 Vdc. A 100 ohm resistor to –2.0 Vdc or 510 ohms to –5.2 Vdc results in an additional 0.2 ns propagation delay per fanout load.

Terminated transmission line signal interconnections are used for best system performance. The propagation delay and rise time of a driving gate are affected very little by capacitance loading along a matched parallel–terminated transmission line. However, the delay and characteristic impedance of the transmission line itself are affected by the distributed capacitance. Signal propagation down the line will be increased by a factor, $\sqrt{1 + C_d/C_o}$. Here C_o is the normal intrinsic line capacitance, and C_d is the distributed capacitance due to loading and stubs off the line.

Maximum allowable stub lengths for loading off of a MECL 10K transmission line vary with the line impedance. For example, with Z_o = 50 ohms, maximum stub length would be 4.5 inches (1.8 in. for MECL III). But when Z_o = 100 ohms, the maximum allowable stub length is decreased to 2.8 inches (1.0 in. for MECL III).

The input loading capacitance of a MECL 10H and MECL 10K gate is about 2.9 pF and 3.3 pF for MECL III. To allow for the IC connector or solder connection and a short stub length, 5 to 7 pF is commonly used in loading calculations.

UNUSED MECL INPUTS

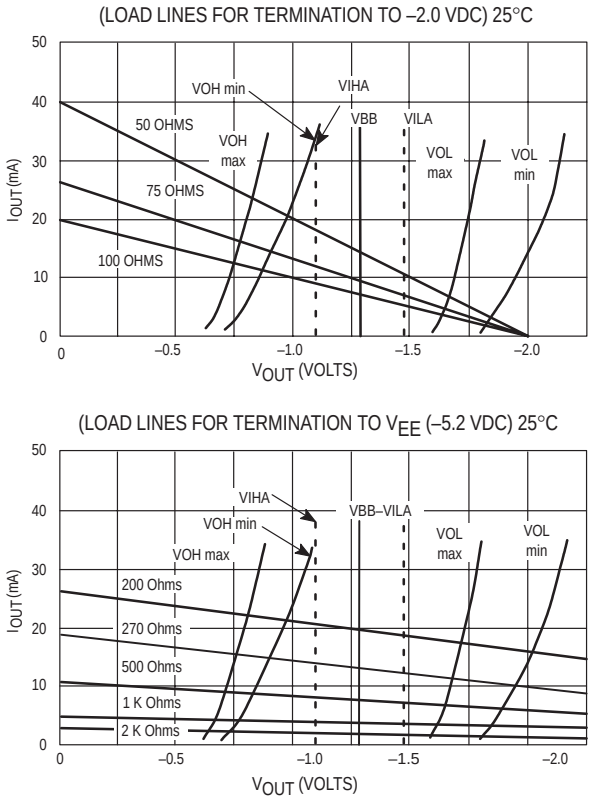
The input impedance of a differential amplifier, as used in the typical MECL input circuit, is very high when the applied signal level is low. Under low–signal conditions, therefore, any leakage to the input capacitance of the gate could cause a gradual buildup of voltage on the input lead, thereby adversely affecting the switching characteristics at low repetition rates.

All single–ended input MECL logic circuits contain input pulldown resistors between the input transistor bases and V_{EE}. As a result, unused inputs may be left unconnected (the resistor provides a sink for I_{CBO} leakage currents, and inputs are held sufficiently negative that circuits will not trigger due to noise coupled into such inputs). Input pulldown resistor values are typically 50 kΩ and are not to be used as pulldown resistors for preceding open–emitter outputs.

Some MECL devices do not have input pulldowns. Examples are the differential line receivers. If a single differential receiver within a package is unused, one input of that receiver must be tied to the V_{BB} pin provided, and the other input goes to V_{EE} or is left open.

MECL circuits do not operate properly when inputs are connected to V_{CC} for a HIGH logic level. Proper design practice is to set a HIGH level about –0.9 volts below V_{CC} with a resistor divider, a diode drop, or an unused gate output.

Figure 19 – OUTPUT VOLTAGE LEVELS versus DC LOADING



SYSTEM DESIGN CONSIDERATIONS

THERMAL MANAGEMENT

Circuit performance and long–term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low.

Electrical power dissipated in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25°C in still air. The temperature increase, then, depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point.

The temperature at the junction is a function of the packaging and mounting system's ability to remove heat generated in the circuit – from the junction region to the ambient environment. The basic formula (a) for converting power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D(\overline{\theta}_{JC} + \overline{\theta}_{CA}) \quad (1)$$

or

$$T_J = T_A + P_D(\overline{\theta}_{JA}) \quad (2)$$

where

T_J = maximum junction temperature
T_A = maximum ambient temperature
P_D = calculated maximum power dissipation including effects of external loads (see Power Dissipation in section III).
$\overline{\theta}_{JC}$ = average thermal resistance, junction to case
$\overline{\theta}_{CA}$ = average thermal resistance, case to ambient
$\overline{\theta}_{JA}$ = average thermal resistance, junction to ambient

This ON Semiconductor recommended formula has been approved by RADC and DESC for calculating a "practical" maximum operating junction temperature for MIL–M–38510 (JAN) MECL 10K devices.

Only two terms on the right side of equation (1) can be varied by the user – the ambient temperature, and the device case–to–ambient thermal resistance, $\overline{\theta}_{CA}$. (To some extent the device power dissipation can be also controlled, but under recommended use the V_{EE} supply and loading dictate a fixed power dissipation.) Both system air flow and the package mounting technique affect the $\overline{\theta}_{CA}$ thermal resistance term. $\overline{\theta}_{JC}$ is essentially independent of air flow and external mounting method, but is sensitive to package material, die bonding method, and die area.

Table 8 – THERMAL RESISTANCE VALUES FOR STANDARD MECL I/C PACKAGES

Thermal Resistance in Still Air										
Package Description							θ_{JA} (°C/Watt)		θ_{JC} (°C/Watt)	
No. Leads	Body Style	Body Material	Body WxL	Die Bond	Die Area (Sq. Mils)	Flag Area (Sq. Mils)	Avg.	Max.	Avg.	Max.
8	DIL	EPOXY	1/4″×3/8″	EPOXY	2496	8100	102	133	50	80
8	DIL	ALUMINA	1/4″×3/8″	SILVER/GLASS	2496	N/A	140	182	35	56
14	DIL	EPOXY	1/4″×3/4″	EPOXY	4096	6400	84	109	38	61
14	DIL	ALUMINA	1/4″×3/4″	SILVER/GLASS	4096	N/A	100	130	25	40
16	DIL	EPOXY	1/4″×3/4″	EPOXY	4096	12100	70	91	34	54
16	DIL	ALUMINA	1/4″×3/4″	SILVER/GLASS	4096	N/A	100	130	25	40
20	PLCC	EPOXY	0.35″×0.35″	EPOXY	4096	14,400	74	82	N/A (6)	N/A (6)
24	DIL (4)	EPOXY	1/2″×1–1/4″	EPOXY	8192	22500	67	87	31	50
24	DIL (5)	ALUMINA	1/2″×1–1/4″	SILVER/GLASS	8192	N/A	50	65	10	16
28	PLCC	EPOXY	0.45″×0.45″	EPOXY	7134	28,900	65	68	N/A (6)	N/A (6)

NOTES:
1. All plastic packages use copper lead frames – ceramic packages use alloy 42 frames.
2. Body style DIL is "Dual–In–Line."
3. Standard Mounting Methods:
   a. Dual–In–Line In Socket or P/C board with no contact between bottom of package and socket or P/C board.
   b. PLCC packages solder attached to traces on 2.24″ × 2.24″ × 0.062″ FR4 type glass epoxy board with 1 oz./S.F. copper (solder coated) mounted to tester with 3 leads of 24 gauge copper wire.
4. Case Outline 649
5. Case Outline 623
6. $\theta_{JC} = \theta_{JA} - \left(\frac{T_C - T_A}{P_D}\right)$

   T_C = Case Temperature (determined by thermocouple)

For applications where the case is held at essentially a fixed temperature by mounting on a large or temperature–controlled heatsink, the estimated junction temperature is calculated by:

$$T_J = T_C + P_D (\bar{\theta}_{JC}) \quad (3)$$

where T_C = maximum case temperature and the other parameters are as previously defined.

The maximum and average thermal resistance values for standard MECL IC packages are given in Table 8. In , this basic data is converted into graphs showing the maximum power dissipation allowable at various ambient temperatures (still air) for circuits mounted in the different packages, taking into account the maximum permissible operating junction temperature for long term life ($\geq$ 100,000 hours for ceramic packages).

AIR FLOW

The effect of air flow over the packages on $\bar{\theta}_{JA}$ (due to a decrease in $\bar{\theta}_{CA}$) is illustrated in the graphs of Figure 20 through Figure 22. This air flow reduces the thermal resistance of the package, therefore permitting a corresponding increase in power dissipation without exceeding the maximum permissible operating junction temperature.

As an example of the use of the information above, the maximum junction temperature for a 16 lead ceramic dual–in–line packaged MECL 10K quad OR/NOR gate (MC10101L) loaded with four 50 ohm loads can be calculated. Maximum total power dissipation (including 4 output loads) for this quad gate is 195 mW. Assume for this thermal study that air flow is 500 linear feet per minute. From Figure 23, $\bar{\theta}_{JA}$ is 50°C/W. With T_A (air flow temperature at the device) equal to 25°C, the following maximum junction temperature results:

$$T_J = P_D (\bar{\theta}_{JA}) + T_A$$

$$T_J = (0.195\ W)\ (50°C/W) + 25°C = 34.8°C$$

Under the above operating conditions, the MECL 10K quad gate has its junction elevated above ambient temperature by only 9.8°C.

Even though different device types mounted on a printed circuit board may each have different power dissipations, all will have the same input and output levels provided that each is subject to identical air flow and the same ambient air temperature. This eases design, since the only change in levels between devices is due to the increase in ambient temperatures as the air passes over the devices, or differences in ambient temperature between two devices.

Figure 20 – AMBIENT TEMPERATURE DERATING CURVES (Ceramic Dual–In–Line Pkg)

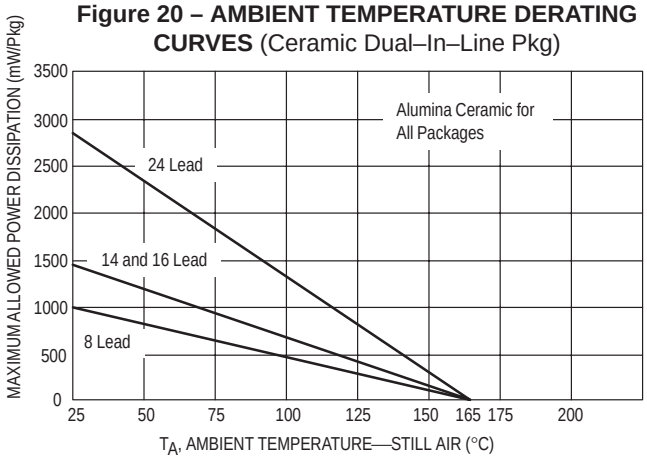


Figure 21 – AMBIENT TEMPERATURE DERATING CURVES (Plastic Dual–In–Line Pkg)

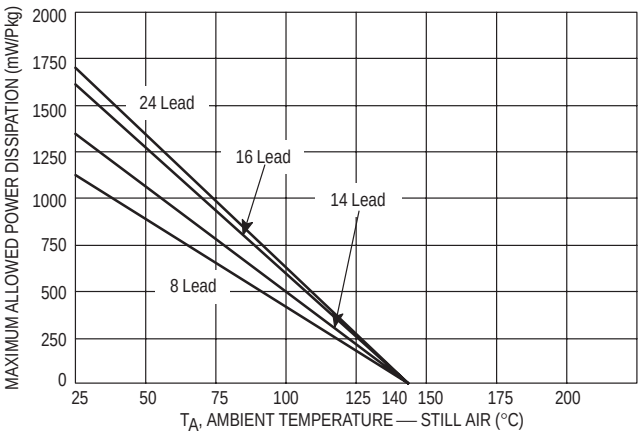


Figure 22 – AMBIENT TEMPERATURE DERATING CURVES (PLCC Pkg)

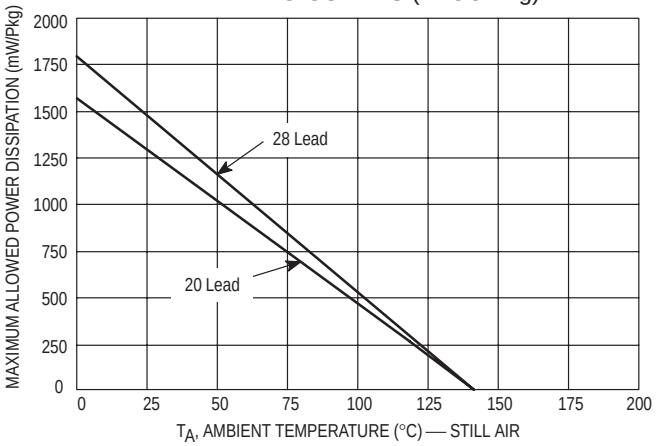


Figure 23 – AIRFLOW versus THERMAL RESISTANCE
(Ceramic Dual–In–Line Pkg)

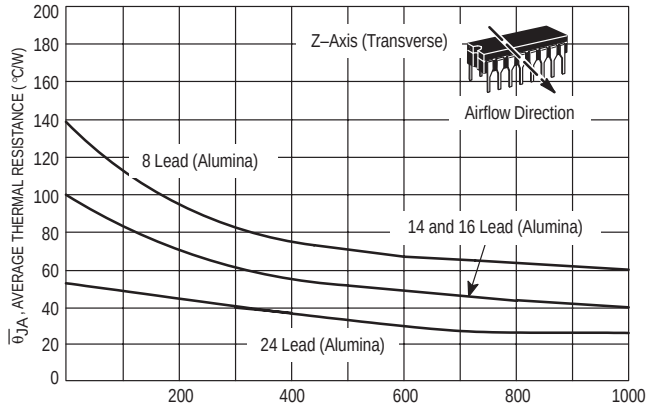


Figure 24 – AIRFLOW versus THERMAL RESISTANCE (Plastic Dual–In–Line Pkg)

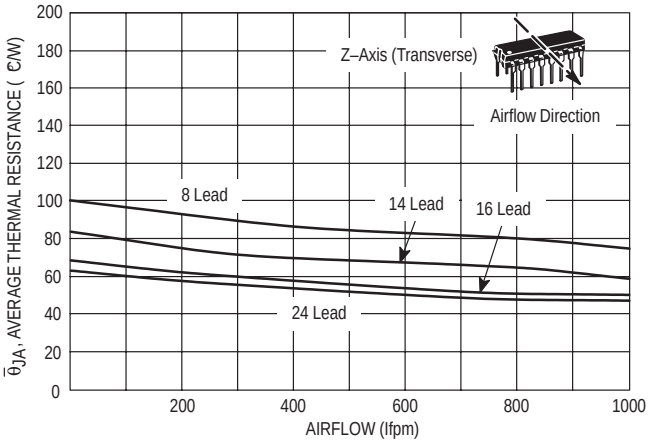


Figure 25 – AIRFLOW versus THERMAL RESISTANCE
(PLCC Pkg)

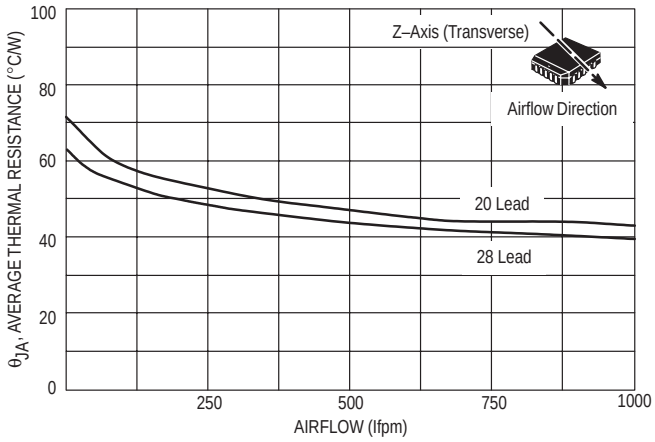


Table 9 – THERMAL GRADIENT OF JUNCTION TEMPERATURE (16–Pin MECL Dual–In–Line Package)

Power Dissipation (mW)	Junction Temperature Gradient (°C/Package)
200	0.4
250	0.5
300	0.63
400	0.88

Devices mounted on 0.062″ PC board with Z axis spacing 0.5″. Air flow is 500 lfpm along the Z axis.

The majority of MECL 10H, MECL 10K, and MECL III users employ some form of air–flow cooling. As air passes over each device on a printed circuit board, it absorbs heat from each package. This heat gradient from the first package to the last package is a function of the air flow rate and individual package dissipations. Table 9 provides gradient data at power levels of 200 mW, 250 mW, 300 mW, and 400 mW with an air flow rate of 500 lfpm. These figures show the proportionate increase in the junction temperature of each dual–in–line package as the air passes over each device. For higher rates of air flow the change in junction temperature from package to package down the airstream will be lower due to greater cooling.

OPTIMIZING THE LONG TERM RELIABILITY OF PLASTIC PACKAGES

Todays plastic integrated circuit packages are as reliable as ceramic packages under most environmental conditions. However when the ultimate in system reliability is required, thermal management must be considered as a prime system design goal.

Modern plastic package assembly technology utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. When exposed to high temperatures for protracted periods of time an intermetallic compound can form in the bond area resulting in high impedance contacts and degradation of device performance. Since the formation of intermetallic compounds is directly related to device junction temperature, it is incumbent on the designer to determine that the device junction temperatures are consistent with system reliability goals.

Predicting Bond Failure Time:

Based on the results of almost ten (10) years of +125°C operating life testing, a special arrhenius equation has been developed to show the relationship between junction temperature and reliability.

$$(1)\ T = (6.376 \times 10^{-9})\ e^{\left[\frac{11554.267}{273.15 + T_J}\right]}$$

Where: T = Time in hours to 0.1% bond failure (1 failure per 1,000 bonds).

T_J = Device junction temperature, °C.

And:

$$(2)\ T_J = T_A + P_D\theta_{JA} = T_A + \Delta T_J$$

Where: T_J = Device junction temperature, °C.

T_A = Ambient temperature, °C.

P_D = Device power dissipation in watts.

θ_{JA} = Device thermal resistance, junction to air, °C/Watt.

ΔT_J = Increase in junction temperature due to on–chip power dissipation.

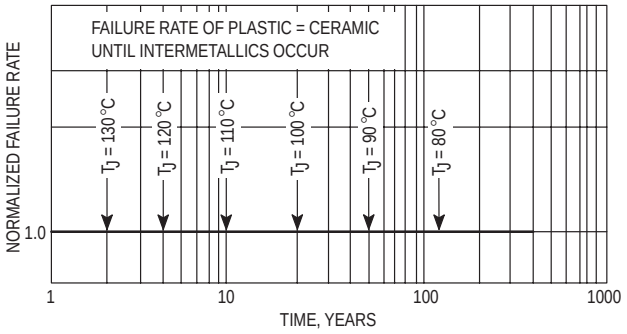
Table 10 shows the relationship between junction temperature, and continuous operating time to 0.1% bond failure, (1 failure per 1,000 bonds).

Table 10 – DEVICE JUNCTION TEMPERATURE versus TIME TO 0.1% BOND FAILURES

Junction Temp °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Table 10 is graphically illustrated in Figure 26 which shows that the reliability for plastic and ceramic devices are the same until elevated junction temperatures induces intermetallic failures in plastic devices. Early and mid–life failure rates of plastic devices are not effected by this intermetallic mechanism.

Figure 26. FAILURE RATE versus TIME JUNCTION TEMPERATURE



MECL Junction Temperatures:

Power levels have been calculated for a number of MECL 10K and MECL 10H devices in 20 pin plastic leaded chip carriers and translated to the resulting increase of junction temperature (ΔT_J) for still air and moving air at 500 LFPM using equation 2 and are shown in Table 11.

Table 11 – INCREASE IN JUNCTION TEMPERATURE DUE TO I/C POWER DISSIPATION. 20 PIN PLASTIC LEADED CHIP CARRIER

MECL 10K Device Type	ΔT_J, °C Still Air	ΔT_J, °C 500 LFPM Air	MECL 10H Device Type	ΔT_J, °C Still Air	ΔT_J, °C 500 LFPM Air
MC10101	21.8	14.1	MC10H016	48.0	30.0
MC10102	17.6	11.4	MC10H100	16.6	10.8
MC10103	17.6	11.4	MC10H101	22.1	14.5
MC10104	20.8	13.4	MC10H102	18.0	11.8
MC10105	17.2	11.2	MC10H103	18.0	11.8
MC10106	13.0	8.4	MC10H104	21.0	13.5
MC10107	19.8	12.8	MC10H105	17.8	11.7
MC10109	11.7	7.7	MC10H106	13.2	8.7
MC10110	24.7	16.1	MC10H107	20.0	12.9
MC10111	24.7	16.1	MC10H109	11.9	7.8
MC10113	22.2	14.3	MC10H113	22.8	14.8
MC10114	22.6	14.6	MC10H115	16.7	10.9
MC10115	16.7	10.9	MC10H116	17.8	11.7
MC10116	17.2	11.1	MC10H117	16.7	11.0
MC10117	16.2	10.5	MC10H121	13.9	9.1
MC10121	13.5	8.5	MC10H123	23.1	15.0
MC10123	37.6	24.0	MC10H124	44.2	28.4
MC10124	42.9	27.3	MC10H125	–	–
MC10125	–	–	MC10H130	28.2	18.2
MC10131	26.9	17.1	MC10H135	33.2	21.4
MC10133	34.4	21.9	MC10H136	61.7	38.5
MC10134	27.0	17.2	MC10H141	44.3	28.0
MC10135	31.9	20.3	MC10H158	25.3	16.4
MC10136	52.3	32.6	MC10H159	27.3	17.7
MC10138	37.0	23.2	MC10H160	32.1	20.5
MC10141	42.7	26.7	MC10H161	41.5	26.7
MC10153	34.4	21.9	MC10H162	41.5	26.7
MC10158	23.9	15.2	MC10H164	31.9	20.6
MC10159	25.8	16.4	MC10H165	56.3	35.8
MC10160	32.0	20.4	MC10H166	44.4	28.3
MC10161	40.7	26.0	MC10H171	41.9	26.9
MC10162	40.7	26.0	MC10H172	41.9	26.9
MC10164	31.3	20.1	MC10H173	32.6	21.1
MC10165	53.7	33.6	MC10H174	32.5	21.0
MC10166	43.5	27.6	MC10H175	45.9	29.6
MC10168	34.4	21.9	MC10H176	50.9	32.3
MC10170	29.9	18.9	MC10H179	35.0	22.6
MC10171	41.1	26.2	MC10H180	42.4	27.2
MC10172	41.1	26.2	MC10H181[4]	64.4	38.6
MC10173	30.5	19.3	MC10H186	50.2	31.8
MC10174	31.9	20.5	MC10H188	25.8	16.7
MC10175	43.7	27.6	MC10H189	25.8	16.7
MC10176	49.6	31.3	MC10H209	18.9	12.5
MC10178	38.1	23.9	MC10H210	25.0	16.4
MC10186	49.6	31.1	MC10H211	25.0	16.4
MC10188	25.4	16.4	MC10H330[4]	65.8	36.1
MC10189	24.6	15.9	MC10H332	52.2	33.5
MC10192	67.0	43.0	MC10H334	77.8	49.3
MC10195	46.7	29.9	MC10H350	–	–
MC10197	27.7	17.7	MC10H351	27.2	18.1
MC10198	21.2	13.4	MC10H352	27.2	18.1
MC10210	24.5	16.0	MC10H424	37.7	24.3
MC10211	24.6	16.0			
MC10212	24.3	15.8			
MC10216	24.1	15.6			
MC10231	30.6	19.5			

NOTES:

(1) All ECL outputs are loaded with a 50 Ω resistor and assumed operating at 50% duty cycle.

(2) ΔT_J for ECL to TTL translators are excluded since the supply current to the TTL section is dependent on frequency, duty cycle and loading.

(3) Thermal Resistance (θ_{JA}) measured with PLCC packages solder attached to traces on 2.24″ x 2.24″ x 0.062″ FR4 type glass epoxy board with 1 oz./sq. ft. copper (solder–coated) mounted to tester with 3 leads of 24 gauge copper wire.

(4) 28 lead PLCC.

Case Example:

After the desired system failure rate has been established for failure mechanisms other than intermetallics, each plastic device in the system should be evaluated for maximum junction temperature using Table 11. Knowing the maximum junction temperature refer to Table 10 or Equation 1 to determine the continuous operating time required to 0.1% bond failures due to intermetallic formation. At this time, system reliability departs from the desired value as indicated in Figure 26.

To illustrate, assume that system ambient air temperature is 55°C (an accepted industry standard for evaluating system failure rates). Reference is made to Table 11 to determine the maximum junction temperature for each device for still air and transverse air flow of 500 LFPM.

Adding the 55°C ambient to the highest, ΔT_J listed, 77.8°C (for the MC10H334 with no air flow), gives a maximum junction temperature of 132.8°C. Reference to Table 10 indicates a departure from the desired failure rate after about 2 years of constant exposure to this junction temperature. If 500 LFPM of air flow is utilized, maximum junction temperature for this device is reduced to 104.3°C for which Table 10 indicates an increased failure rate in about 15 years.

Air flow is one method of thermal management which should be considered for system longevity. Other commonly used methods include heat sinks for higher powered devices, refrigerated air flow and lower density board stuffing.

The material presented here emphasizes the need to consider thermal management as an integral part of system design and also the tools to determine if the management methods being considered are adequate to produce the desired system reliability.

THERMAL EFFECTS ON NOISE MARGIN

The data sheet dc specifications for standard MECL 10K and MECL III devices are given for an operating temperature range from –30°C to +85°C (0° to +75°C for MECL 10H and memories). These values are based on having an airflow of 500 lfpm over socket or P/C board mounted packages with no special heatsinking (i.e., dual–in–line package mounted on lead seating plane with no contact between bottom of package and socket or P/C board and flat package mounted with bottom in direct contact with non–metalized area of P/C board).

The designer may want to use MECL devices under conditions other than those given above. The majority of the low–power device types may be used without air and with higher $\overline{\theta}_{JA}$. However, the designer must bear in mind that junction temperatures will be higher for higher $\overline{\theta}_{JA}$, even though the ambient temperature is the same. Higher junction temperatures will cause logic levels to shift.

As an example, a 300 mW 16 lead dual–in–line ceramic device operated at $\overline{\theta}_{JA}$ = 100°C/W (in still air) shows a HIGH logic level shift of about 21 mV above the HIGH logic level when operated with 500 lfpm air flow and a $\overline{\theta}_{JA}$ = 50°C/W. (Level shift = $\Delta T_J \times 1.4$ mV/°C).

If logic levels of individual devices shift by different amounts (depending on P_D and θ_{JA}), noise margins are somewhat reduced. Therefore, the system designer must lay out his system bearing in mind that the mounting procedures to be used should minimize thermal effects on noise margin.

The following sections on package mounting and heatsinking are intended to provide the designer with sufficient information to insure good noise margins and high reliability in MECL system use.

MOUNTING AND HEATSINK SUGGESTIONS

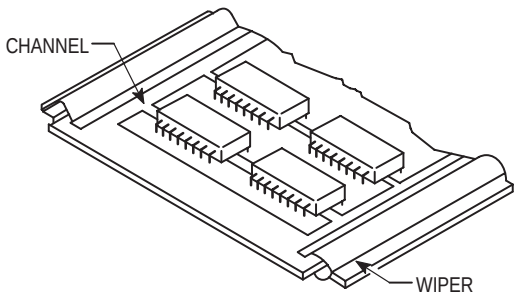
With large high–speed logic systems, the use of multilayer printed circuit boards is recommended to provide both a better ground plane and a good thermal path for heat dissipation. Also, a multilayer board allows the use of microstrip line techniques to provide transmission line interconnections.

Two–sided printed circuit boards may be used where board dimensions and package count are small. If possible, the V_{CC} ground plane should face the bottom of the package to form the thermal conduction plane. If signal lines must be placed on both sides of the board, the V_{EE} plane may be used as the thermal plane, and at the same time may be used as a pseudo ground plane. The pseudo ground plane becomes the ac ground reference under the signal lines placed on the same side as the V_{CC} ground plane (now on the opposite side of the board from the packages), thus maintaining a microstrip signal line environment.

Two–ounce copper P/C board is recommended for thermal conduction and mechanical strength. Also, mounting holes for low power devices may be countersunk to allow the package bottom to contact the heat plane. This technique used along with thermal paste will provide good thermal conduction.

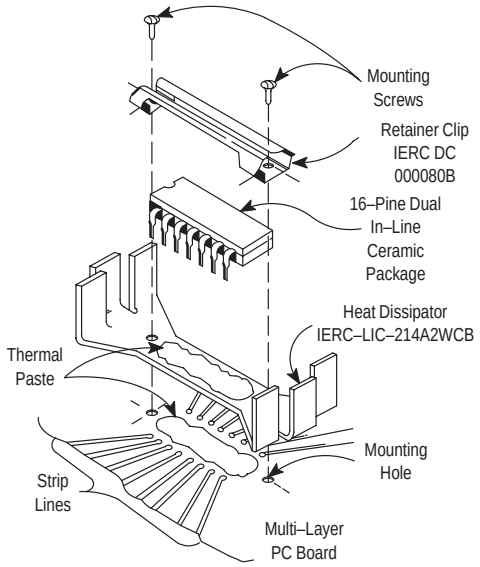
Printed channeling is a useful technique for conduction of heat away from the packages when the devices are soldered into a printed circuit board. As illustrated in Figure 27, this heat dissipation method could also serve as V_{EE} voltage distribution or as a ground bus. The channels should terminate into channel strips at each side or the rear of a plug–in type printed circuit board. The heat can then be removed from the circuit board, or board slide rack, by means of wipers that come into thermal contact with the edge channels.

Figure 27 – CHANNEL/WIPER HEATSINKING ON DOUBLE LAYER BOARD



For operating some of the higher power device types* in 16 lead dual–in–line packages in still air, requiring $\overline{\theta}_{JA}$ <100°C/W, a suitable heatsink is the IERC LIC–214A2WCB shown in Figure 28. This sink reduces the still air $\overline{\theta}_{JA}$ to around 55°C/W. By mounting this heatsink directly on a copper ground plane (using silicone paste) and passing 500 lfpm air over the packages, $\overline{\theta}_{JA}$ is reduced to approximately 35°C/W, permitting use at higher ambient temperatures than +85°C (+75°C for MECL 10H memories) or in lowering T_J for improved reliability.

Figure 28 – MECL HIGH–POWER DUAL–IN–LINE PACKAGE MOUNTING METHOD



It should be noted that the use of a heatsink on the top surface of the dual–in–line package is not very effective in lowering the $\overline{\theta}_{JA}$. This is due to the location of the die near the bottom surface of the package. Also, very little (< 10%) of the internal heat is withdrawn through the package leads due to the isolation from the ceramic by the solder glass seals and the limited heat conduction from the die through 1.0 to 1.5 mil aluminum bonding wires.

INTERFACING MECL TO SLOWER LOGIC TYPES

MECL circuits are interfaceable with most other logic forms. For MECL/TTL/DTL interfaces, when MECL is operated at the recommended –5.2 volts and TTL/DTL at +5.0 V supply, currently available translator circuits, such as the MC10124 and MC10125, may be used.

For systems where a dual supply (–5.2 V and +5 V) is not practical, the MC10H350 includes four single supply MECL to TTL translators, or a discrete component translator can be designed. For details, see MECL System Design Handbook (HB205/D). Such circuits can easily be made fast enough for any available TTL.

MECL also interfaces readily with MOS. With CMOS operating at +5 V, any of the MECL to TTL translators works very well.

Specific circuitry for use in interfacing MECL families to other logic types is given in detail in the MECL System Design Handbook.

Complex MECL 10K devices are presently available for interfacing MECL with MOS logic, MOS memories, TTL three–state circuits, and IBM bus logic levels. See Application Note AN720/D for additional interfacing information.

CIRCUIT INTERCONNECTIONS

Though not necessarily essential, the use of multilayer printed circuit boards offers a number of advantages in the development of high–speed logic cards. Not only do multilayer boards achieve a much higher package density, interconnecting leads are kept shorter, thus minimizing propagation delay between packages. This is particularly beneficial with MECL III which has relatively fast (1 ns) rise and fall times. Moreover, the unbroken ground planes made possible with multilayer boards permit much more precise control of transmission line impedances when these are used for interconnecting purposes. Thus multilayer boards are recommended for MECL III layouts and are justified when operating MECL 10H and MECL 10K at top circuit speed, when high–density package is a requirement, or when transmission line interconnects are used.

Point–to–point back–plane wiring without matched line terminations may be employed for MECL interconnections if line runs are kept short. At MECL 10K speeds, this applies to line runs up to 6 inches, for MECL 10H and MECL III up to 1 inch (Maximum open wire lengths for less than 100 mV undershoot). But, because of the open–emitter outputs of MECL 10H, MECL 10K and MECL III circuits, pull–down resistors are always required. Several ways of connecting such pull–down resistors are shown in Figure 29 through Figure 31.

Resistor values for the connection in Figure 29 may range from 270 ohms to kΩ depending on power and load requirements. (See MECL System Design Handbook.) Power may be saved by connecting pull–down resistors in the range of 50 ohms to 150 ohms, to –2.0 Vdc, as shown in Figure 30. Use of a series damping resistor, Figure 31, will extend permissible lengths of unmatched–impedance interconnec– tions, with some loss of edge speed.

With proper choice of the series damping resistor, line lengths can be extended to any length,** while limiting overshoot and undershoot to a predetermined amount. Damping resistors usually range in value from 10 ohms to 100 ohms, depending on the line length, fanout, and line impedance, the open emitter–follower outputs of MECL 10H, MECL III and MECL 10K give the system designer all possible line driving options.

* 10136 and 10H136 Max P_D > 800 mW.

** Limited only by line attenuation and band–width characteristics.

One major advantage of MECL over saturated logic is its capability for driving matched–impedance transmission lines. Use of transmission lines retains signal integrity over long distances. The MECL 10H and MECL 10K emitter–follower output transistors will drive a 50–ohm transmission line terminated to –2.0 Vdc. This is the equivalent current load of 22 mA in the HIGH logic state and 6 mA in the LOW state.

Parallel termination of transmission lines can be done in two ways. One, as shown in Figure 32, uses a single resistor whose value is equal to the impedance (Z_o) of the line. A terminating voltage (V_{TT}) of –2.0 Vdc must be supplied to the terminating resistor.

Another method of parallel termination uses a pair of resistors, R1 and R2. Figure 33 illustrates this method. The following two equations are used to calculate the values of R1 and R2:

$$R1 = 1.6\ Z_o$$
$$R2 = 2.6\ Z_o$$

Another popular approach is the series–terminated transmission line (see Figure 32 and Figure 33). This differs from parallel termination in that only one–half the logic swing is propagated through the lines. The logic swing doubles at the end of the transmission line due to reflection on an open line, again establishing a full logic swing.

PULL–DOWN RESISTOR TECHNIQUES

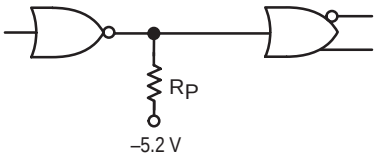


Figure 29

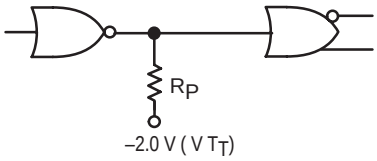


Figure 30

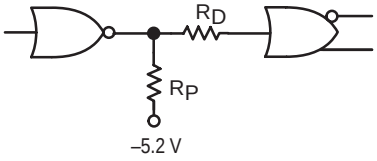


Figure 31

To maintain clean wave fronts, the input impedance of the driven gate must be much greater than the characteristic impedance of the transmission line. This condition is satisfied by MECL circuits which have high impedance inputs. Using the appropriate terminating resistor (R_S) at point A (Figure 34), the reflections in the transmission line will be terminated.

Figure 32 – PARALLEL TERMINATED LINE

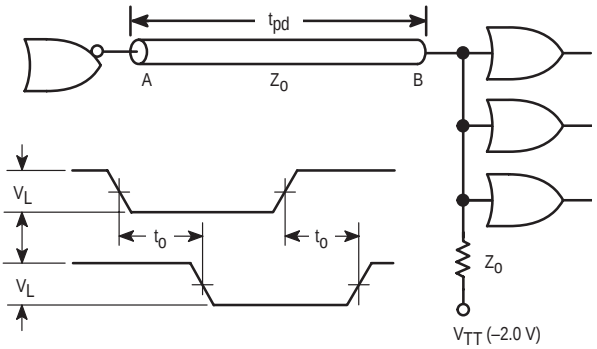


Figure 33 – PARALLEL TERMINATION – THEVENIN EQUIVALENT

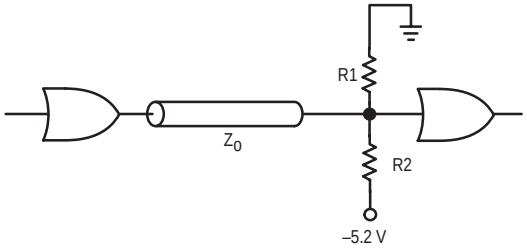
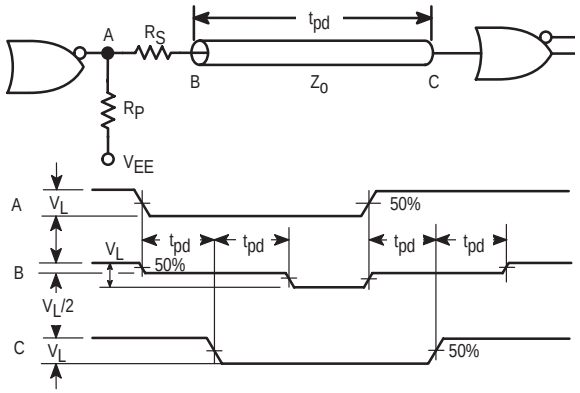


Figure 34 – SERIES TERMINATED LINE



The advantages of series termination include ease of driving multiple series–terminated lines, low power consumption, and low cross talk between adjacent lines. The disadvantage of this system is that loads may not be distributed along the transmission line due to the one–half logic swing present at intermediate points.

For board–to–board interconnections, coaxial cable may be used for signal conductors. The termination techniques just discussed also apply when using coax. Coaxial cable has

the advantages of good noise immunity and low attenuation at high frequencies.

Twisted pair lines are one of the most popular methods of interconnecting cards or panels. The complementary outputs of any MECL function may be connected to one end of the twisted pair line, and any MECL differential line receiver to the other as shown in the example, Figure 35. R_T is used to terminate the twisted pair line. The 1 to 1.5 V common–mode noise rejection of the line receiver ignores common–mode cross talk, permitting multiple twisted pair lines to be tied into cables. MECL signals may be sent very long distances (> 1000 feet) on twisted pair, although line attenuation will limit bandwidth, degrading edge speeds when long line runs are made.

If timing is critical, parallel signals paths (shown in Figure 36) should be used when fanout to several cards is required. This will eliminate distortion caused by long stub lengths off a signal path.

Wire–wrapped connections can be used with MECL 10K. For MECL III and MECL 10H, the fast edge speeds (1 ns) create a mismatch at the wire–wrap connections which can cause reflections, thus reducing noise immunity. The mismatch occurs also with MECL 10K, but the distance between the wire–wrap connections and the end of the line is generally short enough so the reflections cause no problem.

Series damping resistors may be used with wire–wrapped lines to extend permissible backplane wiring lengths. Twisted pair lines may be used for even longer distances across large wire–wrapped cards. The twisted pair gives a more defined characteristic impedance (than a single wire), and can be connected either single–ended, or differentially using a line receiver.

The recommended wire–wrapped circuit cards have a ground plane on one side and a voltage plane on the other side to insure a good ground and a stable voltage source for the circuits. In addition, the ground plane near the wire–wrapped lines lowers the impedance of those lines and facilitates terminating the line. Finally, the ground plane serves to minimize cross talk between parallel paths in the signal lines. Point–to–point wire routing is recommended because cross talk will be minimized and line lengths will be shortest. Commercial wire–wrap boards designed for MECL 10K are available from several vendors.

Figure 35 – TWISTED PAIR LINE DRIVER/RECEIVER

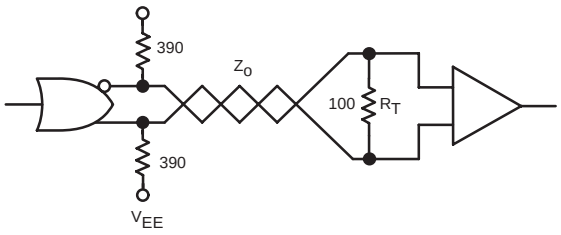
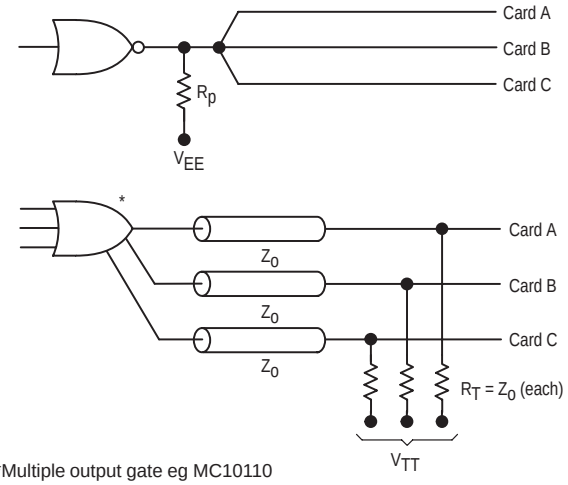


Figure 36 – PARALLEL FANOUT TECHNIQUES

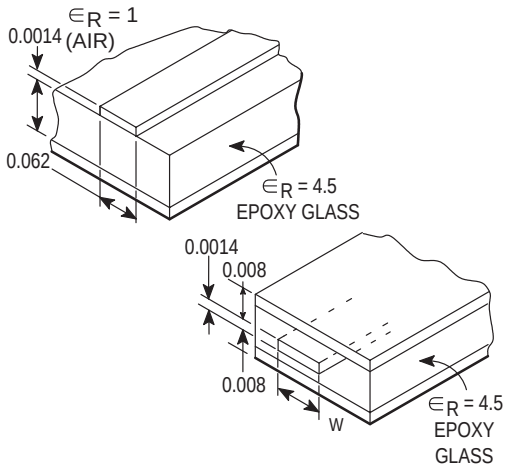


*Multiple output gate eg MC10110

Microstrip and Stripline

Microstrip and stripline techniques are used with printed circuit boards to form transmission lines. Microstrip consists of a constant–width conductor on one side of a circuit board, with a ground plane on the other side (shown in Figure 37). The characteristic impedance is determined by the width and thickness of the conductor, the thickness of the circuit board, and the dielectric constant of the circuit board material.

Figure 37 – PC INTERCONNECTION LINES FOR USE WITH MECL



Stripline is used with multilayer circuit boards as shown in Figure 37. Stripline consists of a constant–width conductor between two ground planes.

Refer to MECL System Design Handbook for a full discussion of the properties and use of these.

CLOCK DISTRIBUTION

Clock distribution can be a system problem. At MECL 10K speeds, either coaxial cable or twisted pair line (using

the MC10101 and MC10115) can be used to distribute clock signals throughout a system. Clock line lengths should be controlled and matched when timing could be critical. Once the clocking signals arrive on card, a tree distribution should be used for large–fanouts at high frequency. An example of the application of the technique is shown in Figure 38.

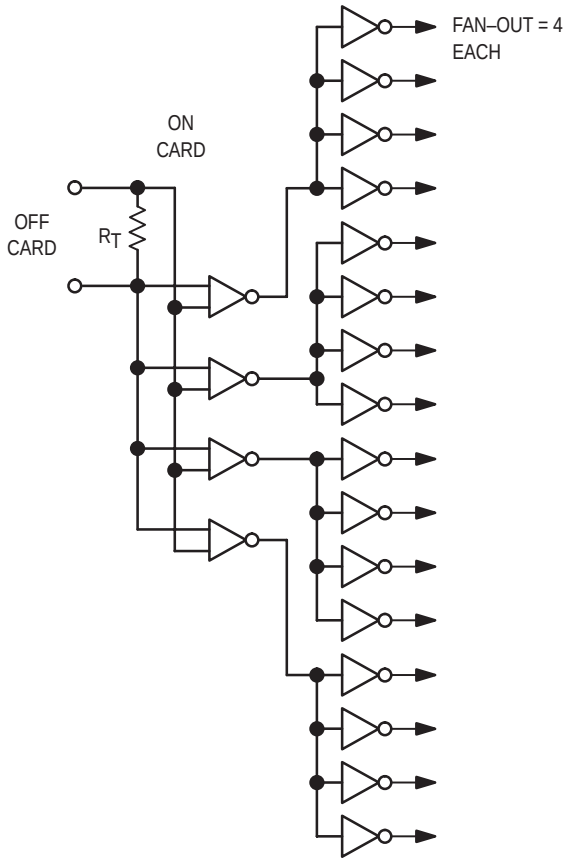
Because of the very high clock rates encountered in MECL III systems, rules for clocking are more rigorous than in slower systems.

The following guidelines should be followed for best results:

A. On–card Synchronous Clock Distribution via Transmission Line

1. Use the NOR output in developing clock chains or trees. Do not mix OR and NOR outputs in the chain.
2. Use balanced fanouts on the clock drivers.
3. Overshoot can be reduced by using two parallel drive lines in place of one drive line with twice the lumped load.

Figure 38 – 64 FANOUT CLOCK DISTRIBUTION (PROPER TERMINATION REQUIRED)



4. To minimize clock skewing problems on synchronous sections of the system, line delays should be matched to within 1 ns.
5. Parallel drive gates should be used when clocking repetition rates are high, or when high capacitance loads occur. The bandwidth of a MECL III gate may be extended by paralleling both halves of a dual gate. Approximately 40 or 50 MHz bandwidth can be gained by paralleling two or three clock driver gates.
6. Fanout limits should be applied to clock distribution drivers. Four to six loads should be the maximum load per driver for best high speed performance. Avoid large lumped loads at the end of lines greater than 3 inches. A lumped load, if used, should be four or fewer loads.
7. For wire–OR (emitter dotting), two–way lines (busses) are recommended. To produce such lines, both ends of a transmission line are terminated with 100–ohm impedance. This method should be used when wire–OR connections exceed 1 inch apart on a drive line.

B. Off–Card Clock Distribution

1. The OR/NOR outputs of an MC1660 may be used to drive into twisted pair lines or into flat, fixed–impedance ribbon cable. At the far end of the twisted pair on MC1692 differential line receiver is used. The line should be terminated as shown in Figure 35. This method not only provides high speed, board–to–board clock distribution, but also provides system noise margin advantages. Since the line receiver operates independently of the V_{BB} reference voltage (differential inputs) the noise margin from board to board is also independent of temperature differentials.

LOGIC SHORTCUTS

MECL circuitry offers several logic design conveniences. Among these are:

1. **Wire–OR** (can be produced by wiring MECL output emitters together outside packages).
2. **Complementary Logic Outputs** (both OR and NOR are brought out to package pins in most cases).

An example of the use of these two features to reduce gate and package count is shown in Figure 39.

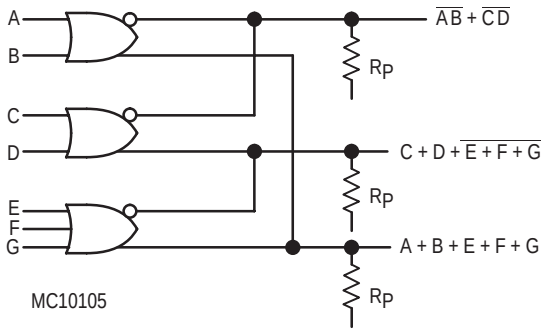
The connection shown saves several gate circuits over performing the same functions with non–ECL type logic. Also, the logic functions in Figure 39 are all accomplished with one gate propagation delay time for best system speed. Wire–ORing permits direct connections of MECL circuits to busses. (MECL System Design Handbook and Application Note AN726/D).

Propagation delay is increased approximately 50 ps per wire–OR connection. In general, wire–OR should be limited to 6 MECL outputs to maintain a proper LOW logic level. The MC10123 is an exception to this rule because it has a special V_{OL} level that allows very high fanout on a bus or wire–OR line. The use of a single output pull–down resistor is recommended per wire–OR, to economize on power

dissipation. However, two pull–down resistors per wired–OR can improve fall times and be used for double termination of busses.

Wire–OR should be done between gates in a package or nearby packages to avoid spikes due to line propagation delay. This does not apply to bus lines which activate only one driver at a time.

Figure 39 – USE OF WIRE–OR AND COMPLEMENTARY OUTPUTS



SYSTEM CONSIDERATIONS – A SUMMARY OF RECOMMENDATIONS

	MECL 10H	MECL 10K
Power Supply Regulation	±5% (1)	10% (2)
On–Card Temperature Gradient	20°C	Less Than 25°C
Maximum Non–Transmission Line Length (No Damping Resistor)	1″	8″
Unused Inputs	Leave Open (3)	Leave Open (3)
PC Board	Multilayer	Standard 2–Sided or Multilayer
Cooling Requirements	500 lfpm Air	500 lfpm Air
Bus Connection Capability	Yes (Wire–OR)	Yes (Wire–OR)
Maximum Twisted Pair Length (Differential Drive)	Limited By Cable Response Only, Usually >1000′	Limited by Cable Response Only, Usually >1000′
The Ground Plane to Occupy Percent Area of Card	>75%	>50%
Wire Wrap may be used	Not Recommended	Yes
Compatible with MECL 10,000	Yes	–

(1) All dc and ac parameters guaranteed for V_{EE} = –5.2 V ± 5%.
(2) At the devices (functional only).
(3) Except special functions without input pull–down resistors.

APPLICATIONS ASSISTANCE FORM

In the event that you have any questions or concerns about the performance of any ON Semiconductor device listed in this catalog, please contact your local ON Semiconductor sales office or the ON Semiconductor Help line for assistance. If further information is required, you can request direct factory assistance.

Please fill out as much of the form as is possible if you are contacting ON Semiconductor for assistance or are sending devices back to ON Semiconductor for analysis. Your information can greatly improve the accuracy of analysis and can dramatically improve the correlation response and resolution time.

Items 4 thru 8 of the following form contain important questions that can be invaluable in analyzing application or device problems. It can be used as a self–help diagnostic guideline or for a baseline of information gathering to begin a dialog with ON Semiconductor representatives.

ON Semiconductor Device Correlation/Component Analysis Request Form

–Please fill out entire form and return with devices to ON Semiconductor, R&QA DEPT., 5005 E. McDowell Rd., Phx, AZ 85008.

1) Name of Person Requesting Correlation: _____

   Phone No: _____ Job Title: _____ Company: _____

2) Alternate Contact: _____ Phone/Position: _____

3) Device Type (user part number): _____

4) Industry Generic Device Type: _____

5) # of devices tested/sampled: _____

   # of devices in question*: _____

   # returned for correlation: _____

   * In the event of 100% failure, does Customer have other date codes of ON Semiconductor devices that pass inspection?

     Yes _____ No _____ Please specify passing date code(s) if applicable _____

   If none, does customer have viable alternate vendor(s) for device type?

     Yes _____ No _____ Alternate vendor's name _____

6) Date code(s) and Serial Number(s) of devices returned for correlation – If possible, please provide one or two "good" units (ON Semiconductor's and/or other vendor) for comparison: _____

   _____

7) Describe USER process that device(s) are questionable in:

   _____ Incoming component inspection {test system = ?}: _____

   _____ Design prototyping: _____

   _____ Board test/burn–in: _____

   _____ Other (please describe): _____

   _____

8) Please describe the device correlation operating parameters as completely as possible for device(s) in question:

> Describe all pin conditions (e.g. floating, high, low, under test, stimulated but not under test, whatever ...), including any input or output loading conditions (resistors, caps, clamps, driving devices or devices being driven ...). Potentially critical information includes:

   _____ Input waveform timing relationships

   _____ Input edge rates

   _____ Input Overshoot or Undershoot – Magnitude and Duration

   _____ Output Overshoot or Undershoot – Magnitude and Duration

> Photographs, plots or sketches of relevant inputs and outputs with voltages and time divisions clearly identified for all waveforms are greatly desirable.

> V_{CC} and Ground waveforms should be carefully described as these characteristics vary greatly between applications and test systems. Dynamic characteristics of Ground and V_{CC} during device switching can dramatically effect input and internal operating levels. Ground & V_{CC} measurements should be made as physically close to the device in question as possible.

> Are there specific circumstances that seem to make the questionable unit(s) worse? Better?

   _____ Temperature _____

   _____ V_{CC} _____

   _____ Input rise/fall time _____

   _____ Output loading (current/capacitance) _____

   _____ Others _____

> ATE functional data should include pattern with decoding key and critical parameters such as V_{CC}, input voltages, Func step rate, voltage expected, time to measure.

CHAPTER 2
MECL 10H Data Sheets

MECL 10H
INTEGRATED CIRCUITS

MC10H100 SERIES
0 TO 75°C

Function Selection – (0 to +75°C)

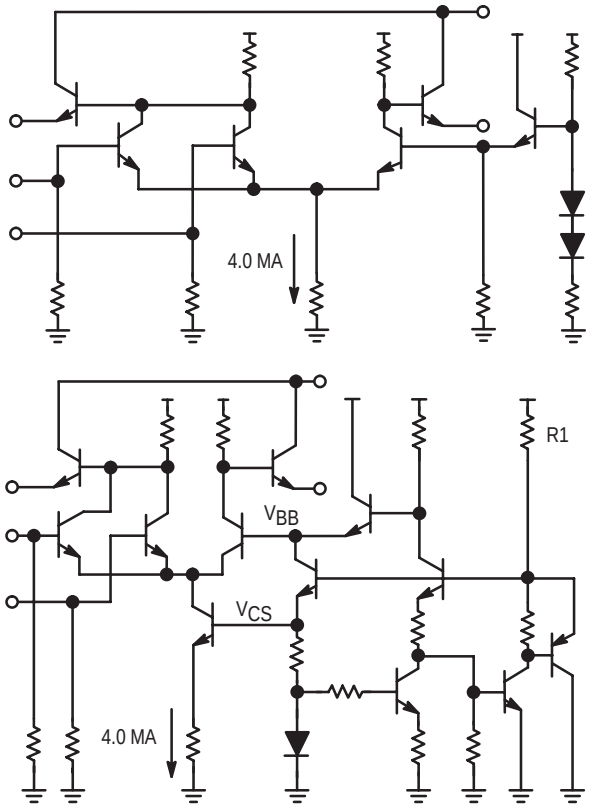
Function	Device	Case
NOR Gate		
Quad 2–Input with Strobe	MC10H100	620, 648, 775
Quad 2–Input	MC10H102	620, 648, 775
Triple 4–3–3 Input	MC10H106	620, 648, 775
Dual 3–Input 3–Output	MC10H211	620, 648, 775
OR Gate		
Quad 2–Input	MC10H103	620, 648, 775
Dual 3–Input 3–Output	MC10H210	620, 648, 775
AND Gates		
Quad AND	MC10H104	620, 648, 775
Complex Gates		
Quad OR/NOR	MC10H101	620, 648, 775
Triple 2–3–2 Input OR/NOR	MC10H105	620, 648, 775
Triple Exclusive OR/NOR	MC10H107	620, 648, 775
Dual 4–5 Input OR/NOR	MC10H109	620, 648, 775
Quad Exclusive OR	MC10H113	620, 648, 775
Dual 2–Wide OR–AND/OR–AND INVERT	MC10H117	620, 648, 775
4–Wide OR–AND/OR–AND INVERT	MC10H121	620, 648, 775
Hex Buffer w/Enable	MC10H188	620, 648, 775
Hex Inverter w/Enable	MC10H189	620, 648, 775
Translators		
Quad TTL to MECL	MC10H124	620, 648, 775
Quad MECL to TTL	MC10H125	620, 648, 775
Quad MECL–to–TTL Translator, Single Power Supply (–5.2 V or +5.0 V)	MC10H350	620, 648, 775
Quad TTL/NMOS to MECL Translator	MC10H351	732, 738, 775
Quad CMOS to MECL Translator	MC10H352	732, 738, 775
Quad TTL to MECL, ECL Strobe	MC10H424	620, 648, 775
9–Bit TTL–ECL Translator	MC10H/100H600	776
9–Bit ECL–TTL Translator	MC10H/100H601	776
9–Bit Latch/TTL–ECL Translator	MC10H/100H602	776
9–Bit Latch/ECL–TTL Translator	MC10H/100H603	776
Registered Hex TTL–ECL Translator	MC10H/100H604	776
Registered Hex ECL–TTL Translator	MC10H/100H605	776
Registered Hex TTL–PECL Translator	MC10H/100H606	776
Registered Hex PECL–TTL Translator	MC10H/100H607	776
Receivers		
Quad Line Receiver	MC10H115	620, 648, 775
Triple Line Receiver	MC10H116	620, 648, 751B, 775
Flip–Flop Latches		
Dual D Latch	MC10H130	620, 648, 775
Dual D Master Slave Flip–Flop	MC10H131	620, 648, 775
Dual J–K Master Slave Flip–Flop	MC10H135	620, 648, 775
Hex D Flip–Flop	MC10H176	620, 648, 775
Quint Latch	MC10H175	620, 648, 775
Hex D Flip–Flop w/Common Reset	MC10H186	620, 648, 775
Encoders Decoders		
Binary to 1–8 (Low)	MC10H161	620, 648, 775
Binary to 1–8 (High)	MC10H162	620, 648, 775
Dual Binary to 1–4 (Low)	MC10H171	620, 648, 775
Dual Binary to 1–4 (High)	MC10H172	620, 648, 775
8–Input Priority Encoder	MC10H165	620, 648, 775
Parity Checker		
12–Bit Parity Generator/Checker	MC10H160	620, 648, 775

Function	Device	Case
Transceivers		
4–Bit Differential ECL Bus to TTL Bus Transceiver	MC10/10H680	776
Hex ECL–TTL Transceiver w/Latches	MC10/10H681	776
Data Selector Multiplexer		
Quad Bus Driver/Receiver with 2–to–1 Output Multiplexers	MC10H330	758, 724, 776
Quad 2–Input Multiplexers (Noninverting)	MC10H158	620, 648, 775
Quad 2–Input Multiplexers (Inverting)	MC10H159	620, 648, 775
8–Line Multiplexer	MC10H164	620, 648, 775
Quad 2–Input Multiplexer Latch	MC10H173	620, 648, 775
Dual 4–1 Multiplexer	MC10H174	620, 648, 775
Counters		
Universal Hexadecimal	MC10H136	620, 648, 775
Binary Counter	MC10H016	620, 648, 775
Arithmetic Functions		
Look Ahead Carry Block	MC10H179	620, 648, 775
Dual High Speed Adder/Subtractor	MC10H180	620, 648, 775
4–Bit ALU	MC10H181	724, 758, 776
Special Function		
4–Bit Universal Shift Register	MC10H141	620, 648, 775
5–Bit Magnitude Comparator	MC10H166	620, 648, 775
Quad Bus Driver/Receiver with Transmit and Receiver Latches	MC10H334	732, 738, 775
Bus Driver (25 ohm outputs)		
Triple 4–3–3 Input Bus Driver (25 Ohms)	MC10H123	620, 648, 775
Quad Bus Driver/Receiver with 2–to–1 Output Multiplexers	MC10H330	724, 758, 776
Dual Bus Driver/Receiver with 4–to–1 Output Multiplexers	MC10H332	732, 738, 775
Quad Bus Driver/Receiver with Transmit and Receiver Latches	MC10H334	732, 738, 775
OR/NOR Gate		
Dual 4–5 Input OR/NOR Gate	MC10H209	620, 648, 775
Clock Drivers		
68030/40 ECL–TTL Clock Driver	MC10/100H640	776
Single Supply PECL–ECL 1:9 Clock Distribution	MC10/100H641	776
68030/40 ECL–TTL Clock Driver	MC10/100H642	776
Dual Supply ECT–TTL 1:8 Clock Driver	MC10/100H643	776
68030/40 PECL–TTL Clock Driver	MC10/100H644	775
1:9 TTL Clock Driver	MC10H645	776
PCL–TTL–TTL 1:8 Clock Distribution Chip	MC10/100H646	776

MECL 10H INTRODUCTION

ON Semiconductor's MECL 10H family features 100% improvement in propagation delay and clock speeds while maintaining power supply current equal to MECL 10K. This MECL family is voltage compensated which allows guaranteed dc and switching parameters over a ±5% power supply range. Noise margins of MECL 10H are 75% better than the MECL 10K series over the ±5% power supply range. MECL 10H is compatible with MECL 10K and MECL III, a key element in allowing users to enhance existing systems by increasing the speed in critical timing areas. Also, many MECL 10H devices are pinout/functional duplications of the MECL 10K series devices.

FIGURE 1 – MECL 10K versus MECL 10H GATE DESIGN



The schematics in Figure 1 compare the basic gate structure of the MECL 10H to that of MECL 10K devices. The gate switch current is established with a current source in the MECL 10H family as compared to a resistor source in MECL 10K. The bias generator in the MECL 10K device has been replaced with a voltage regulator in the MECL 10H series. The advantages of these design changes are: current–sources permit–matched collector resistors that yield correspondingly better matched delays, less variation in the output–voltage level with power supply changes, and matched output– tracking rates with temperature. These circuit changes increase complexity at the gate level; however, the added performance more than compensates.

The MECL 10H family is being fabricated using Motorola's MOSAIC I (Motorola Oxide Self Assigned Implanted Circuits). The switching transistor's geometries obtained in the MOSAIC I process show a two–fold improvement in fτ, a reduction of more than 50% in parasitic capacitance and a decrease in device area of almost 76%.

FIGURE 2 – MOSAIC versus MECL 10K SWITCHING TRANSISTOR GEOMETRY

With improved geometry, the MECL10H switching transistors (left) are one–seventh the size of the older MECL 10K transistors (right). Along with the smaller area comes an improved f_T and reduced parasitic capacitances.

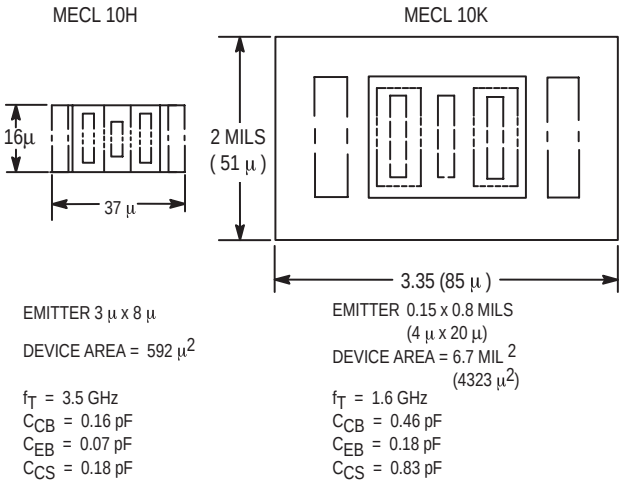


Figure 2 illustrates the relative size difference between the junction isolated transistor of MECL 10K and the MOSAIC I transistor of MECL 10H. This suggests that performance could be improved twofold at lower power levels. However, at the gate level, the power of the output transistor cannot be reduced without sacrificing output characteristics because of the 50 ohm drive requirements of MECL. In more complex functions, where part of the delay is associated with internal gates, MECL 10H devices use less power than the equivalent MECL 10K devices and provide an even more significant improvement in ac performance.

Table 1. – TYPICAL FAMILY CHARACTERISTICS FOR 10K AND 10H CIRCUITS

	10K	10H
Propagation delay (ns)	2.0	1.0
Power (mW)	25	25
Power–speed product (pJ)	50	25
Rise/fall times (ns) (20–80%)	2.0	1.0
Temperature range (°C)	–30 to +85	0 to +75
Voltage regulated	No	Yes
Technology	Junction isolated	Oxide isolated
V_{EE} = –5.2 V		

Supply & Temperature Variation

MECL 10H temperature and voltage compensation is designed to guarantee compatibility with MECL 10K, MECL III, MECL Memories and the MC10900 and Macrocell Array products. Table 1 summarizes some performance characteristics of the MECL 10K and 10H logic families in a 16–pin DIP. The MECL 10H devices offer typical propagation delays of 1.0 ns at 25 mW per gate when operated from a V_{EE} of –5.2 V. The resulting speed–power product of 25 picojoules is one of the best of any ECL logic family available today.

The operating temperature range is changed from –30°C to +85°C of the MECL 10K family to the narrower range of 0°C to 75°C for MECL 10H. This change matches the constraints established by the memory and array products. Operation at –30°C would require compromises in performance and power. With few exceptions, commercial applications are satisfied by 0°C min.

Table 2. – MECL 10H AC SPECIFICATIONS AND TRACKING

Parameter	0°C Min	0°C Typ	0°C Max	25°C Min	25°C Typ	25°C Max	75°C Min	75°C Typ	75°C Max	Units
t_{PD}	0.4	1.0	1.5	0.4	1.0	1.6	0.4	1.0	1.7	ns
	Min		Max	Min		Max	Min		Max	
t_R (20–80%)	0.5		1.5	0.5		1.6	0.5		1.7	ns
t_F (20–80%)	0.5		1.5	0.5		1.6	0.5		1.7	ns
V_{EE} = –5.2 V ±5%										

Parameter		Propagation delay (ns)* Typ	Propagation delay (ns)* Max	Delay variation vs temp (ps/°C) Typ	Delay variation vs temp (ps/°C) Max	Delay variation vs supply (ps/V) Typ	Delay variation vs supply (ps/V) Max
t_{PD}	10K	2.0	2.9	2.0	7.0	80	
	10H	1.0	1.5	0.5	4.0	0	0

*V_{EE} = –5.2 V, Temp = 25°C

AC specifications of MECL 10H products appear in Table 2. In the MECL 10H family, all ac specifications have guaranteed minimums and maximums for extremes of both temperature and supply – a first in ECL logic. In addition, flip flops, latches and counters will have guaranteed limits for setup time, hold time, and clock pulse width. The limits in Table 2 are guaranteed for a power supply variation of ±5%. MECL 10K typically has a propagation delay (t_{PD}) variation of 80 ps/V with no guaranteed maximum. The typical variation in t_{PD} for MECL 10H circuits is only 38 ps typically over the entire specified temperature range and power–supply tolerance, and is guaranteed not to exceed 300 ps.

The improved performance in temperature over MECL 10K are a result of the internal voltage regulator. The primary difference being the flatter tracking rate of the output “0” level voltage (V_{OL}). This difference does not affect the compatibility with existing MECL families.

Changes in output “1” level voltages (V_{OH}) with supply variations are 10 mV/V less for the MECL 10H family. V_{OH} varies with the supply, primarily because of changes in chip temperature caused by the changes in power dissipation. However, the current in the MECL 10H circuits remains almost constant with supply changes, since the circuits are voltage compensated and use current sources for all internal emitter followers. Threshold voltage (V_{BB}) and output “0” level voltage (V_{OL}) variations are shown with respect to MECL 10K in Table 3. In both cases voltage compensation has reduced the variations significantly.

Table 3. – LOGIC LEVEL DC TRACKING RATE FOR 10K AND 10H CIRCUITS

		Min	Typ	Max
$\Delta V_{OH}/\Delta T$ (mV/°C)	10H	1.2	1.3	1.5
	10K	1.2	1.3	1.5
$\Delta V_{BB}/\Delta T$ (mV/°C)	10H	0.8	1.0	1.2
	10K	0.8	1.0	1.2
$\Delta V_{OL}/\Delta T$ (mV/°C)	10H	0	0.4	0.6
	10K	0.35	0.5	0.75
		0.75	1.0	1.55
$\Delta V_{OH}/\Delta V_{EE}$ (mV/V)	10H	–20		0
	10K	–30		0
$\Delta V_{BB}/\Delta V_{EE}$ (mV/V)	10H	0	10	25
	10K	110	150	190
$\Delta V_{OL}/\Delta V_{EE}$ (mV/V)	10H	0	20	50
	10K	200	250	320

Noise Margin Considerations

Specification of input voltage levels (V_{IHA}, V_{ILA}) are changed from those of MECL 10K resulting in improved noise margins for MECL 10H.

The MECL 10K circuits have two sets of output voltage specifications (V_{OH}, V_{OHA}, and V_{OL}, V_{OLA}). The first output voltage specification in each set (V_{OH} and V_{OL}) are guaranteed maximum and minimum output levels for typical input levels. The second specification in each set (V_{OHA} and V_{OLA}) is the guaranteed worst–case output level for input threshold voltages. System analysis for worst–case noise margin considers V_{OHA} and V_{OLA} only. The MECL 10H family has only one set of output voltages (V_{OH} and V_{OL}) with minimum and maximum values specified. The minimum value of V_{OH} and the maximum value for V_{OL} of the MECL 10H family is synonymous with the V_{OHA} and V_{OLA} specifications of MECL 10K family.

The V_{OH} values for the MECL 10H circuits are equal to or better than the MECL 10K levels at all temperatures. Input threshold voltages (V_{IHA} and V_{ILA}, which are synonymous with $V_{IH\ min}$ and $V_{IL\ max}$ for 10H) are also improved and guaranteed V_{IHA} has been decreased by 25 mV over the entire operating temperature range, resulting in a “1” level noise margin of 150 mV (compared to 125 mV for MECL 10K circuits). V_{ILA} has been decreased by 5.0 mV, providing a “0” level noise margin equal to the “1” level noise margin. The V_{OL} minimum of the MECL 10H is more

negative than for MECL 10K (–1950 mV instead of –1850 mV). The V_{OL} level for the MECL 10K family was selected to ensure that the gate would not saturate at high temperatures and high supply voltages. The reduction in operating temperature range for the MECL 10H family and the improvement in tracking rate allow the lower V_{OL} level. The change in this level does not affect system noise margins. Although some of the interface levels change with temperature, the changes in voltage levels are well within the tolerance ranges that would keep the families compatible. Table 4 lists some noise margins for V_{EE} supply variations.

Table 4. – NOISE MARGIN versus POWER–SUPPLY CONDITIONS

Parameter		V_{EE} –10% Typ	V_{EE} –10% Min	V_{EE} –5% Typ	V_{EE} –5% Min	V_{EE} Typ	V_{EE} Min	V_{EE} +5% Typ	V_{EE} +5% Min
Noise Margin High	10H	224	150	227	150	230	150	233	150
V_{NH} (mV)	10K	127	47	166	86	205	125	241	164
Noise Margin Low	10H	264	150	267	150	270	150	273	150
V_{NL} (mV)	10K	223	103	249	129	275	155	301	181

*Temp = 0 to 75°C

The compatibility of MECL 10H with MECL 10K may be demonstrated by applying the tracking rates in Table 3 to the dc specifications. The method for determining compatibility is to show acceptable noise margins for MECL 10H, MECL 10K and mixed MECL 10K/MECL 10H systems. The assumption is that the families are compatible if the noise margin for a mixed system is equal to or better than the same system using only the MECL 10K series.

Using an all MECL 10K system as a reference, three possible logic mixes must be considered: MECL 10K driving MECL 10H; MECL 10H driving MECL 10K; and MECL 10H driving MECL 10H. The system noise margin for the three configurations can now be calculated for the following cases (See Figure 3):

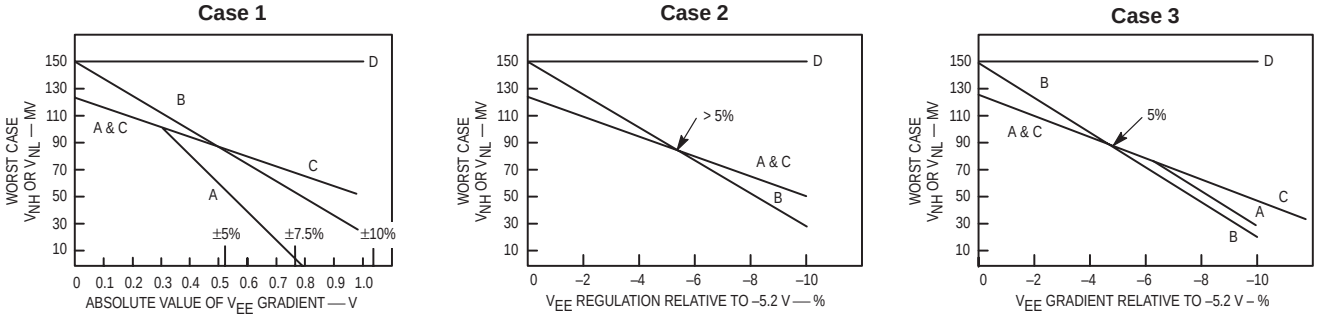
In Case 1, the system uses multiple power supplies, each independently voltage regulated to some percentage tolerance. Worst–case is where one device is at the plus extreme and the other device is at the minus extreme of the supply tolerance.

In Case 2, a system operates on a single supply or several supplies slaved to a master supply. The entire system can drift, but all devices are at the same supply voltage.

In Case 3, a system has excessive supply drops throughout. Supply gradients are due to resistive drops in V_{EE} bus.

The analysis indicates that the noise margins for a MECL 10K/10H system equal or exceed the margins for an all 10K system for supply tolerance up to ±5%. The results of the analysis are shown in Figure 3.

FIGURE 3 – NOISE MARGIN versus POWER–SUPPLY VARIATION



A = MECL 10K DRIVING MECL 10K
B = MECL 10K DRIVING MECL 10H
C = MECL 10H DRIVING MECL 10K
D = MECL 10H DRIVING MECL 10H

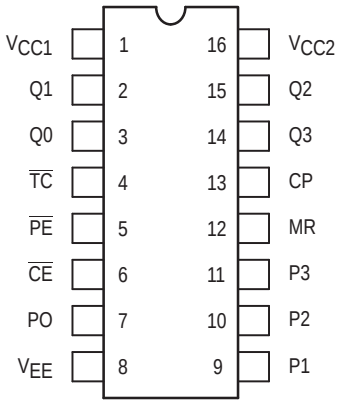
MC10H016

4-Bit Binary Counter

The MC10H016 is a high–speed synchronous, presettable, cascadable 4–bit binary counter. It is useful for a large number of conversion, counting and digital integration applications.

- Counting Frequency, 200 MHz Minimum
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible
- Positive Edge Triggered

DIP
PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

TRUTH TABLE

$\overline{CE}$	$\overline{PE}$	MR	CP	Function
L	L	L	Z	Load Parallel (P_n to Q_n)
H	L	L	Z	Load Parallel (P_n to Q_n)
L	H	L	Z	Count
H	H	L	Z	Hold
X	X	L	ZZ	Masters Respond; Slaves Hold
X	X	H	X	Reset (Q_n = LOW, $\overline{T}_C$ = HIGH)

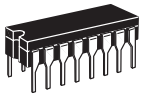
Z = Clock Pulse (Low to High); ZZ = Clock Pulse (High to Low)

Features include assertion inputs and outputs on each of the four master/slave counting flip–flops. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter.

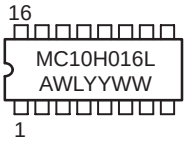
ON Semiconductor

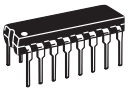
http://onsemi.com

MARKING DIAGRAMS

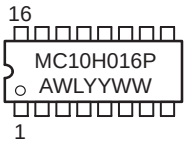


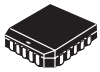
CDIP–16
L SUFFIX
CASE 620





PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H016L	CDIP–16	25 Units/Rail
MC10H016P	PDIP–16	25 Units/Rail
MC10H016FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

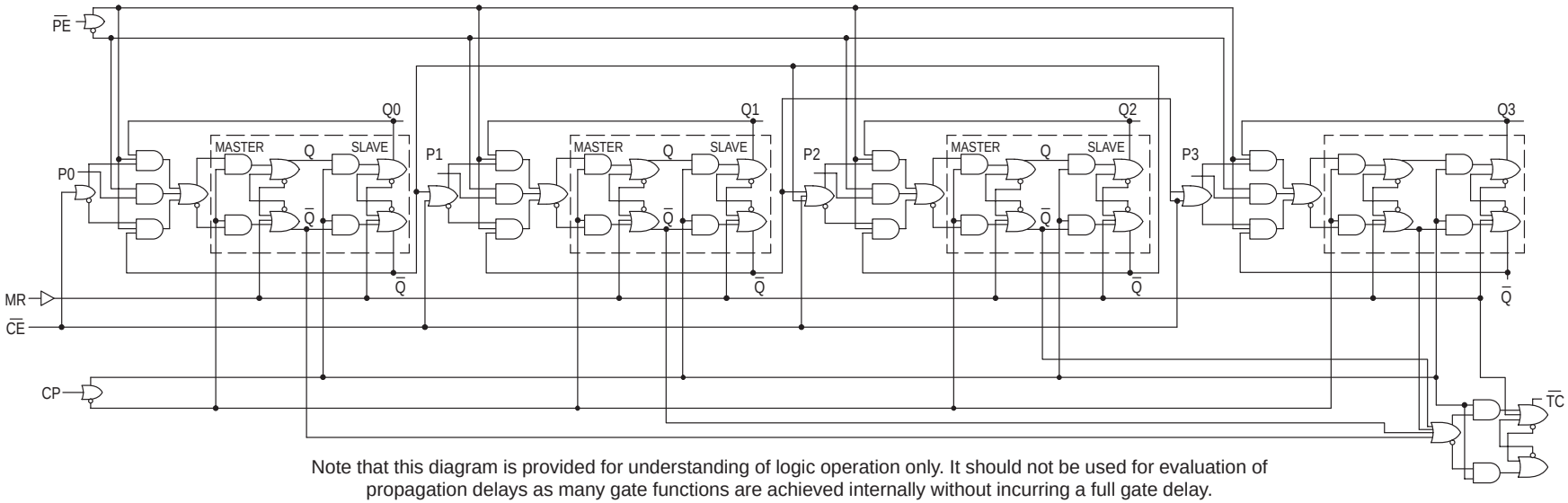
		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	126	–	115	–	126	mA
I_{inH}	Input Current High All Except MR Pin 12 MR	 – –	 450 1190	 – –	 265 700	 – –	 265 700	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

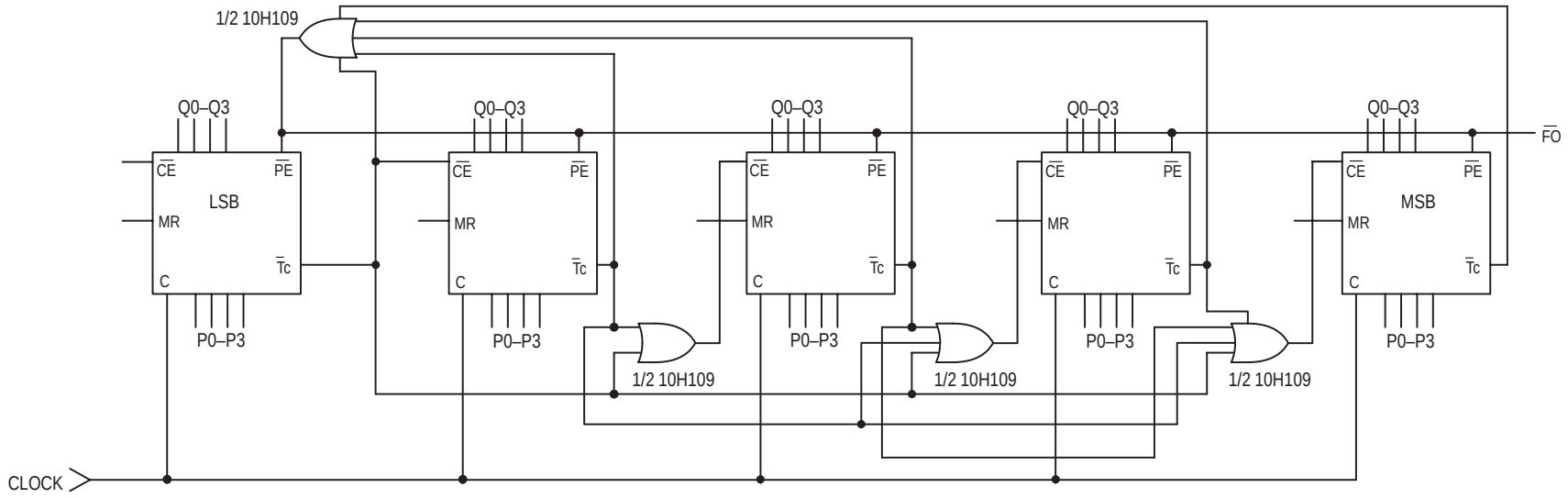
t_{pd}	Propagation Delay Clock to Q Clock to $\overline{TC}$ MR to Q	 1.0 0.7 0.7	 2.4 2.4 2.4	 1.0 0.7 0.7	 2.5 2.5 2.5	 1.0 0.7 0.7	 2.7 2.6 2.6	ns
t_{set}	Set–up Time P_n to Clock $\overline{CE}$ or $\overline{PE}$ to Clock	 2.0 2.5	 – –	 2.0 2.5	 – –	 2.0 2.5	 – –	ns
t_{hold}	Hold Time Clock to P_n Clock to $\overline{CE}$ or $\overline{PE}$	 1.0 0.5	 – –	 1.0 0.5	 – –	 1.0 0.5	 – –	ns
f_{count}	Counting Frequency	200	–	200	–	200	–	MHz
t_r	Rise Time	0.5	2.0	0.5	2.1	0.5	2.2	ns
t_f	Fall Time	0.5	2.0	0.5	2.1	0.5	2.2	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

4–Bit Binary Counter Logic Diagram



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.



÷N Counter 1 to 16 5

MC10H016 Cascaded for 5 Stage Presettable Counter

Max freq. is only OR gate delay below max when counting alone.

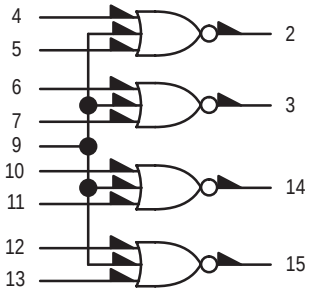
MC10H100

Quad 2-Input NOR Gate With Strobe

The MC10H100 is a quad NOR gate. Each gate has 3 inputs, two of which are independent and one of which is tied common to all four gates.

- Propagation Delay, 1.0 ns Typical
- 25 mW Typ/Gate (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

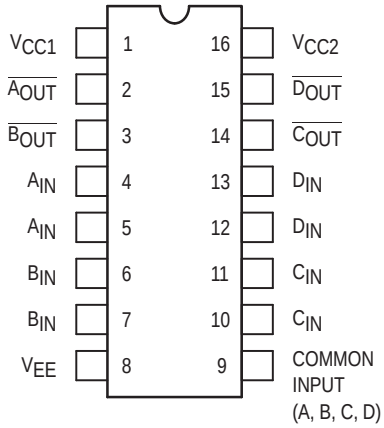
LOGIC DIAGRAM



$2 = \overline{4 + 5 + 9}$

V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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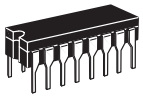
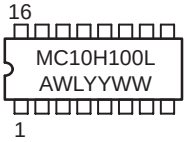
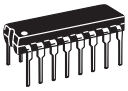
MARKING DIAGRAMS

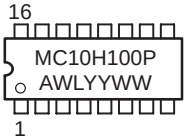


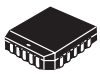
CDIP–16
L SUFFIX
CASE 620



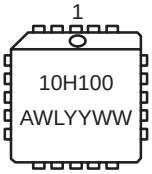


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H100L	CDIP–16	25 Units/Rail
MC10H100P	PDIP–16	25 Units/Rail
MC10H100FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	29	–	26	–	29	mA
I_{inH}	Input Current High Pin 9 All Other Inputs	 – –	 900 500	 – –	 560 310	 – –	 560 310	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay Pin 9 Only Exclude Pin 9	 0.65 0.4	 1.6 1.3	 0.7 0.45	 1.7 1.35	 0.7 0.5	 1.8 1.5	ns
t_r	Rise Time	0.5	2.0	0.5	2.1	0.5	2.2	ns
t_f	Fall Time	0.5	2.0	0.5	2.1	0.5	2.2	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

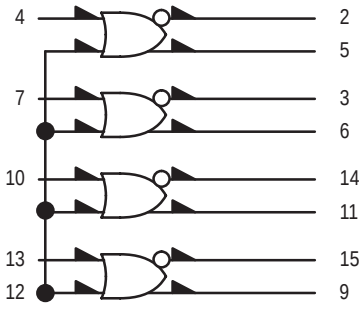
MC10H101

Quad OR/NOR Gate

The MC10H101 is a quad 2–input OR/NOR gate with one input from each gate common to pin 12. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increases in power–supply current.

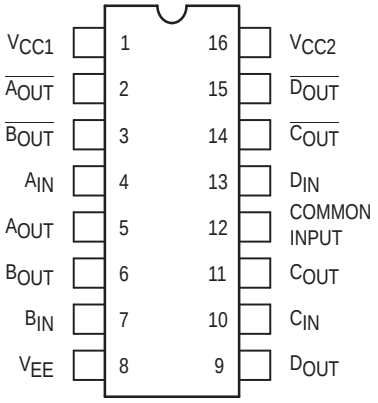
- Propagation Delay, 1.0 ns Typical
- Power Dissipation 25 mW/Gate (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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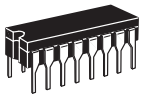
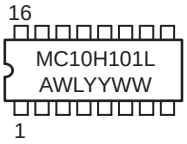
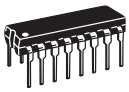
MARKING DIAGRAMS

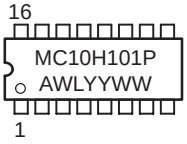


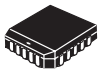
CDIP–16
L SUFFIX
CASE 620



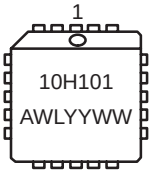


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H101L	CDIP–16	25 Units/Rail
MC10H101P	PDIP–16	25 Units/Rail
MC10H101FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	29	–	26	–	29	mA
I_{inH}	Input Current High (Pin 12 only)	– –	425 850	– –	265 535	– –	265 535	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay Pin 12 Only Exclude Pin 12	 0.5 0.5	 1.6 1.45	 0.5 0.5	 1.6 1.5	 0.5 0.5	 1.7 1.6	ns
t_r	Rise Time	0.5	2.1	0.5	2.2	0.5	2.3	ns
t_f	Fall Time	0.5	2.1	0.5	2.2	0.5	2.3	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

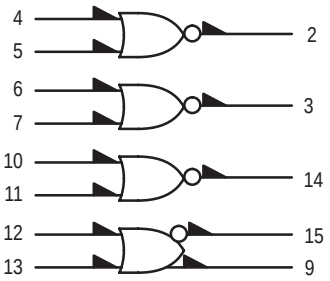
MC10H102

Quad 2-Input NOR Gate

The MC10H102 is a quad 2–input NOR gate. The MC10H102 provides one gate with OR/NOR outputs. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increases in power– supply current.

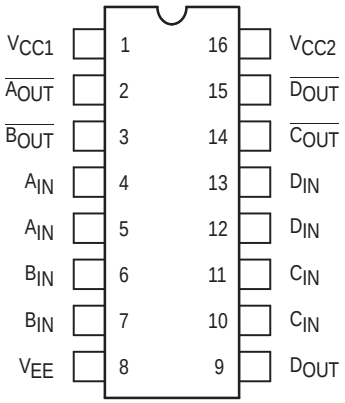
- Propagation Delay, 1.0 ns Typical
- Power Dissipation 25 mW/Gate (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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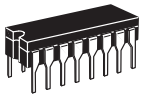
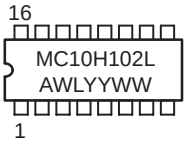
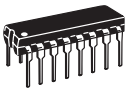
MARKING DIAGRAMS

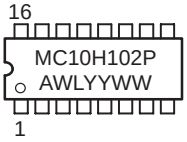


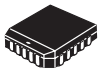
CDIP–16
L SUFFIX
CASE 620



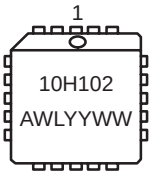


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H102L	CDIP–16	25 Units/Rail
MC10H102P	PDIP–16	25 Units/Rail
MC10H102FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	29	–	26	–	29	mA
I_{inH}	Input Current High	–	425	–	265	–	265	μA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	μA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay	0.4	1.25	0.4	1.25	0.4	1.4	ns
t_r	Rise Time	0.5	1.5	0.5	1.6	0.55	1.7	ns
t_f	Fall Time	0.5	1.5	0.5	1.6	0.55	1.7	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

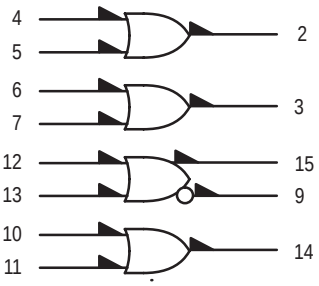
MC10H103

Quad 2-Input OR Gate

The MC10H103 is a quad 2–input OR gate. The MC10H103 provides one gate with OR/NOR outputs. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increases in power– supply current.

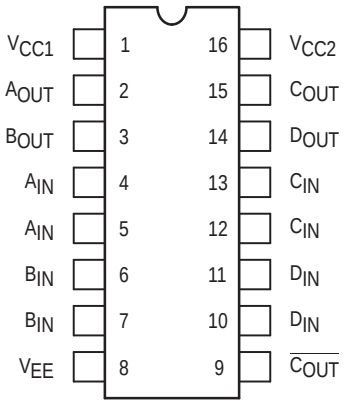
- Propagation Delay, 1.0 ns Typical
- Power Dissipation 25 mW/Gate (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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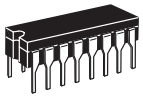
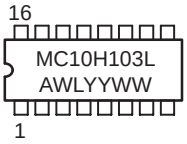
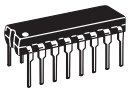
MARKING DIAGRAMS

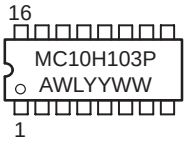


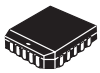
CDIP–16
L SUFFIX
CASE 620



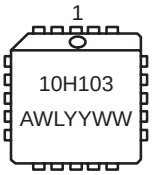


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H103L	CDIP–16	25 Units/Rail
MC10H103P	PDIP–16	25 Units/Rail
MC10H103FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	29	–	26	–	29	mA
I_{inH}	Input Current High	–	425	–	265	–	265	μA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	μA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay	0.4	1.3	0.4	1.3	0.45	1.45	ns
t_r	Rise Time	0.5	1.7	0.5	1.8	0.5	1.9	ns
t_f	Fall Time	0.5	1.7	0.5	1.8	0.5	1.9	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

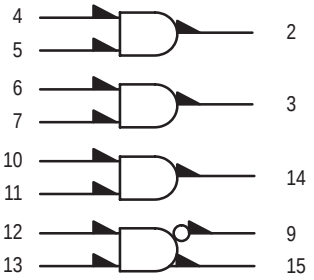
MC10H104

Quad 2-Input AND Gate

The MC10H104 is a quad 2–input AND gate. One of the gates has both AND/NAND outputs available. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power– supply current.

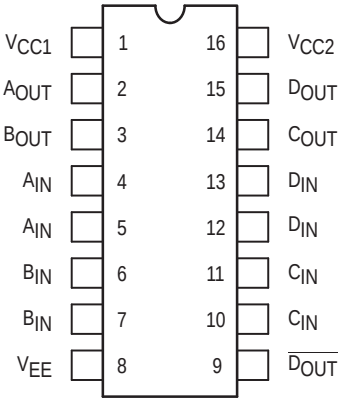
- Propagation Delay, 1.0 ns Typical
- Power Dissipation 25 mW/Gate (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP
PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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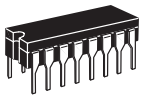
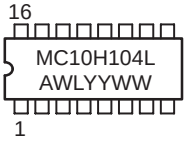
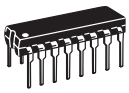
MARKING DIAGRAMS

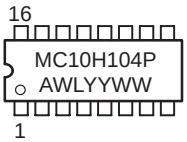


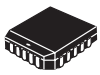
CDIP–16
L SUFFIX
CASE 620



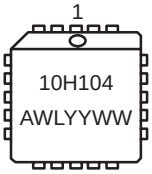


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H104L	CDIP–16	25 Units/Rail
MC10H104P	PDIP–16	25 Units/Rail
MC10H104FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	39	–	35	–	39	mA
I_{inH}	Input Current High	–	425	–	265	–	265	μA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	μA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay	0.4	1.6	0.45	1.75	0.45	1.9	ns
t_r	Rise Time	0.5	1.6	0.5	1.7	0.5	1.8	ns
t_f	Fall Time	0.5	1.6	0.5	1.7	0.5	1.8	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

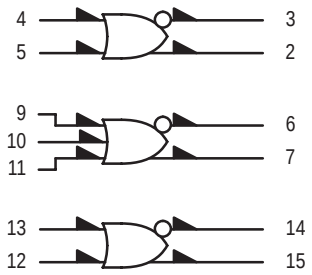
MC10H105

Triple 2-3-2-Input OR/NOR Gate

The MC10H105 is a triple 2–3–2–input OR/NOR gate. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increases in power–supply current.

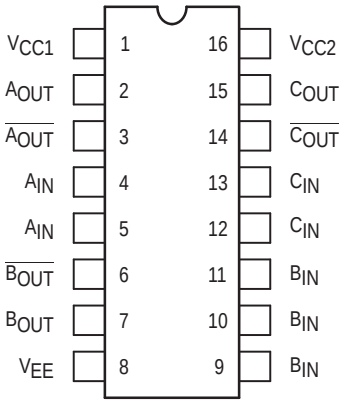
- Propagation Delay, 1.0 ns Typical
- Power Dissipation 25 mW/Gate (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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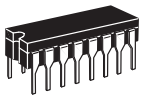
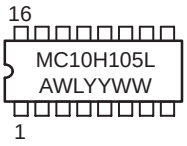
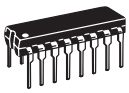
MARKING DIAGRAMS

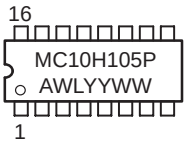


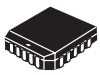
CDIP–16
L SUFFIX
CASE 620



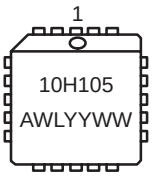


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H105L	CDIP–16	25 Units/Rail
MC10H105P	PDIP–16	25 Units/Rail
MC10H105FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	23	–	21	–	23	mA
I_{inH}	Input Current High	–	425	–	265	–	265	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay	0.43	1.2	0.4	1.2	0.4	1.3	ns
t_r	Rise Time	0.5	1.5	0.5	1.6	0.5	1.7	ns
t_f	Fall Time	0.5	1.5	0.5	1.6	0.5	1.7	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

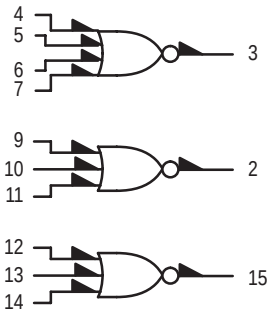
MC10H106

Triple 4-3-3-Input NOR Gate

The MC10H106 is a triple 4–3–3 input NOR gate. This 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power– supply current.

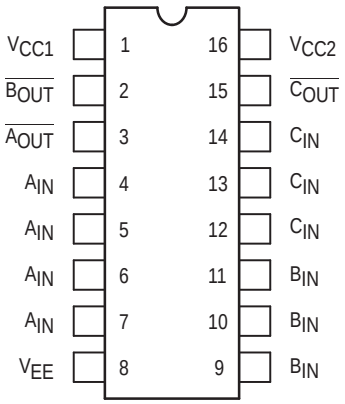
- Propagation Delay, 1.0 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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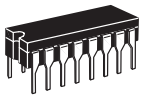
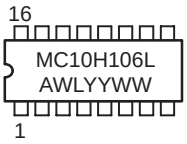
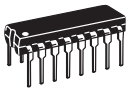
MARKING DIAGRAMS

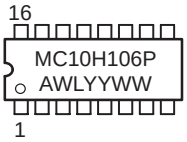


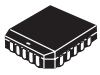
CDIP–16
L SUFFIX
CASE 620



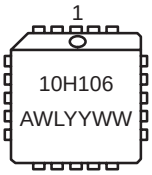


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H106L	CDIP–16	25 Units/Rail
MC10H106P	PDIP–16	25 Units/Rail
MC10H106FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	23	–	21	–	23	mA
I_{inH}	Input Current High	–	500	–	310	–	310	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay	0.5	1.3	0.5	1.5	0.55	1.55	ns
t_r	Rise Time	0.5	1.7	0.5	1.8	0.55	1.9	ns
t_f	Fall Time	0.5	1.7	0.5	1.8	0.55	1.9	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

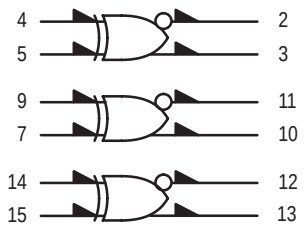
MC10H107

Triple 2-Input Exclusive OR/ Exclusive NOR Gate

The MC10H107 is a triple 2–input exclusive OR/NOR gate. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power–supply current.

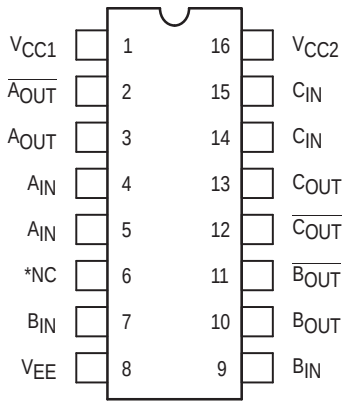
- Propagation Delay, 1.0 ns Typical
- Power Dissipation 35 mW/Gate Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



***NC = No Connection**

Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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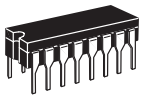
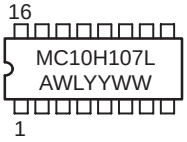
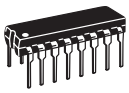
MARKING DIAGRAMS

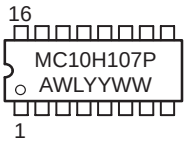


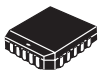
CDIP–16
L SUFFIX
CASE 620



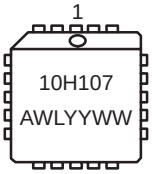


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H107L	CDIP–16	25 Units/Rail
MC10H107P	PDIP–16	25 Units/Rail
MC10H107FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	31	–	28	–	31	mA
I_{inH}	Input Current High	–	425	–	265	–	265	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay	0.4	1.5	0.4	1.6	0.4	1.7	ns
t_r	Rise Time	0.5	1.5	0.5	1.6	0.5	1.7	ns
t_f	Fall Time	0.5	1.5	0.5	1.6	0.5	1.7	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

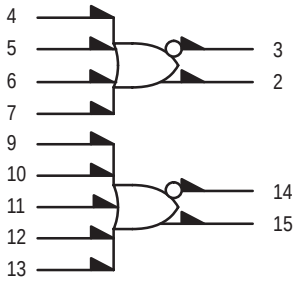
MC10H109

Dual 4-5-Input OR/NOR Gate

The MC10H109 is a dual 4–5–input OR/NOR gate. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power–supply current.

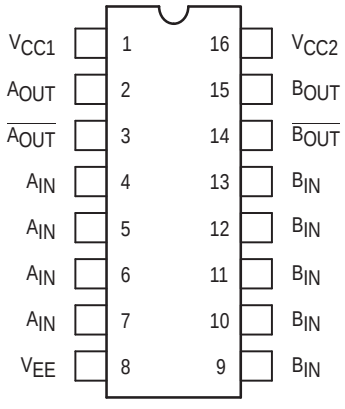
- Propagation Delay, 1.0 ns Typical
- Power Dissipation 35 mW/Gate Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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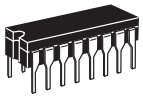
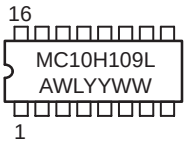
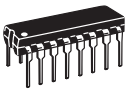
MARKING DIAGRAMS

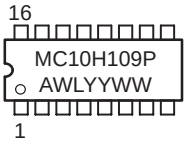


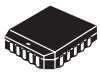
CDIP–16
L SUFFIX
CASE 620



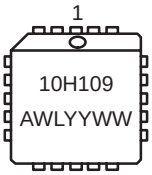


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H109L	CDIP–16	25 Units/Rail
MC10H109P	PDIP–16	25 Units/Rail
MC10H109FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	15	–	14	–	15	mA
I_{inH}	Input Current High	–	425	–	265	–	265	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay	0.4	1.3	0.4	1.3	0.45	1.45	ns
t_r	Rise Time	0.5	2.0	0.5	2.1	0.5	2.2	ns
t_f	Fall Time	0.5	2.0	0.5	2.1	0.5	2.2	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

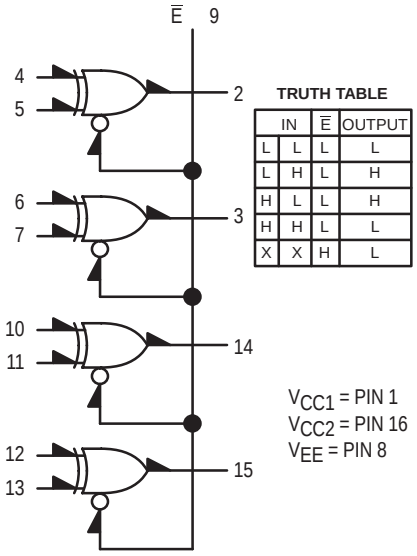
MC10H113

Quad Exclusive OR Gate

The MC10H113 is a Quad Exclusive OR Gate with an enable common to all four gates. The outputs may be wire–ORed together to perform a 4–bit comparison function (A = B). The enable is active LOW.

- Propagation Delay, 1.3 ns Typical
- Power Dissipation 175 mW Typ/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

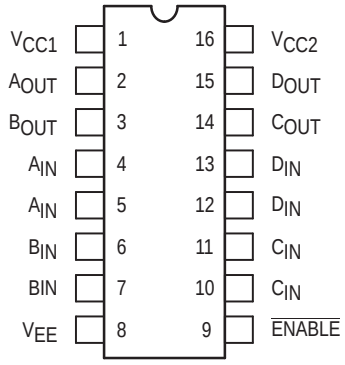
LOGIC DIAGRAM



TRUTH TABLE

IN		$\overline{E}$	OUTPUT
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
X	X	H	L

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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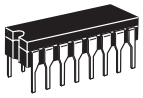
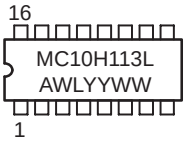
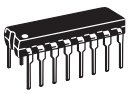
MARKING DIAGRAMS

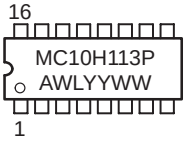


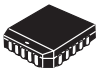
CDIP–16
L SUFFIX
CASE 620



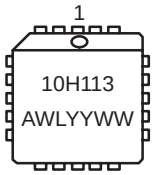


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H113L	CDIP–16	25 Units/Rail
MC10H113P	PDIP–16	25 Units/Rail
MC10H113FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	46	–	42	–	46	mA
I_{inH}	Input Current High Pins 5, 7, 11, 13 Pins 4, 6, 10, 12 Pin 9	 – – –	 430 510 1100	 – – –	 270 320 740	 – – –	 270 320 740	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay Data Enable	 0.4 0.5	 1.7 2.3	 0.4 0.5	 1.8 2.4	 0.5 0.6	 1.9 2.5	ns
t_r	Rise Time	0.5	1.8	0.6	1.9	0.6	2.0	ns
t_f	Fall Time	0.5	1.8	0.6	1.9	0.6	2.0	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

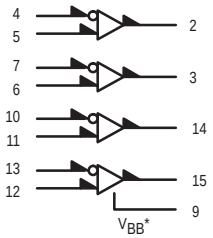
MC10H115

Quad Line Receiver

The MC10H115 is a quad differential amplifier designed for use in sensing differential signals over long lines. This 10H part is a functional/ pinout duplication of the standard MECL 10K family part, with 100% improvement in counting frequency and no increase in power–supply current.

The base bias supply (V_{BB}) is made available at Pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary. Active current sources provide the MC10H115 with excellent common mode rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (Pin 9) to prevent upsetting the current source bias network.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 110 mW Typ/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

When input pin with bubble goes positive its respective output pin with bubble goes positive.

LOGIC DIAGRAM

*V_{BB} to be used to supply bias to the MC10H115 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor to ground (0 V). V_{BB} can source < 1.0 mA.

The MC10H115 is designed to be used in sensing differential signals over long lines. The bias supply (V_{BB}) is made available to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

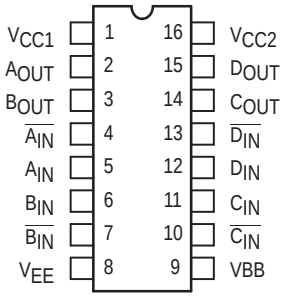
Active current sources provide these receivers with excellent common–mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} to prevent unbalancing the current–source bias network.

The MC10H115 does not have internal–input pull– down resistors. This provides high impedance to the amplifier input and facilitates differential connections.

Applications:

- Low Level Receiver
- Schmitt Trigger
- Voltage Level Interface

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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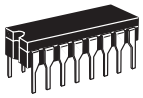
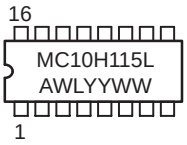
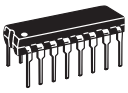
MARKING DIAGRAMS

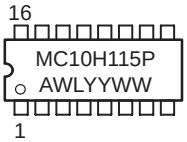


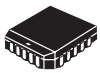
CDIP–16
L SUFFIX
CASE 620



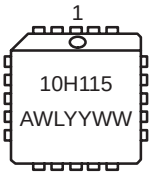


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H115L	CDIP–16	25 Units/Rail
MC10H115P	PDIP–16	25 Units/Rail
MC10H115FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (Note 2.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	29	–	26	–	29	mA
I_{inH}	Input Current High	–	150	–	95	–	95	μA
I_{CBO}	Input Leakage Current	–	1.5	–	1.0	–	1.0	μA
V_{BB}	Reference Voltage	–1.38	–1.27	–1.35	–1.25	–1.31	–1.19	Vdc
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage (Note 1.)	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage (Note 1.)	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc
V_{CMR}	Common Mode Range (Note 3.)	–	–	–2.85 to –0.8		–	–	Vdc
V_{PP}	Input Sensitivity (Note 4.)	–	–	150 typ		–	–	mV_{PP}

AC PARAMETERS

t_{pd}	Propagation Delay	0.4	1.3	0.4	1.3	0.45	1.45	ns
t_r	Rise Time	0.5	1.4	0.5	1.5	0.5	1.6	ns
t_f	Fall Time	0.5	1.4	0.5	1.5	0.5	1.6	ns

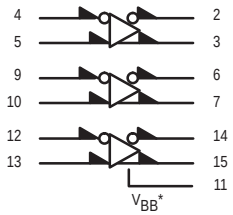
1. When V_{BB} is used as the reference voltage.
2. Each MECL 10H series circuit has been designed to meet the specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.
3. Differential input not to exceed 1.0 Vdc.
4. 150 $mV_{p–p}$ differential input required to obtain full logic swing on output.

MC10H116

Triple Line Receiver

The MC10H116 is a functional/pinout duplication of the MC10116, with 100% improvement in propagation delay and no increase in power–supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 85 mW Typ/Pkg (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

When input pin with bubble goes positive it's respective output pin with bubble goes positive.

LOGIC DIAGRAM

*V_{BB} to be used to supply bias to the MC10H115 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor to ground (0 V). V_{BB} can source < 1.0 mA.

The MC10H115 is designed to be used in sensing differential signals over long lines. The bias supply (V_{BB}) is made available to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

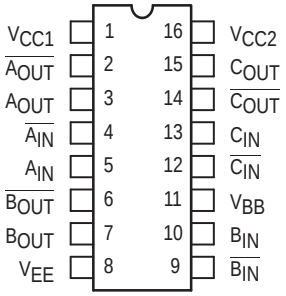
Active current sources provide these receivers with excellent common–mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} to prevent unbalancing the current–source bias network.

The MC10H115 does not have internal–input pull– down resistors. This provides high impedance to the amplifier input and facilitates differential connections.

Applications:

- Low Level Receiver
- Schmitt Trigger
- Voltage Level Interface

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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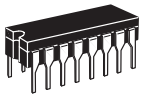
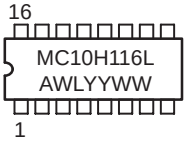
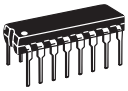
MARKING DIAGRAMS

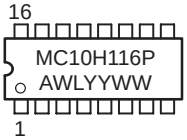


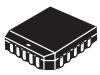
CDIP–16
L SUFFIX
CASE 620





PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H116L	CDIP–16	25 Units/Rail
MC10H116P	PDIP–16	25 Units/Rail
MC10H116FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (Note 2.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	23	–	21	–	23	mA
I_{inH}	Input Current High	–	150	–	95	–	95	μA
I_{CBO}	Input Leakage Current	–	1.5	–	1.0	–	1.0	μA
V_{BB}	Reference Voltage	–1.38	–1.27	–1.35	–1.25	–1.31	–1.19	Vdc
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage (Note 1.)	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage (Note 1.)	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc
V_{CMR}	Common Mode Range (Note 4.)	–	–	–2.85 to –0.8		–	–	Vdc
V_{PP}	Input Sensitivity (Note 3.)	–	–	150 typ		–	–	mV_{PP}

AC PARAMETERS

t_{pd}	Propagation Delay	0.4	1.3	0.4	1.3	0.45	1.45	ns
t_r	Rise Time	0.5	1.5	0.5	1.6	0.5	1.7	ns
t_f	Fall Time	0.5	1.5	0.5	1.6	0.5	1.7	ns

1. When V_{BB} is used as the reference voltage.
2. Each MECL 10H series circuit has been designed to meet the specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.
3. Differential input not to exceed 1.0 Vdc.
4. 150 $mV_{p–p}$ differential input required to obtain full logic swing on output.

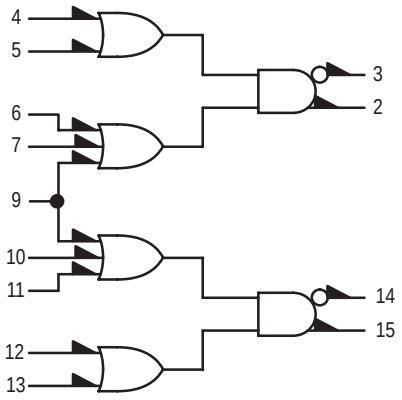
MC10H117

Dual 2-Wide 2-3-Input OR-AND/OR-AND Gate

The MC10H117 dual 2–wide 2–3–input OR–AND/OR–AND–Invert gate is a general purpose logic element designed for use in data control, such as digital multiplexing or data distribution. Pin 9 is common to both gates. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power–supply current.

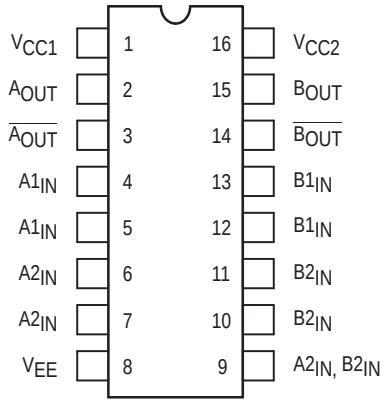
- Propagation Delay, 1.0 ns Typical
- Power Dissipation 100 mW/Gate Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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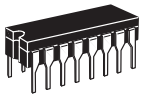
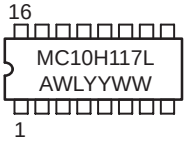
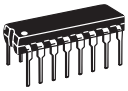
MARKING DIAGRAMS

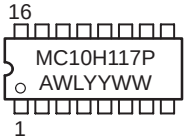


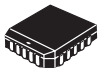
CDIP–16
L SUFFIX
CASE 620





PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H117L	CDIP–16	25 Units/Rail
MC10H117P	PDIP–16	25 Units/Rail
MC10H117FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current — Continuous — Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range — Plastic — Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	—	29	—	26	—	29	mA
I_{inH}	Input Current High							µA
	Pins 4, 5, 12, 13	—	465	—	275	—	275	
	Pins 6, 7, 10, 11	—	545	—	320	—	320	
	Pin 9	—	710	—	415	—	415	
I_{inL}	Input Current Low	0.5	—	0.5	—	0.3	—	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay	0.45	1.35	0.45	1.35	0.5	1.5	ns
t_r	Rise Time	0.5	1.5	0.5	1.6	0.5	1.7	ns
t_f	Fall Time	0.5	1.5	0.5	1.6	0.5	1.7	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

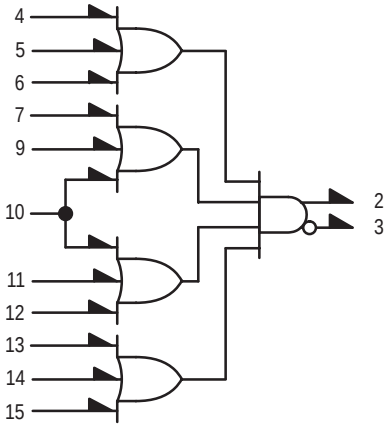
MC10H121

4-Wide OR-AND/$\overline{\text{OR-AND}}$ Gate

The MC10H121 is a basic logic building block providing the simultaneous OR–AND/OR–AND–Invert function, useful in data control and digital multiplexing applications. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power– supply current.

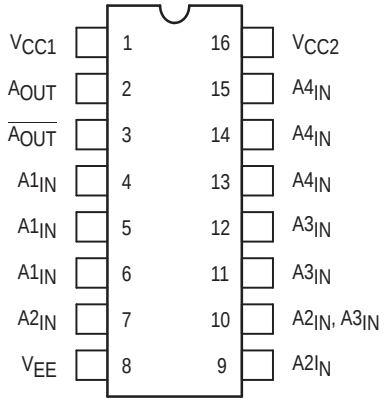
- Propagation Delay, 1.0 ns Typical
- Power Dissipation 100 mW/Gate Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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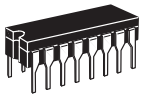
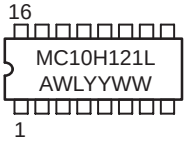
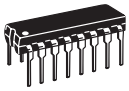
MARKING DIAGRAMS

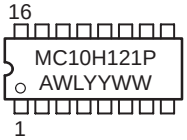


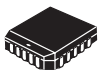
CDIP–16
L SUFFIX
CASE 620





PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H121L	CDIP–16	25 Units/Rail
MC10H121P	PDIP–16	25 Units/Rail
MC10H121FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current — Continuous — Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range — Plastic — Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	—	29	—	26	—	29	mA
I_{inH}	Input Current High Pins 3, 4, 5, 6, 7, 9 11, 12, 13, 14, 15 Pin 10	 — —	 500 610	 — —	 295 360	 — —	 295 360	µA
I_{inL}	Input Current Low	0.5	—	0.5	—	0.3	—	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay Pin 10 Only Exclude Pin 10	 0.45 0.55	 1.8 1.95	 0.45 0.6	 1.8 2.0	 0.55 0.7	 2.2 2.4	ns
t_r	Rise Time	0.5	1.7	0.5	1.8	0.5	1.9	ns
t_f	Fall Time	0.5	1.7	0.5	1.8	0.5	1.9	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

MC10H123

Triple 4-3-3-Input Bus Driver

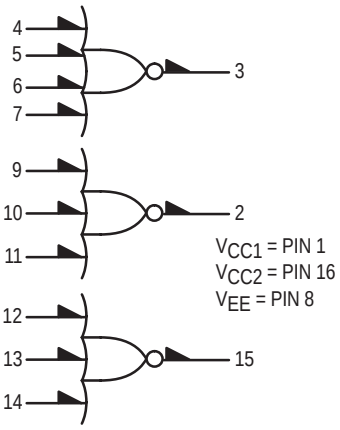
The MC10H123 is a triple 4–3–3–Input Bus Driver.

The MC10H123 consists of three NOR gates designed for bus driving applications on card or between cards. Output low logic levels are specified with V_{OL} = –2.1 Vdc so that the bus may be terminated to –2.0 Vdc. The gate output, when low, appears as a high impedance to the bus, because the output emitter–followers of the MC10H123 are "turned–off." This eliminates discontinuities in the characteristic impedance of the bus.

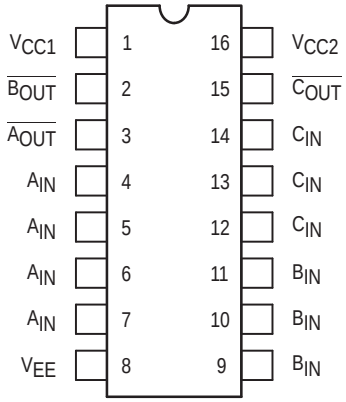
The V_{OH} level is specified when driving a 25–ohm load terminated to –2.0 Vdc, the equivalent of a 50–ohm bus terminated at both ends. Although 25 ohms is the lowest characteristic impedance that can be driven by the MC10H123, higher impedance values may be used with this part. A typical 50–ohm bus is shown in Figure 1.

- Propagation Delay, 1.5 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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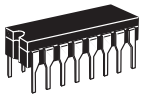
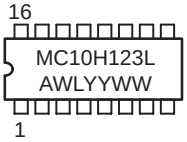
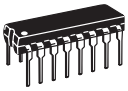
MARKING DIAGRAMS

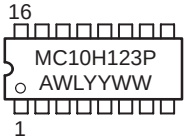


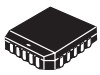
CDIP–16
L SUFFIX
CASE 620



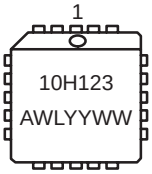


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H123L	CDIP–16	25 Units/Rail
MC10H123P	PDIP–16	25 Units/Rail
MC10H123FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current — Continuous — Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range — Plastic — Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

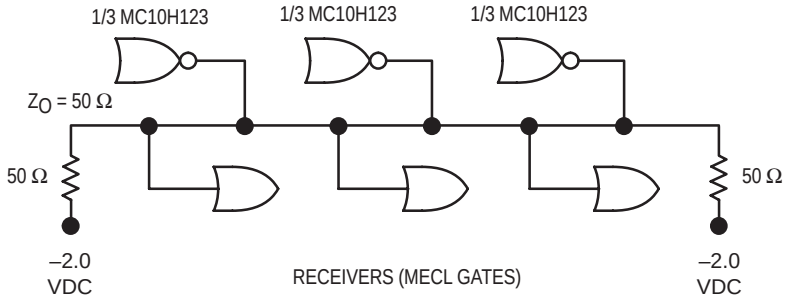
		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	—	60	—	56	—	60	mA
I_{inH}	Input Current High	—	495	—	310	—	310	µA
I_{inL}	Input Current Low	0.5	—	0.5	—	0.3	—	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–2.1	–2.03	–2.1	–2.03	–2.1	–2.03	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay	0.7	1.5	0.7	1.6	0.7	1.7	ns
t_r	Rise Time	0.7	1.6	0.7	1.7	0.7	1.8	ns
t_f	Fall Time	0.7	1.6	0.7	1.7	0.7	1.8	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.1 volts.

FIGURE 1 — 50–OHM BUS DRIVER (25–OHM LOAD)



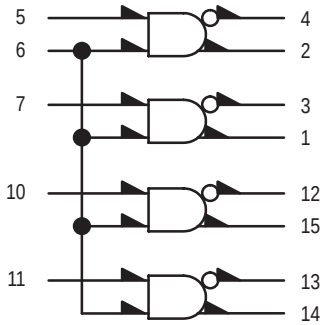
MC10H124

Quad TTL-to-MECL Translator With TTL Strobe Input

The MC10H124 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power–supply current.

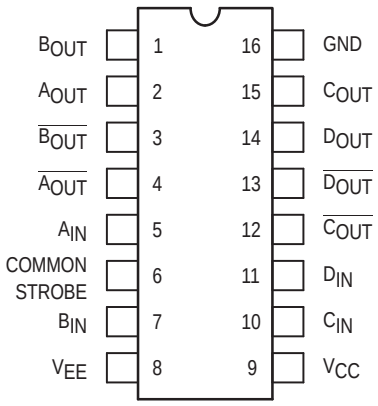
- Propagation Delay, 1.5 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



GND = PIN 16
V_{CC} (+5.0 VDC)= PIN 9
V_{EE} (–5.2 VDC) = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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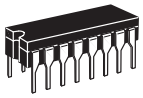
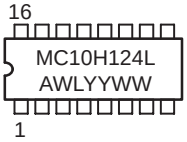
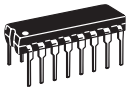
MARKING DIAGRAMS

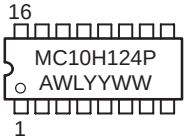


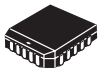
CDIP–16
L SUFFIX
CASE 620





PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H124L	CDIP–16	25 Units/Rail
MC10H124P	PDIP–16	25 Units/Rail
MC10H124FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 5.0 V)	–8.0 to 0	Vdc
V_{CC}	Power Supply (V_{EE} = –5.2 V)	0 to +7.0	Vdc
V_I	Input Voltage (V_{CC} = 5.0 V) TTL	0 to V_{CC}	Vdc
I_{out}	Output Current — Continuous — Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range — Plastic — Ceramic	–55 to +150 –55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%, V_{CC} = 5.0 V ± 5.0%)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Negative Power Supply Drain Current	—	72	—	66	—	72	mA
I_{CCH}	Positive Power Supply Drain Current	—	16	—	16	—	18	mA
I_{CCL}		—	25	—	25	—	25	mA
I_R	Reverse Current Pin 6 Pin 7	 — —	 200 50	 — —	 200 50	 — —	 200 50	µA
I_F	Forward Current Pin 6 Pin 7	 — —	 –12.8 –3.2	 — —	 –12.8 –3.2	 — —	 –12.8 –3.2	mA
$V_{(BR)in}$	Input Breakdown Voltage	5.5	—	5.5	—	5.5	—	Vdc
V_I	Input Clamp Voltage	—	–1.5	—	–1.5	—	–1.5	Vdc
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	2.0	—	2.0	—	2.0	—	Vdc
V_{IL}	Low Input Voltage	—	0.8	—	0.8	—	0.8	Vdc

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%, V_{CC} = 5.0 V ± 5.0%)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
AC PARAMETERS								
t_{pd}	Propagation Delay	0.55	2.25	0.55	2.4	0.85	2.95	ns
t_r	Rise Time	0.5	1.5	0.5	1.6	0.5	1.7	ns
t_f	Fall Time	0.5	1.5	0.5	1.6	0.5	1.7	ns

APPLICATIONS INFORMATION

The MC10H124 has TTL–compatible inputs and MECL complementary open–emitter outputs that allow use as an inverting/non–inverting translator or as a differential line driver. When the common strobe input is at the low–logic level, it forces all true outputs to a MECL low–logic state and all inverting outputs to a MECL high–logic state.

An advantage of this device is that TTL–level information can be transmitted differentially, via balanced twisted pair lines, to MECL equipment, where the signal can be received by the MC10H115 or MC10H116 differential line receivers. The power supply requirements are ground, +5.0 volts, and –5.2 volts.

MC10H125

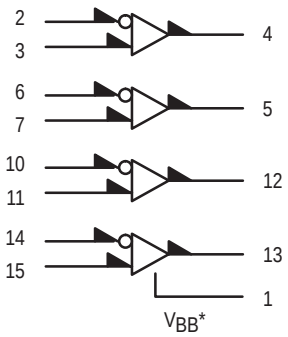
Quad MECL-to-TTL Translator

The MC10H125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic section of digital systems. The 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power–supply current.

Outputs of unused translators will go to low state when their inputs are left open.

- Propagation Delay, 2.5 ns Typical
- Voltage Compensated
- Improved Noise Margin 150 mV
  (Over Operating Voltage and Temperature Range)
- MECL 10K–Compatible

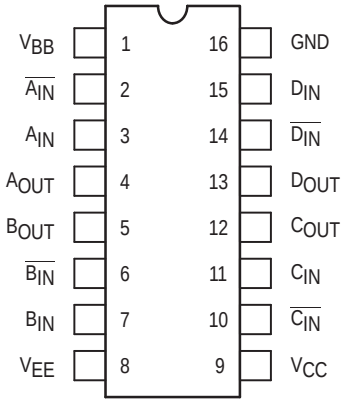
LOGIC DIAGRAM



GND = PIN 16
V_{CC} (+5.0 VDC) = PIN 9
V_{EE} (–5.2 VDC) = PIN 8

*V_{BB} to be used to supply bias to the MC10H125 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor to ground (0 V). V_{BB} can source < 1.0 mA.

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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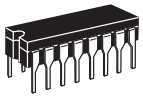
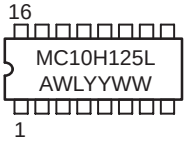
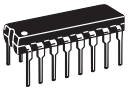
MARKING DIAGRAMS

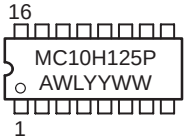


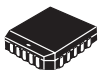
CDIP–16
L SUFFIX
CASE 620



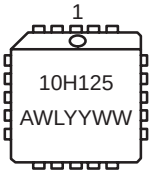


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H125L	CDIP–16	25 Units/Rail
MC10H125P	PDIP–16	25 Units/Rail
MC10H125FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 5.0 V)	–8.0 to 0	Vdc
V_{CC}	Power Supply (V_{EE} = –5.2 V)	0 to +7.0	Vdc
V_I	Input Voltage (V_{CC} = 5.0 V)	0 to V_{EE}	Vdc
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range — Plastic — Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%; V_{CC} = 5.0 V ± 5.0 %) (See Note)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Negative Power Supply Drain Current	—	44	—	40	—	44	mA
I_{CCH}	Positive Power Supply Drain Current	—	63	—	63	—	63	mA
I_{CCL}		—	40	—	40	—	40	mA
I_{inH}	Input Current	—	225	—	145	—	145	µA
I_{CBO}	Input Leakage Current	—	1.5	—	1.0	—	1.0	µA
V_{OH}	High Output Voltage I_{OH} = –1.0 mA	2.5	—	2.5	—	2.5	—	Vdc
V_{OL}	Low Output Voltage I_{OL} = +20 mA	—	0.5	—	0.5	—	0.5	Vdc
V_{IH}	High Input Voltage(1)	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage(1)	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc
I_{OS}	Short Circuit Current	60	150	60	150	50	150	mA
V_{BB}	Reference Voltage	–1.38	–1.27	–1.35	–1.25	–1.31	–1.19	Vdc
V_{CMR}	Common Mode Range (3)	—	—	–2.85 to +0.3				V
		Typical						
V_{PP}	Input Sensitivity (4)	150						mV

AC PARAMETERS

t_{pd}	Propagation Delay	0.8	3.3	0.85	3.35	0.9	3.4	ns
t_r	Rise Time(5)	0.3	1.2	0.3	1.2	0.3	1.2	ns
t_f	Fall Time(5)	0.3	1.2	0.3	1.2	0.3	1.2	ns

1. When V_{BB} is used as the reference voltage.
2. Each MECL 10H series circuit has been designed to meet the specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.
3. Differential input not to exceed 1.0 Vdc.
4. 150 mV_{p-p} differential input required to obtain full logic swing on output.
5. 1.0 V to 2.0 V w/25 pF into 500 Ω.

APPLICATION INFORMATION

The MC10H125 incorporates differential inputs and Schottky TTL “totem pole” outputs. Differential inputs allow for use as an inverting/non–inverting translator or as a differential line receiver. The V_{BB} reference voltage is available on Pin 1 for use in single–ended input biasing. The outputs of the MC10H125 go to a low–logic level whenever the inputs are left floating, and a high–logic output level is achieved with a minimum input level of 150 mV_{p-p}.

An advantage of this device is that MECL–level information can be received, via balanced twisted pair lines, in the TTL equipment. This isolates the MECL–logic from the noisy TTL environment. Power supply requirements are ground, +5.0 volts and –5.2 volts.

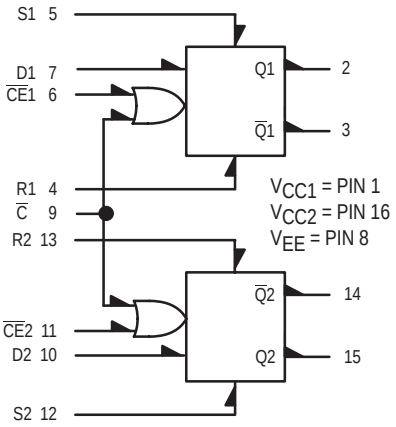
MC10H130

Dual Latch

The MC10H130 is a MECL 10H part which is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock speed and propagation delay and no increase in power–supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation, 155 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

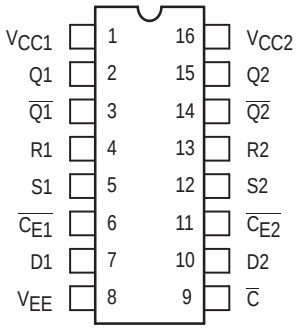
LOGIC DIAGRAM



TRUTH TABLE

D	$\overline{C}$	$\overline{CE}$	Q_{n+1}
L	L	L	L
H	L	L	H
X	L	H	Q_n
X	H	L	Q_n
X	H	H	Q_n

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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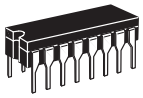
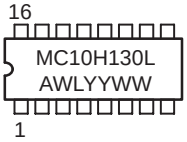
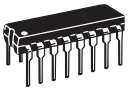
MARKING DIAGRAMS

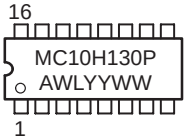


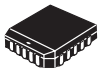
CDIP–16
L SUFFIX
CASE 620



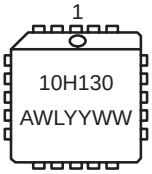


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H130L	CDIP–16	25 Units/Rail
MC10H130P	PDIP–16	25 Units/Rail
MC10H130FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	38	–	35	–	38	mA
I_{inH}	Input Current High Pins 6, 11 Pins 7, 9, 10 Pins 4, 5, 12, 13	 – – –	 468 545 434	 – – –	 275 320 255	 – – –	 275 320 255	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay Data Set, Reset Clock, $\overline{CE}$	 0.4 0.6 0.5	 1.6 1.7 1.6	 0.4 0.7 0.5	 1.7 1.8 1.7	 0.4 0.8 0.6	 1.8 1.9 1.8	ns
t_r	Rise Time	0.5	1.6	0.5	1.7	0.5	1.8	ns
t_f	Fall Time	0.5	1.6	0.5	1.7	0.5	1.8	ns
t_{set}	Set–up Time	2.2	–	2.2	–	2.2	–	ns
t_{hold}	Hold Time	0.7	–	0.7	–	0.7	–	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

APPLICATION INFORMATION

The MC10H130 is a clocked dual D type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock ($\overline{C}$).

Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

The set and reset inputs do not override the clock and D inputs. They are effective only when either $\overline{C}$ or $\overline{CE}$ or both are high.

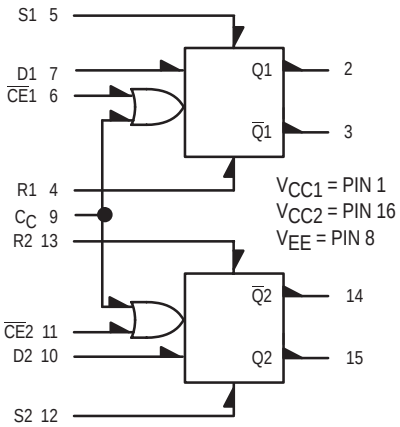
MC10H131

Dual D Type Master-Slave Flip-Flop

The MC10H131 is a MECL 10H part which is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock speed and propagation delay and no increase in power–supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation, 235 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



RS TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

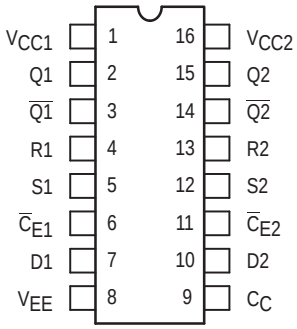
CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	X	Q_n
H	L	L
H	H	H

$C = \overline{CE} + C_C$

A clock H is a clock transition from a low to a high state.

DIP
PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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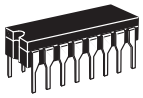
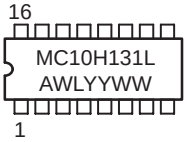
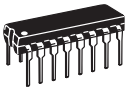
MARKING DIAGRAMS

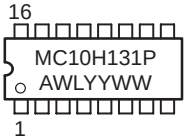


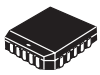
CDIP–16
L SUFFIX
CASE 620





PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H131L	CDIP–16	25 Units/Rail
MC10H131P	PDIP–16	25 Units/Rail
MC10H131FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	62	–	56	–	62	mA
I_{inH}	Input Current High Pins 6, 11 Pin 9 Pins 7, 10 Pins 4, 5, 12, 13	 – – – –	 530 660 485 790	 – – – –	 310 390 285 465	 – – – –	 310 390 285 465	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay Clock, $\overline{CE}$ Set, Reset	 0.8 0.6	 1.6 1.6	 0.8 0.7	 1.7 1.7	 0.8 0.7	 1.8 1.8	ns
t_r	Rise Time	0.6	2.0	0.6	2.0	0.6	2.2	ns
t_f	Fall Time	0.6	2.0	0.6	2.0	0.6	2.2	ns
t_{set}	Set–up Time	0.7	–	0.7	–	0.7	–	ns
t_{hold}	Hold Time	0.8	–	0.8	–	0.8	–	ns
f_{tog}	Toggle Frequency	250	–	250	–	250	–	MHz

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

APPLICATION INFORMATION

The MC10H131 is a dual master–slave type D flip–flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable ($\overline{CE}$) inputs. Each flip–flop may be clocked separately by holding the common clock in the new low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip–flop, the Clock Enable inputs must be in the low state.

In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip–flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

MC10H135

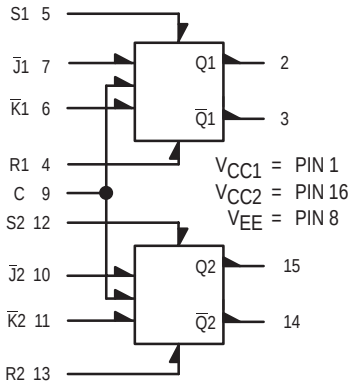
Dual J-K Master-Slave Flip-Flop

The MC10H135 is a dual J–K master–slave flip–flop. The device is provided with an asynchronous set(s) and reset(R). These set and reset inputs overide the clock.

A common clock is provided with separate $\overline{J}$–$\overline{K}$ inputs. When the clock is static, the $\overline{JK}$ inputs do not effect the output. The output states of the flip flop change on the positive transition of the clock.

- Propagation delay, 1.5 ns Typical
- Power Dissipation, 280 mW Typical/Pkg. (No Load)
- f_{tog} 250 MHz Max
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



RS TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

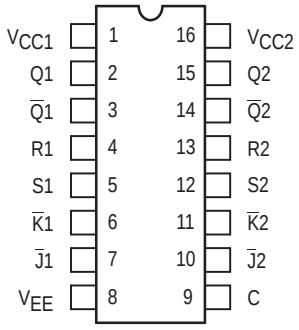
N.D. = Not Defined

CLOCK J–K TRUTH TABLE*

$\overline{J}$	$\overline{K}$	Q_{n+1}
L	L	$\overline{Q_n}$
H	L	L
L	H	H
H	H	Q_n

*Output states change on positive transition of clock for $\overline{J}$–$\overline{K}$ input condition present.

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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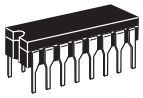
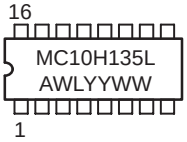
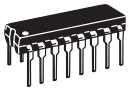
MARKING DIAGRAMS

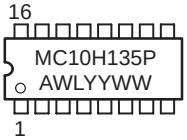


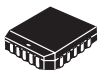
CDIP–16
L SUFFIX
CASE 620



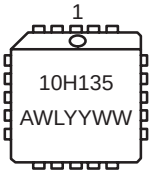


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H135L	CDIP–16	25 Units/Rail
MC10H135P	PDIP–16	25 Units/Rail
MC10H135FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	75	–	68	–	75	mA
I_{inH}	Input Current High Pins 6, 7, 10, 11 Pins 4, 5, 12, 13 Pin 9	 – – –	 460 800 675	 – – –	 285 500 420	 – – –	 285 500 420	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay Set, Reset, Clock	0.7	2.6	0.7	2.6	0.7	2.6	ns
t_r	Rise Time	0.7	2.2	0.7	2.2	0.7	2.2	ns
t_f	Fall Time	0.7	2.2	0.7	2.2	0.7	2.2	ns
t_{set}	Set–up Time	1.5	–	1.5	–	1.5	–	ns
t_{hold}	Hold Time	1.0	–	1.0	–	1.0	–	ns
f_{tog}	Toggle Frequency	250	–	250	–	250	–	MHz

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

MC10H136

Universal Hexadecimal Counter

The MC10H136 is a high speed synchronous hexadecimal counter. This 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in counting frequency and no increase in power-supply current.

- Counting Frequency, 250 MHz Minimum
- Power Dissipation, 625 mW Typical
- Improved Noise Margin 150 mV
  (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

FUNCTION SELECT TABLE

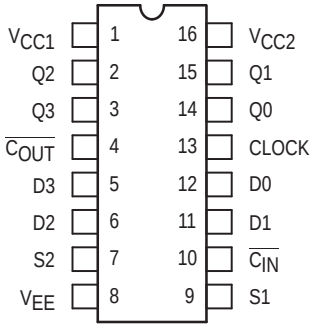
$\overline{CIN}$	S1	S2	Operating Mode
X	L	L	Preset (Program)
L	L	H	Increment (Count Up)
H	L	H	Hold Count
L	H	L	Decrement (Count Down)
H	H	L	Hold Count
X	H	H	Hold (Stop Count)

SEQUENTIAL TRUTH TABLE *

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	L	L	H	H	X	H	L	L	H	H	L
L	H	X	X	X	X	L	H	H	L	H	H	H
L	H	X	X	X	X	L	H	L	H	H	H	H
L	H	X	X	X	X	L	H	H	H	H	H	L
L	H	X	X	X	X	H	L	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H
H	H	X	X	X	X	X	H	H	H	H	H	H
L	L	H	H	L	L	X	H	H	H	L	L	L
H	L	X	X	X	X	L	H	L	H	L	L	H
H	L	X	X	X	X	L	H	H	L	L	L	H
H	L	X	X	X	X	L	H	L	L	L	L	L
H	L	X	X	X	X	L	H	H	H	H	H	L

* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.
** A clock H is defined as a clock input transition from a low to a high logic level.

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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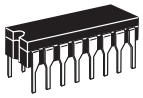
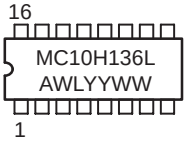
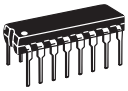
MARKING DIAGRAMS

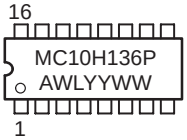


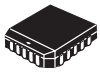
CDIP–16
L SUFFIX
CASE 620



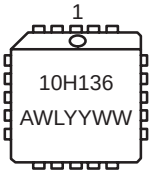


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H136L	CDIP–16	25 Units/Rail
MC10H136P	PDIP–16	25 Units/Rail
MC10H136FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

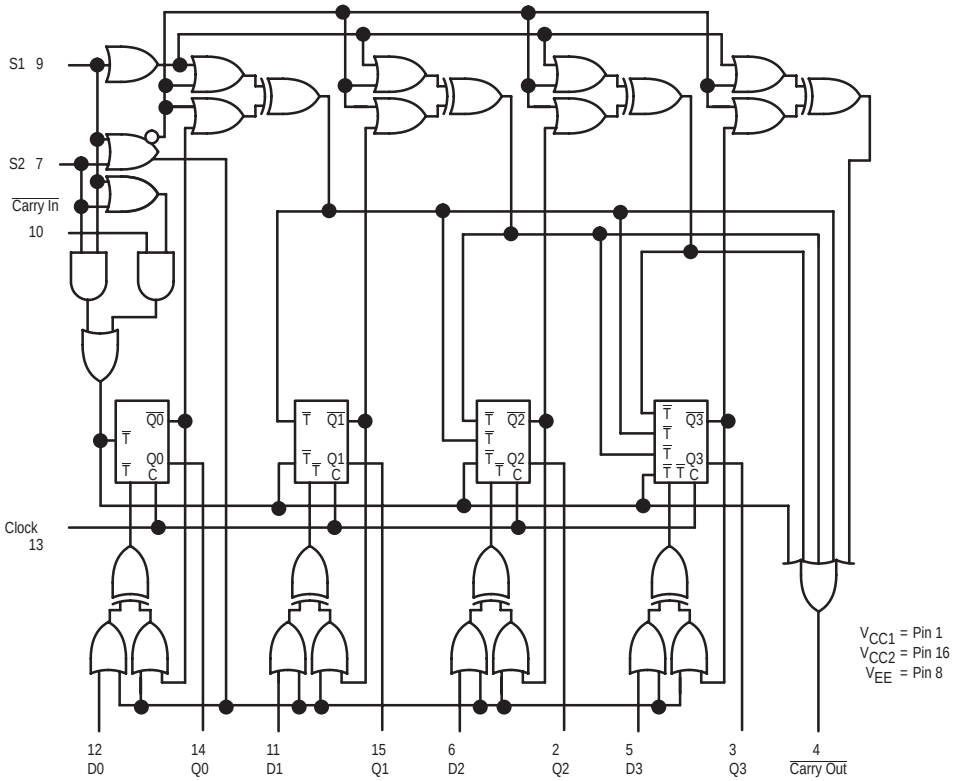
		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	165	–	150	–	165	mA
I_{inH}	Input Current High							µA
	Pins 5, 6, 11, 12, 13	–	430	–	275	–	275	
	Pin 9	–	670	–	420	–	420	
	Pin 7	–	535	–	335	–	335	
	Pin 10	–	380	–	240	–	240	
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay							ns
	Clock to Q	0.7	2.3	0.7	2.4	0.7	2.5	
	Clock to Carry Out	1.0	4.8	1.0	4.9	1.0	5.0	
	Carry in to Carry Out	0.7	2.5	0.7	2.6	0.7	2.7	
t_{set}	Set-up Time							ns
	Data (D0 to C)	2.0	–	2.0	–	2.0	–	
	Select (S to C)	3.5	–	3.5	–	3.5	–	
	Carry In (C_{in} to C)	2.0	–	2.0	–	2.0	–	
	(C to C_{in})	0	–	0	–	0	–	
t_{hold}	Hold Time							ns
	Data (C to D0)	0	–	0	–	0	–	
	Select (C to S)	–0.5	–	–0.5	–	–0.5	–	
	Carry In (C to C_{in})	0	–	0	–	0	–	
	(C_{in} to C)	2.2	–	2.2	–	2.2	–	
f_{count}	Counting Frequency	250	–	250	–	250	–	MHz
t_r	Rise Time	0.5	2.3	0.5	2.4	0.5	2.5	ns
t_f	Fall Time	0.5	2.3	0.5	2.4	0.5	2.5	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts.

LOGIC DIAGRAM



NOTE: FLIP-FLOPS WILL TOGGLE WHEN ALL $\overline{T}$ INPUTS ARE LOW.

APPLICATION INFORMATION

The MC10H136 is a high speed synchronous counter that operates at 250 MHz. Counter operating modes include count up, count down, pre-set and hold count. This device allows the designer to use one basic counter for many applications.

The S1, S2, control lines determine the operating modes of the counter. In the pre-set mode, a clock pulse is necessary to load the counter with the information present on the data inputs (D0, D1, D2, and D3). Carry out goes low on the terminal count or when the counter is being pre-set.

MC10H141

Four-Bit Universal Shift Register

The MC10H141 is a four–bit universal shift register. This device is a functional/pinout duplication of the standard MECL 10K part with 100% improvement in propagation delay and operation frequency and no increase in power supply current.

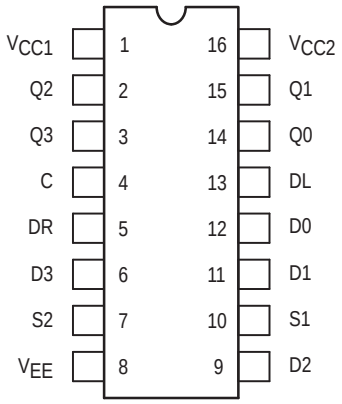
- Shift frequency, 250 MHz Min
- Power Dissipation, 425 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

TRUTH TABLE

SELECT		OPERATING MODE	OUTPUTS			
S1	S2		$Q0_{n+1}$	$Q1_{n+1}$	$Q2_{n+1}$	$Q3_{n+1}$
L	L	Parallel Entry	D0	D1	D2	D3
L	H	Shift Right*	$Q1_n$	$Q2_n$	$Q3_n$	DR
H	L	Shift Left*	DL	$Q0_n$	$Q1_n$	$Q2_n$
H	H	Stop Shift	$Q0_n$	$Q1_n$	$Q2_n$	32_n

* Outputs as exist after pulse appears at “C” input with input conditions as shown (Pulse Positive transition of clock input).

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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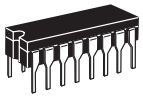
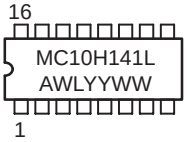
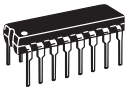
MARKING DIAGRAMS

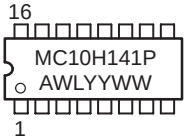


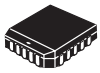
CDIP–16
L SUFFIX
CASE 620





PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H141L	CDIP–16	25 Units/Rail
MC10H141P	PDIP–16	25 Units/Rail
MC10H141FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%, See Note 1.)

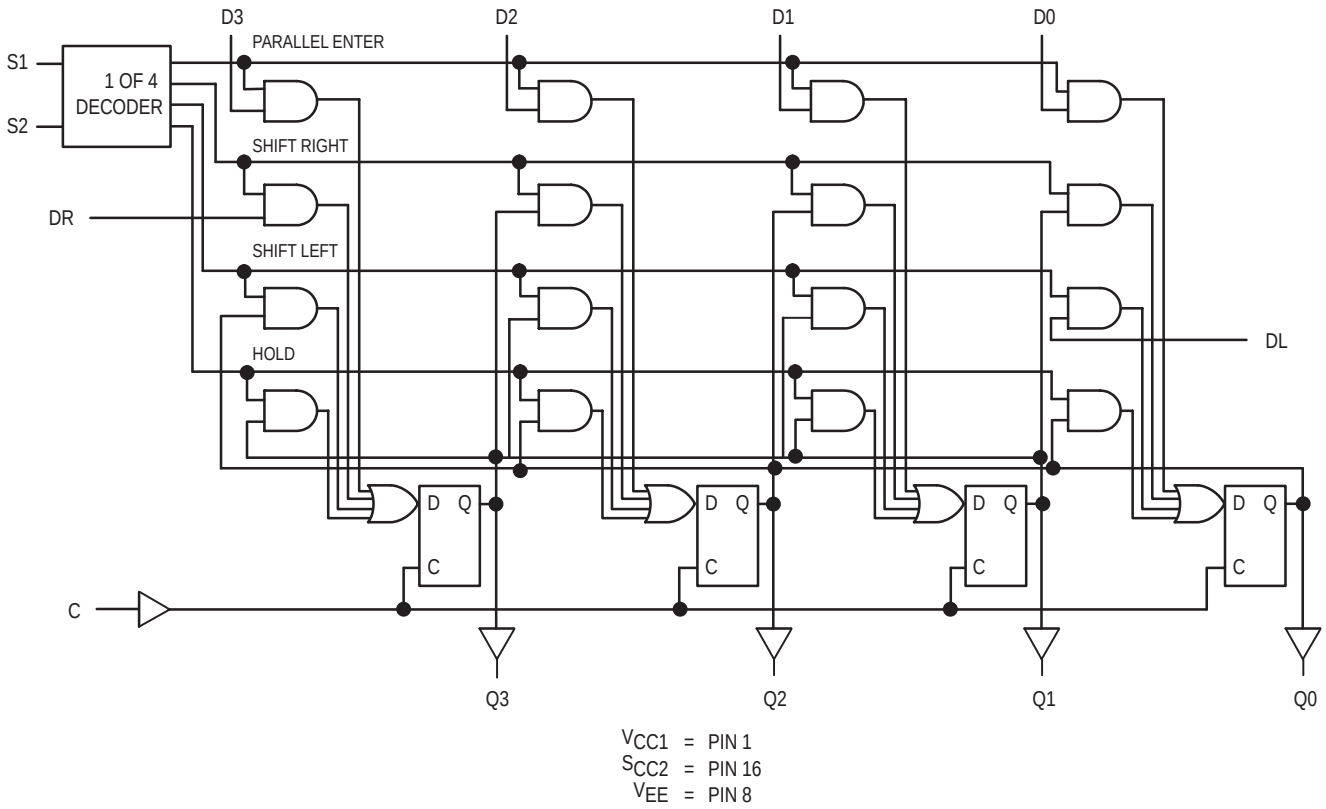
		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	112	–	102	–	112	mA
I_{inH}	Input Current High Pins 5,6,9,11,12,13 Pins 7,10 Pin 4	 – – –	 405 416 510	 – – –	 255 260 320	 – – –	 255 260 320	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay	1.0	2.0	1.0	2.0	1.1	2.1	ns
t_{hold}	Hold Time – Data, Select	1.0	–	1.0	–	1.0	–	ns
t_{set}	Set–up Time Data Select	 1.5 3.0	 – –	 1.5 3.0	 – –	 1.5 3.0	 – –	ns
t_r	Rise Time	0.5	2.4	0.5	2.4	0.5	2.4	ns
t_f	Fall Time	0.5	2.4	0.5	2.4	0.5	2.4	ns
f_{shift}	Shift Frequency	250	–	250	–	250	–	MHz

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 ohm resistor to –2.0 volts.

LOGIC DIAGRAM



APPLICATION INFORMATION

The MC10H141 is a four–bit universal shift register which performs shift left, or shift right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control the four possible operations of the register without external gating of the clock. The flip–flops shift information on the positive edge of the clock. The four operations are stop shift, shift left, shift right, and parallel entry of data. The other six inputs are all data type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR).

MC10H158

Quad 2-Input Multiplexer

(Non–Inverting)

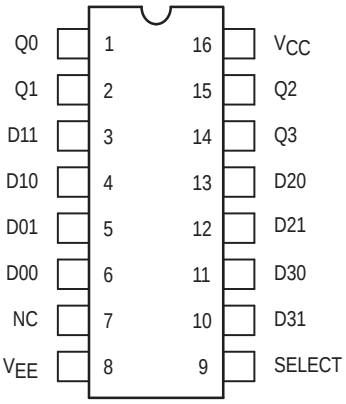
The MC10H158 is a quad two channel multiplexer with common input select. A “high” level select enables input D00, D10, D20 and D30 and a “low” level select enables input D01, D11, D21 and D31. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power–supply current.

- Propagation Delay, 1.5 ns Typical
- Power Dissipation, 197 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

TRUTH TABLE

Select	D0	D1	Q
L	X	L	L
L	X	H	H
H	L	X	L
H	H	X	H

DIP
PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ON Semiconductor

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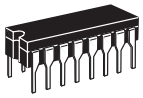
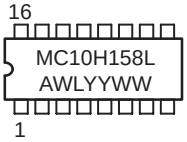
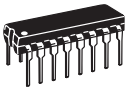
MARKING DIAGRAMS

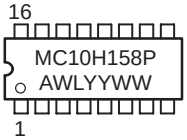


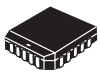
CDIP–16
L SUFFIX
CASE 620



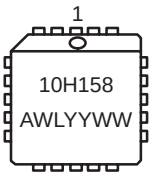


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H158L	CDIP–16	25 Units/Rail
MC10H158P	PDIP–16	25 Units/Rail
MC10H158FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%)

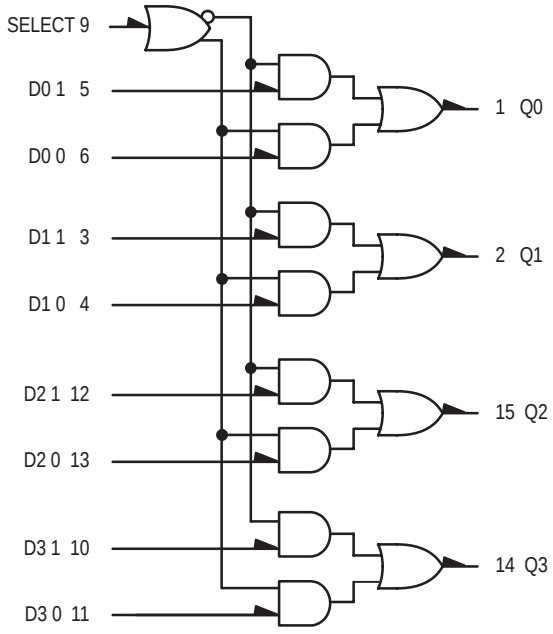
		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	53	–	48	–	53	mA
I_{inH}	Input Current High Pin 9 Pins 3–6 and 10–13	 – –	 475 515	 – –	 295 320	 – –	 295 320	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay Data Select	 0.5 1.0	 1.9 2.9	 0.5 1.0	 1.9 2.9	 0.5 1.0	 2.0 2.9	ns
t_r	Rise Time	0.7	2.2	0.7	2.2	0.7	2.2	ns
t_f	Fall Time	0.7	2.2	0.7	2.2	0.7	2.2	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

LOGIC DIAGRAM



V_{CC} = PIN 16
V_{EE} = PIN 8

MC10H159

Quad 2-Input Multiplexer

(Inverting)

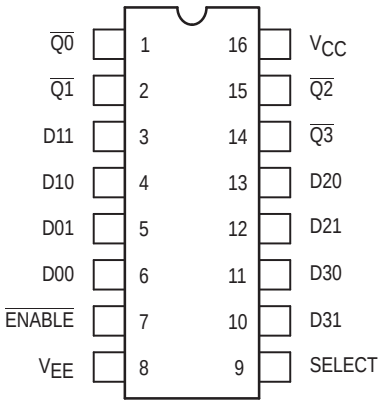
The MC10H159 is a quad 2–input multiplexer with enable. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power–supply current.

- Propagation Delay, 1.5 ns Typical
- Power Dissipation, 218 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

TRUTH TABLE

$\overline{\text{Enable}}$	Select	D0	D1	Q
L	L	X	L	H
L	L	X	H	L
L	H	L	X	H
L	H	H	X	L
H	X	X	X	L

DIP
PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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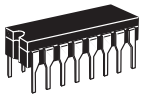
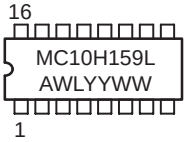
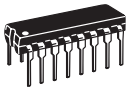
MARKING DIAGRAMS

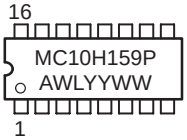


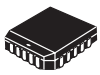
CDIP–16
L SUFFIX
CASE 620



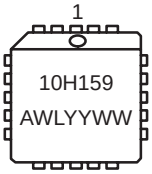


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H159L	CDIP–16	25 Units/Rail
MC10H159P	PDIP–16	25 Units/Rail
MC10H159FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	58	–	53	–	58	mA
I_{inH}	Input Current High Pin 9 Pins 3–7 and 10–13	 – –	 475 515	 – –	 295 320	 – –	 295 320	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

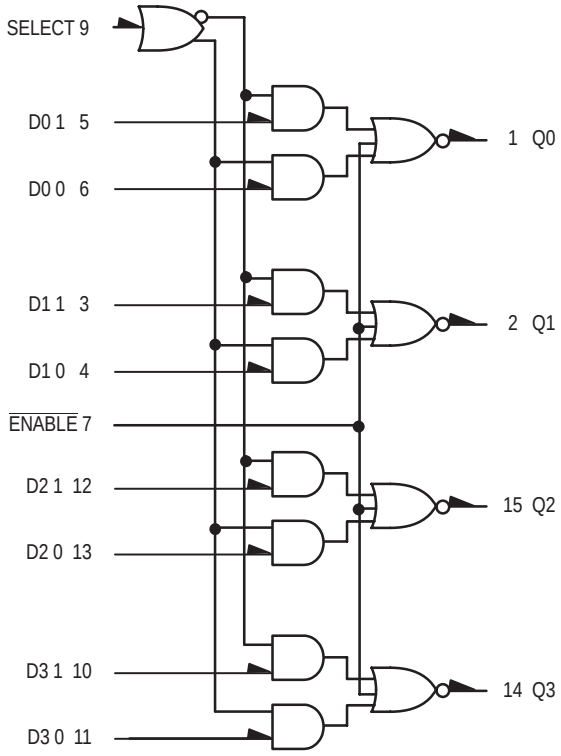
t_{pd}	Propagation Delay Data Select Enable	 0.5 1.0 1.0	 2.2 3.2 3.2	 0.5 1.0 1.0	 2.2 3.2 3.2	 0.5 1.0 1.0	 2.2 3.2 3.2	ns
t_r	Rise Time	0.5	2.2	0.5	2.2	0.5	2.2	ns
t_f	Fall Time	0.5	2.2	0.5	2.2	0.5	2.2	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

APPLICATION INFORMATION

The MC10H159 is a quad two channel multiplexer with enable. It incorporates common enable and common data select inputs. The select input determines which data inputs are enabled. A high (H) level enables data inputs D0 0, D1 0, D2 0, and D3 0. A low (L) level enables data inputs D0 1, D1 1, D2 1, and D3 1. Any change on the data inputs will be reflected at the outputs while the enable is low. Input levels are inverted at the output.

LOGIC DIAGRAM



V_{CC} PIN 16
V_{EE} PIN 8

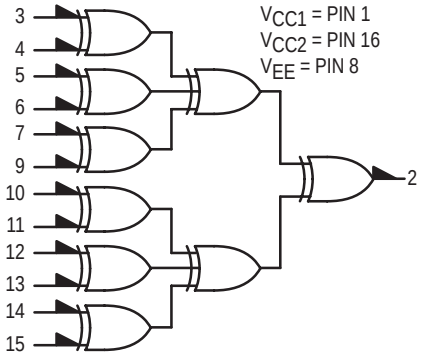
MC10H160

12-Bit Parity Generator-Checker

The MC10H160 is a 12–bit parity generator–checker. The output goes high when an odd number of inputs are high providing the odd parity function. Unconnected inputs are pulled to a logic low allowing parity detection and generation for less than 12 bits. The MC10H160 is a functional pin duplication of the standard 10K family part with 100% improvement in propagation delay and no increase in power–supply current.

- Propagation Delay, 2.5 ns Typical
- Power Dissipation, 320 mW Typical
- Improved Noise Margin 150 mV
  (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

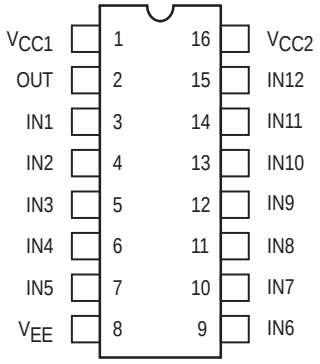
LOGIC DIAGRAM



TRUTH TABLE

INPUT	OUTPUT
Sum of High Level Inputs	Pin 2
Even	Low
Odd	High

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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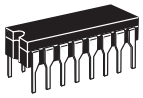
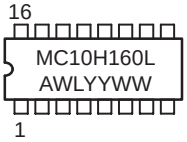
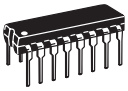
MARKING DIAGRAMS

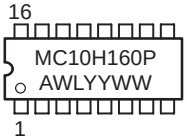


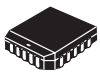
CDIP–16
L SUFFIX
CASE 620



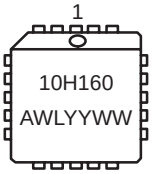


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H160L	CDIP–16	25 Units/Rail
MC10H160P	PDIP–16	25 Units/Rail
MC10H160FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	88	–	78	–	88	mA
I_{inH}	Input Current High Pins 3,5,7,10,12,14 Pins 4,6,9,11,13,15	 – –	 391 457	 – –	 246 285	 – –	 246 285	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay	1.1	3.1	1.1	3.3	1.2	3.5	ns
t_r	Rise Time	0.55	1.5	0.55	1.6	0.75	1.7	ns
t_f	Fall Time	0.55	1.5	0.55	1.6	0.75	1.7	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

MC10H161

Binary to 1-8 Decoder (Low)

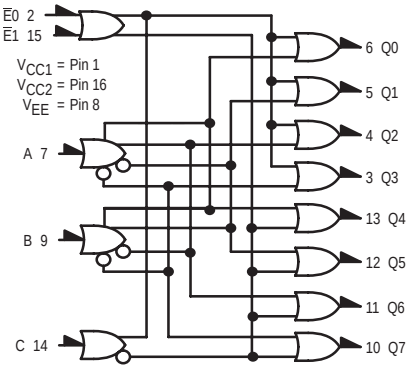
The MC10H161 provides parallel decoding of a three bit binary word to one of eight lines. The MC10H161 is useful in high–speed multiplexer/demultiplexer applications.

The MC10H161 is designed to decode a three bit input word to one of eight output lines. The MC10H161 output will be low when selected while all other output are high. The enable inputs, when either or both are high, force all outputs high.

The MC10H161 is a true parallel decoder. This eliminates unequal parallel path delay times found in other decoder designs. These devices are ideally suited for multiplexer/demultiplexer applications.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation, 315 mW Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

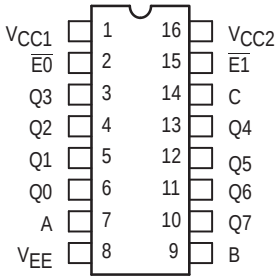
LOGIC DIAGRAM



TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
$\overline{E}1$	$\overline{E}0$	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	H	H	H	H	H	H	H	H

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package. For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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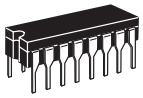
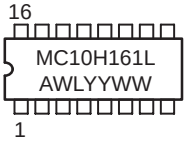
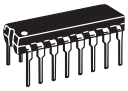
MARKING DIAGRAMS

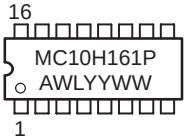


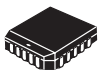
CDIP–16
L SUFFIX
CASE 620





PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H161L	CDIP–16	25 Units/Rail
MC10H161P	PDIP–16	25 Units/Rail
MC10H161FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	84	–	76	–	84	mA
I_{inH}	Input Current High	–	465	–	275	–	275	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

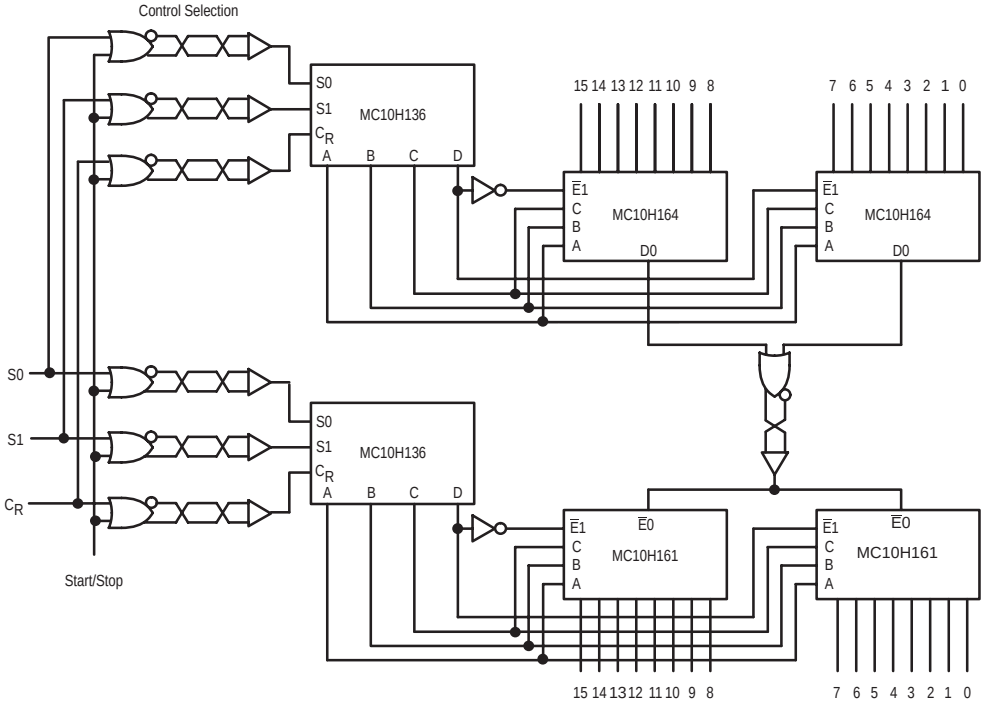
AC PARAMETERS

t_{pd}	Propagation Delay Data Enable	 0.6 0.8	 2.0 2.3	 0.65 0.8	 2.1 2.4	 0.7 0.9	 2.2 2.5	ns
t_r	Rise Time	0.55	1.7	0.65	1.8	0.7	1.9	ns
t_f	Fall Time	0.55	1.7	0.65	1.8	0.7	1.9	ns

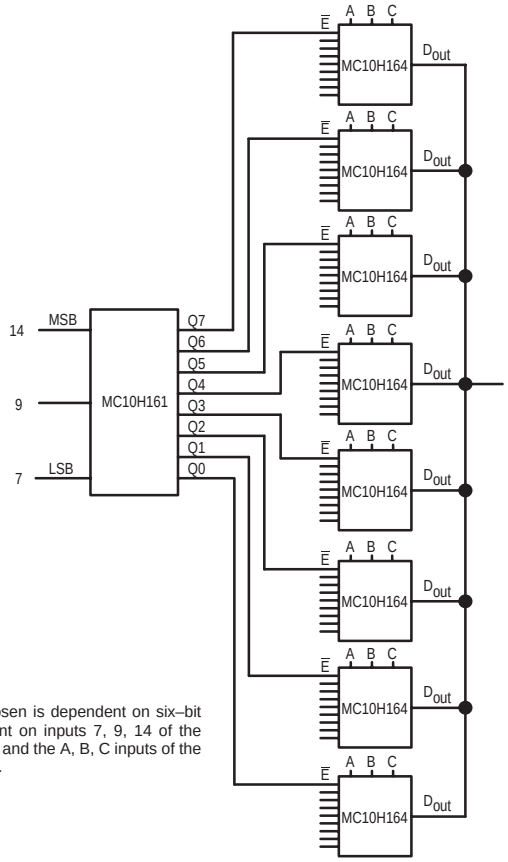
1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

TYPICAL APPLICATIONS

HIGH SPEED 16–BIT MULTIPLEXER/DEMULTIPLEXER



1–OF–64 LINE MULTIPLEXER



The Bit chosen is dependent on six–bit code present on inputs 7, 9, 14 of the MC10H161 and the A, B, C inputs of the MC10H164.

MC10H162

Binary to 1-8 Decoder (High)

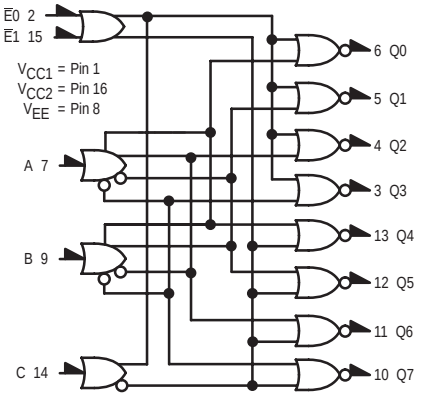
The MC10H162 provides parallel decoding of a three bit binary word to one of eight lines. The MC10H162 is useful in high–speed multiplexer/ demultiplexer applications.

The MC10H162 is designed to decode a three bit input word to one of eight output lines. The MC10H162 output will be high when selected while all other output are low. The enable inputs, when either or both are high, force all outputs low.

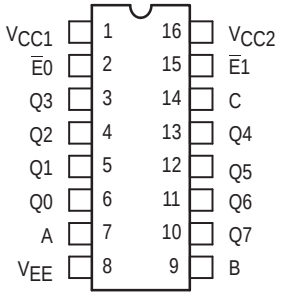
The MC10H162 is a true parallel decoder. This eliminates unequal parallel path delay times found in other decoder designs. These devices are ideally suited for multiplexer/demultiplexer applications.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation, 315 mW Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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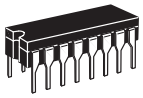
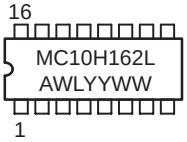
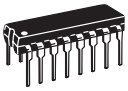
MARKING DIAGRAMS

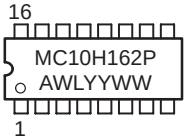


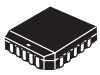
CDIP–16
L SUFFIX
CASE 620



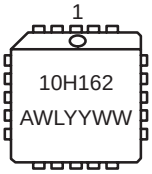


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

TRUTH TABLE

INPUTS					OUTPUTS							
$\overline{E}$0	$\overline{E}$1	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	L	L	L	L	L	L	L	L

ORDERING INFORMATION

Device	Package	Shipping
MC10H162L	CDIP–16	25 Units/Rail
MC10H162P	PDIP–16	25 Units/Rail
MC10H162FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	84	–	76	–	84	mA
I_{inH}	Input Current High	–	465	–	275	–	275	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

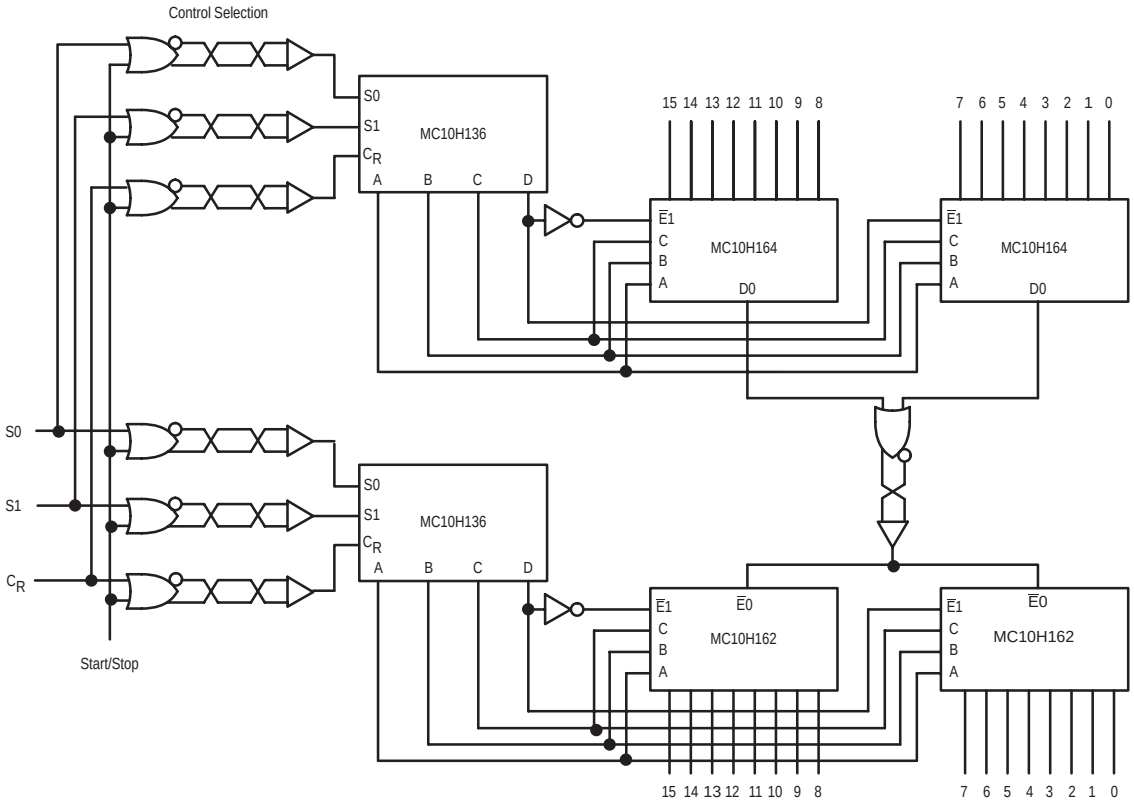
AC PARAMETERS

t_{pd}	Propagation Delay Pins 7, 9, 14 Only Pins 2, 15 Only	 0.7 0.8	 2.0 2.3	 0.7 0.8	 2.1 2.4	 0.8 0.9	 2.5 2.6	ns
t_r	Rise Time	0.6	1.8	0.6	1.9	0.6	2.0	ns
t_f	Fall Time	0.6	1.8	0.6	1.9	0.6	2.0	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

TYPICAL APPLICATIONS

FIGURE 1 – HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER



MC10H164

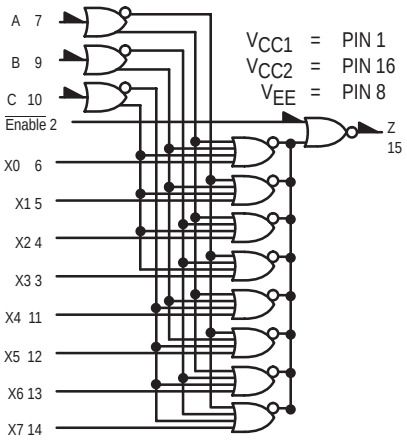
8-Line Multiplexer

The MC10H164 is a MECL 10H part which is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power supply current.

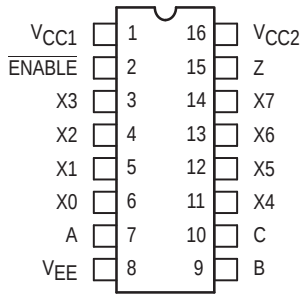
The MC10H164 is designed to be used in data multiplexing and parallel to serial conversion applications. Full parallel gating provides equal delays through any data path. The MC10H164 incorporates an output buffer, eight inputs and an enable. A high on the enable forces the output low. The open emitter output allows the MC10H164 to be connected directly to a data bus. The enable line allows an easy means of expanding to more than 8 lines using additional MC10H164's.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation, 310 mW Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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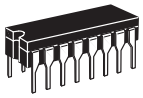
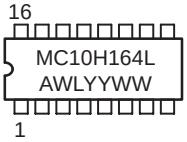
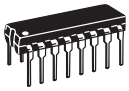
MARKING DIAGRAMS

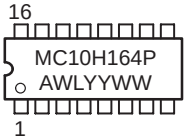


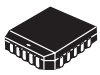
CDIP–16
L SUFFIX
CASE 620





PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

TRUTH TABLE

ENABLE	ADDRESS INPUTS C	B	A	Z
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	L

ORDERING INFORMATION

Device	Package	Shipping
MC10H164L	CDIP–16	25 Units/Rail
MC10H164P	PDIP–16	25 Units/Rail
MC10H164FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	83	–	75	–	83	mA
I_{inH}	Input Current High	–	512	–	320	–	320	μA
I_{inL}	Input Current Low	0.7	–	0.7	–	0.7	–	μA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay							ns
	Enable	0.4	1.45	0.4	1.5	0.5	1.7	
	Data	0.7	2.4	0.8	2.5	0.9	2.6	
	Address	1.0	2.8	1.1	2.9	1.2	3.2	
t_r	Rise Time	0.5	1.5	0.5	1.6	0.5	1.7	ns
t_f	Fall Time	0.5	1.5	0.5	1.6	0.5	1.7	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

TYPICAL APPLICATIONS

FIGURE 1 – HIGH SPEED 16–BIT MULTIPLEXER/DEMULTIPLEXER

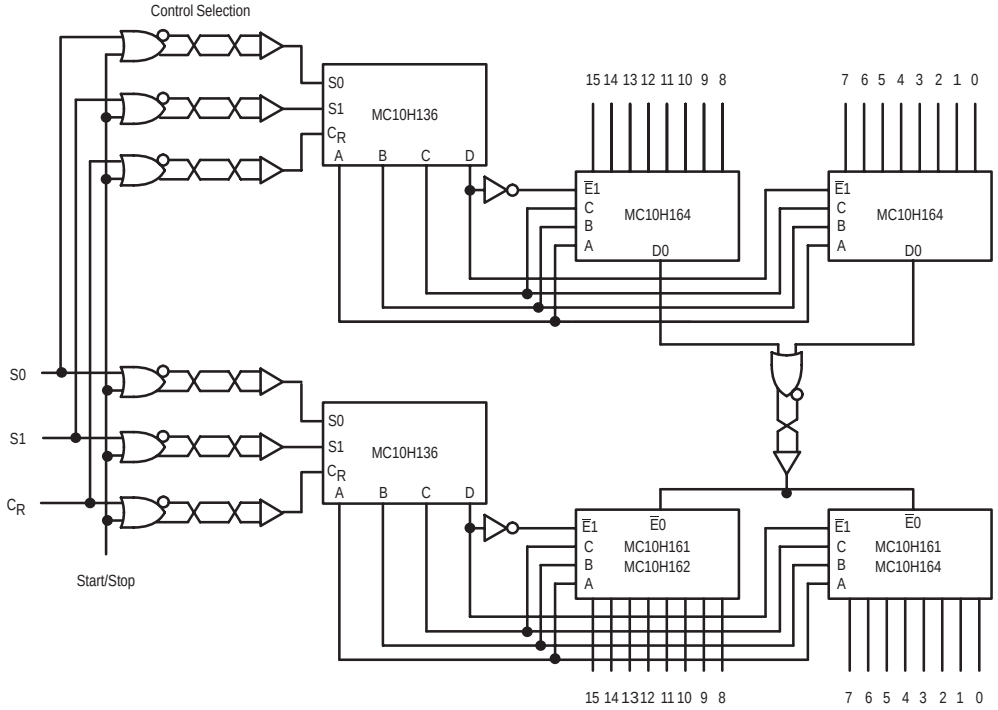
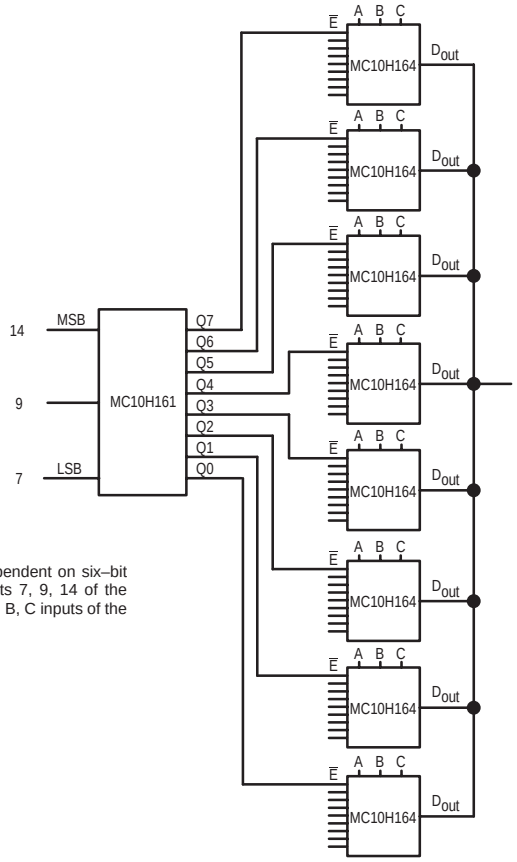


FIGURE 2 – 1–OF–64 LINE MULTIPLEXER



The Bit chosen is dependent on six–bit code present on inputs 7, 9, 14 of the MC10H161 and the A, B, C inputs of the MC10H164.

MC10H165

8-Input Priority Encoder

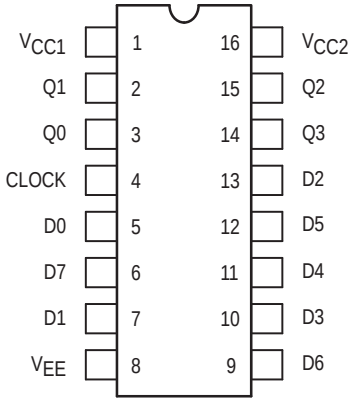
The MC10H165 is an 8–Input Priority Encoder. This 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increases in power–supply current.

- Propagation Delay, Data–to–Output, 2.2 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

TRUTH TABLE

DATA INPUTS								OUTPUTS			
D0	D1	D2	D3	D4	D5	D6	D7	Q3	Q2	Q1	Q0
H	X	X	X	X	X	X	X	H	L	L	L
L	H	X	X	X	X	X	X	H	L	L	H
L	L	H	X	X	X	X	X	H	L	H	L
L	L	L	H	X	X	X	X	H	L	H	H
L	L	L	L	H	X	X	X	H	H	L	L
L	L	L	L	L	H	X	X	H	H	L	H
L	L	L	L	L	L	H	X	H	H	H	L
L	L	L	L	L	L	L	H	L	H	H	L

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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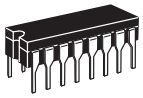
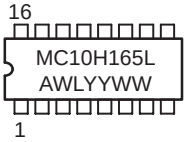
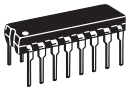
MARKING DIAGRAMS

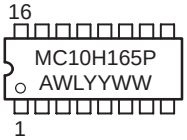


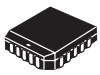
CDIP–16
L SUFFIX
CASE 620



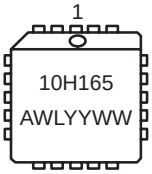


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H165L	CDIP–16	25 Units/Rail
MC10H165P	PDIP–16	25 Units/Rail
MC10H165FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	144	–	131	–	144	mA
I_{inH}	Input Current High Pin 4 Data Inputs	 – –	 510 600	 – –	 320 370	 – –	 320 370	μAdc
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	μA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay Data Input Output Clock Input Output	 0.7 0.7	 3.4 2.2	 0.7 0.7	 3.4 2.2	 0.7 0.7	 3.4 2.2	ns
t_{set}	Set–up Time	3.0	–	3.0	–	3.0	–	ns
t_{hold}	Hold Time	0.5	–	0.5	–	0.5	–	ns
t_r	Rise Time	0.5	2.4	0.5	2.4	0.5	2.4	ns
t_f	Fall Time	0.5	2.4	0.5	2.4	0.5	2.4	ns

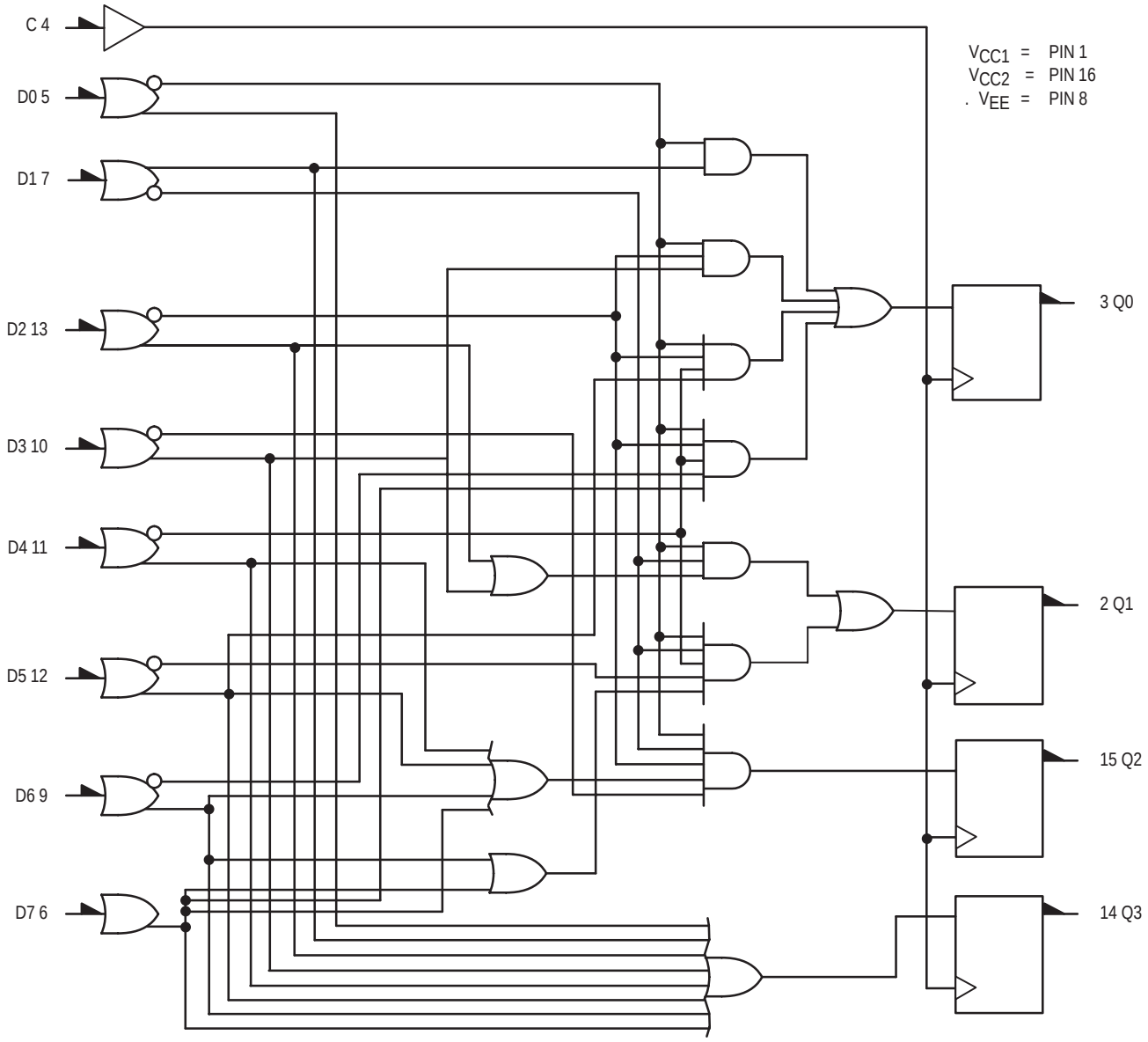
1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

8–INPUT PRIORITY ENCODER

The MC10H165 is a device designed to encode eight inputs to a binary coded output. The output code is that of the highest order input. Any input of lower priority is ignored. Each output incorporates a latch allowing synchronous operation. When the clock is low the outputs follow the inputs and latch when the clock goes high. This device is very useful for a variety of applications in checking system status in control processors, peripheral controllers, and testing systems.

The input is active when high, (e.g., the three binary outputs are low when input D0 is high). The Q3 output is high when any input is high. This allows direct extension into another priority encoder when more than eight inputs are necessary. The MC10H165 can also be used to develop binary codes from random logic inputs, for addressing ROMs, RAMs, or for multiplexing data.

LOGIC DIAGRAM

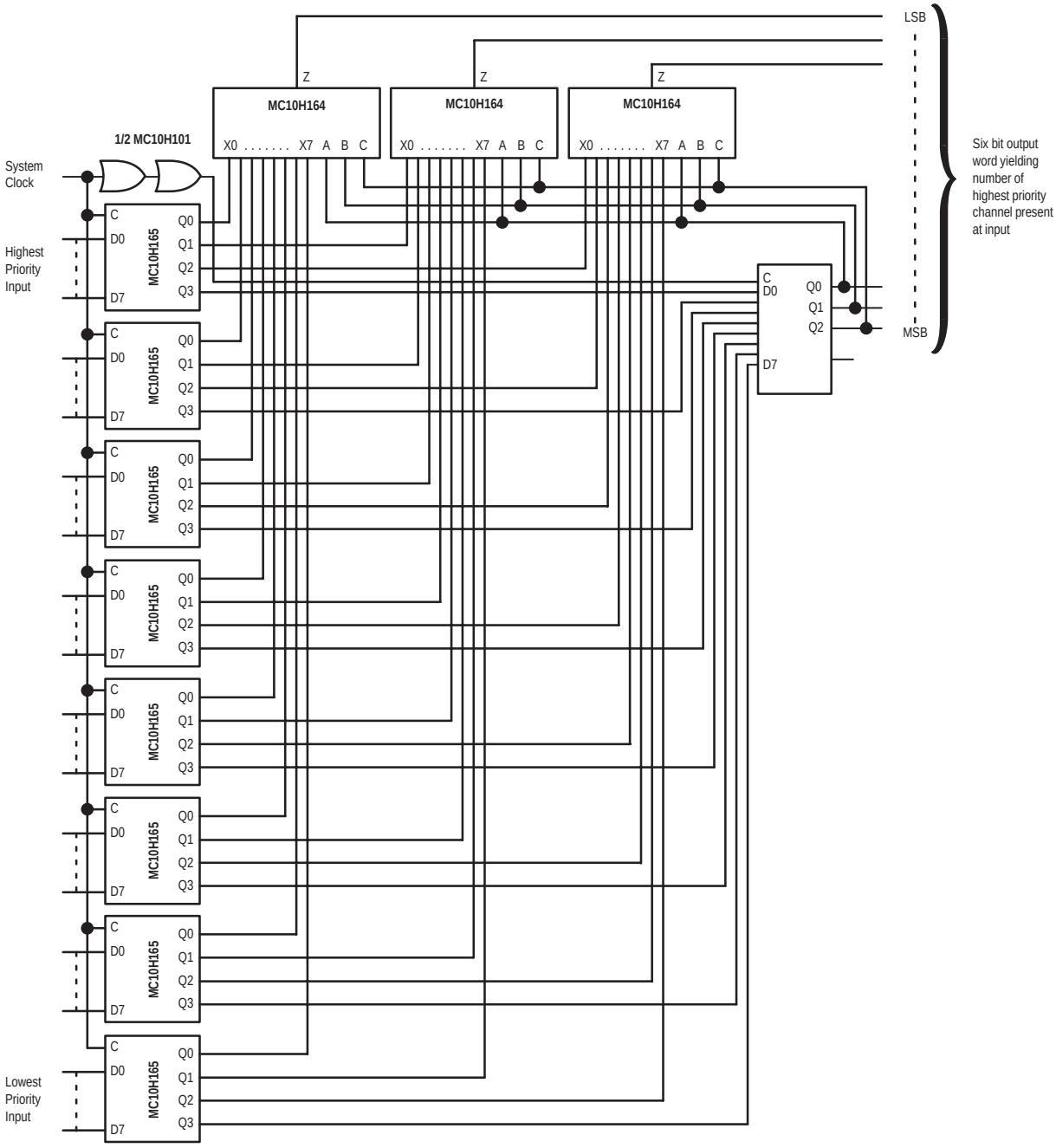


Numbers at ends of terminals denote pin numbers for L and P packages.

APPLICATION INFORMATION

A typical application of the MC10H165 is the decoding of system status on a priority basis. A 64–line priority encoder is shown in the figure below. System status lines are connected to this encoder such that, when a given condition exists, the respective input will be at a logic high level. This scheme will select the one of 64 different system conditions, as represented at the encoder inputs, which has priority in determining the next system operation to be performed. The binary code showing the address of the highest priority input present will appear at the encoder outputs to control other system logic functions.

64–LINE PRIORITY ENCODER



MC10H166

5-Bit Magnitude Comparator

The MC10H166 is a 5–Bit Magnitude Comparator and is a functional/ pinout duplication of the standard MECL 10K part with 100% improvement in propagation delay and no increase in power–supply current.

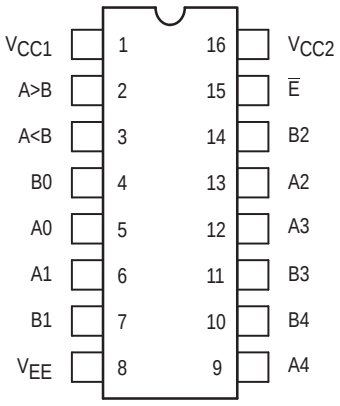
The MC10H166 is a high–speed expandable 5–bit comparator for comparing the magnitude of two binary words. Two outputs are provided: A<B and A>B. The A = B function can be obtained by wire–ORing these outputs (a low level indicates A = B) or by wire–NORing the outputs (a high level indicates A = B). A high level on the enable function forces both outputs low.

- Propagation Delay, Data–to–Output, 2.0 ns Typical
- Power Dissipation 440 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

TRUTH TABLE

Inputs			Outputs	
$\overline{E}$	A	B	A < B	A > B
H	X	X	L	L
L	WORD A = WORD B		L	L
L	WORD A > WORD B		L	H
L	WORD A < WORD B		H	L

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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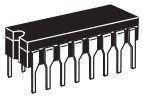
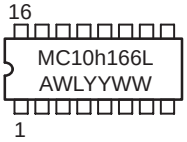
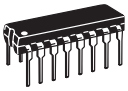
MARKING DIAGRAMS

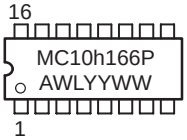


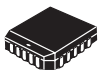
CDIP–16
L SUFFIX
CASE 620



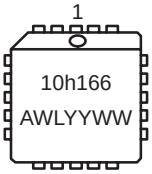


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10h166L	CDIP–16	25 Units/Rail
MC10h166P	PDIP–16	25 Units/Rail
MC10h166FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	117	–	106	–	117	mA
I_{inH}	Input Current High	–	350	–	220	–	220	μA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	μA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay Data–to–Output Enable–to–Output	 1.1 0.6	 3.5 1.7	 1.1 0.7	 3.7 1.7	 1.2 0.7	 4.1 1.8	ns
t_r	Rise Time	0.6	1.5	0.6	1.6	0.6	1.7	ns
t_f	Fall Time	0.6	1.5	0.6	1.6	0.6	1.7	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

LOGIC DIAGRAM

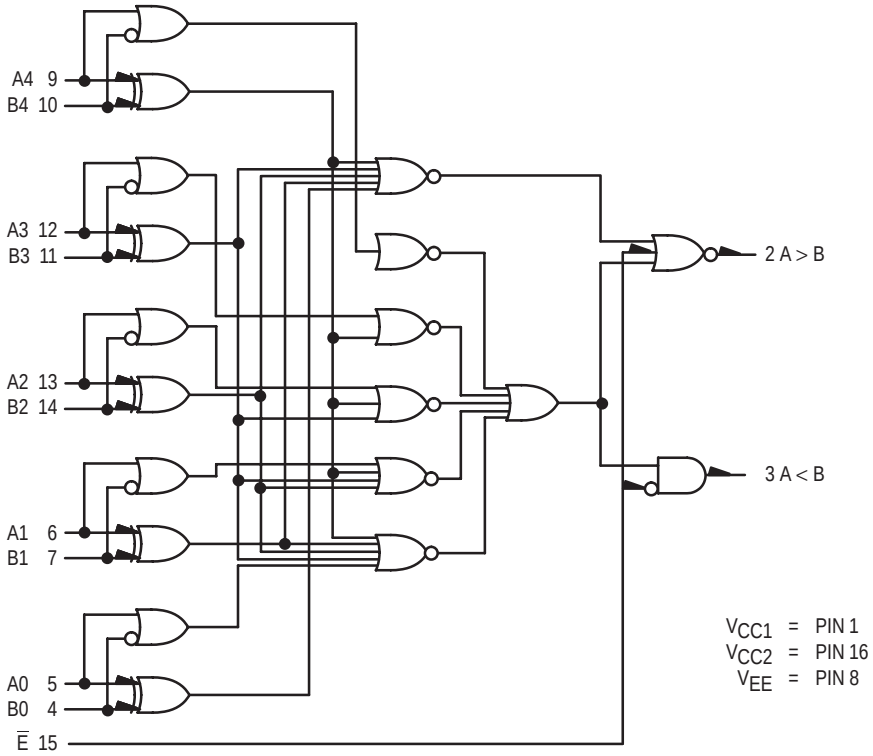
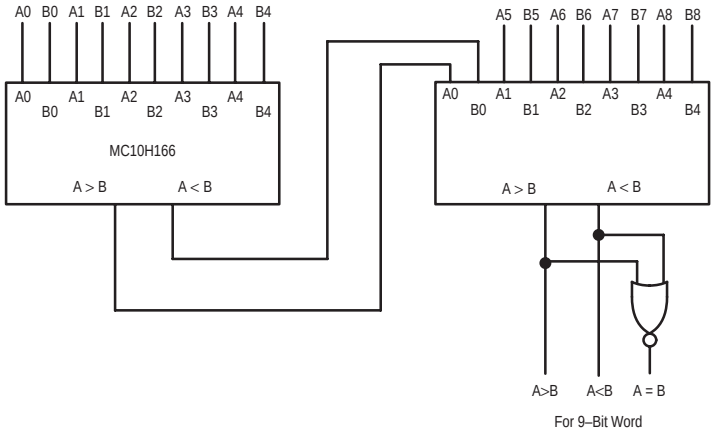
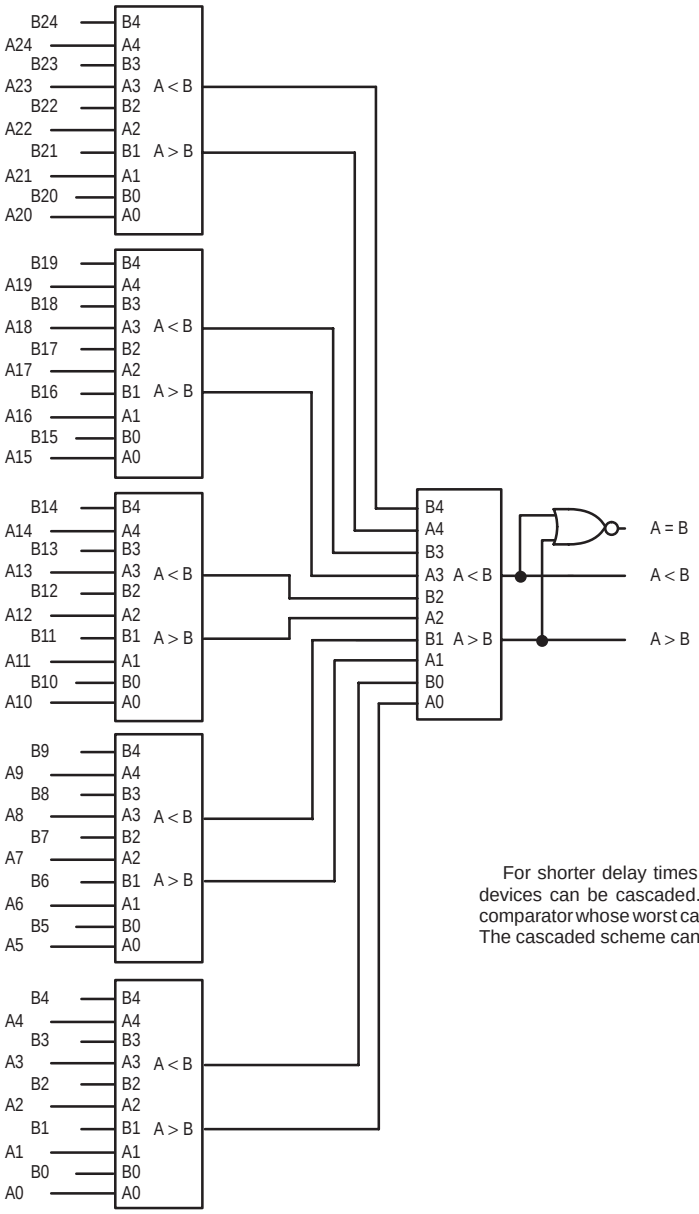


FIGURE 1 – 9–BIT MAGNITUDE COMPARATOR



For longer word lengths, the MC10H166 can be serially expanded or cascaded. Figure 1 shows two devices in a serial expansion for a 9–bit word length. The A > B and A < B outputs are fed to the A0 and B0 inputs respectively of the next device. The connection for an A = B output is also shown. The worst case delay time of serial expansion is equal to the number of comparators times the data–to–output delay.

FIGURE 2 – 25–BIT MAGNITUDE COMPARATOR



For shorter delay times than possible with serial expansion, devices can be cascaded. Figure 2 shows a 25–bit cascaded comparator whose worst case delay is two data–to–output delays. The cascaded scheme can be extended to longer word lengths.

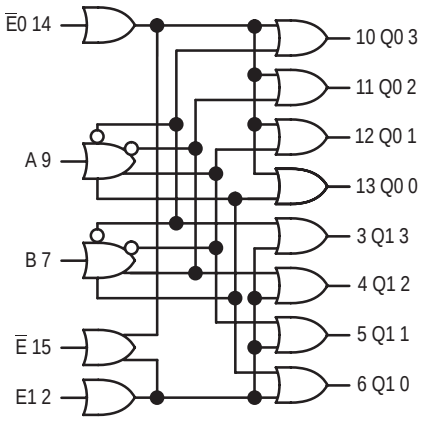
MC10H171

Dual Binary to 1-4 Decoder (Low)

The MC10H171 is a binary coded 2 line to dual 4 line decoder with selected outputs low. With either $\overline{E}0$ or $\overline{E}1$ high, the corresponding selected 4 outputs are high. The common enable $\overline{E}$, when high, forces all outputs high.

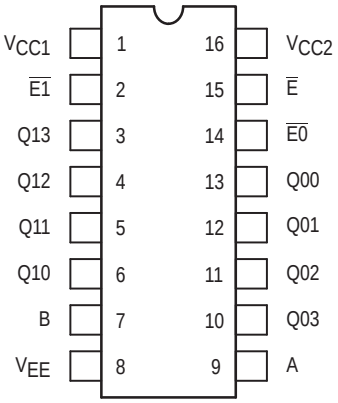
- Propagation Delay, 2 ns Typical
- Power Dissipation 325 mW Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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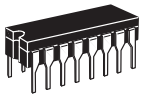
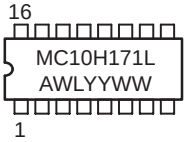
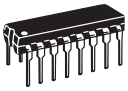
MARKING DIAGRAMS

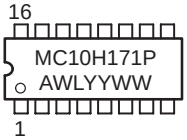


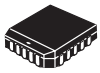
CDIP–16
L SUFFIX
CASE 620





PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H171L	CDIP–16	25 Units/Rail
MC10H171P	PDIP–16	25 Units/Rail
MC10H171FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	85	–	77	–	85	mA
I_{inH}	Input Current High	–	425	–	265	–	265	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
t_{pd}	Propagation Delay							ns
	Data	0.5	2.0	0.5	2.1	0.5	2.2	
	Select	0.5	2.6	0.5	2.7	0.5	2.8	
t_r	Rise Time	0.5	1.7	0.5	1.8	0.5	1.9	ns
t_f	Fall Time	0.5	1.7	0.5	1.8	0.5	1.9	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

TRUTH TABLE

Enable Inputs			Inputs		Outputs							
$\overline{E}$	$\overline{E}$0	$\overline{E}$1	A	B	Q10	Q11	Q12	Q13	Q00	Q01	Q02	Q03
L	L	L	L	L	L	H	H	H	L	H	H	H
L	L	L	L	H	H	L	H	H	H	L	H	H
L	L	L	H	L	H	H	L	H	H	H	L	H
L	L	L	H	H	H	H	H	L	H	H	H	L
L	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	L	L	L	H	H	H	H	H	H	H
H	X	X	X	X	H	H	H	H	H	H	H	H

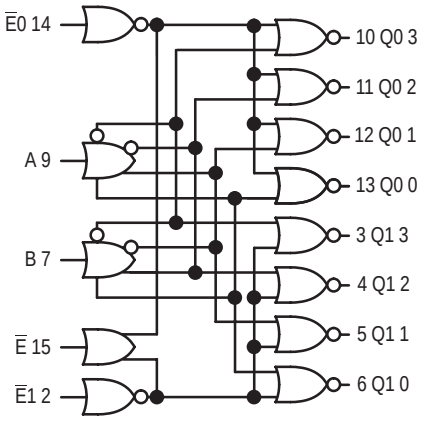
MC10H172

Dual Binary to 1-4-Decoder (High)

The MC10H172 is a binary coded 2 line to dual 4 line decoder with selected outputs high. With either $\overline{E}0$ or $\overline{E}1$ low, the corresponding selected 4 outputs are low. The common enable $\overline{E}$, when high, forces all outputs low.

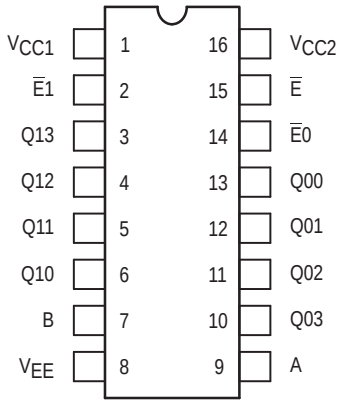
- Propagation Delay, 2 ns Typical
- Power Dissipation 325 mW Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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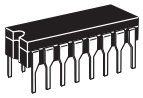
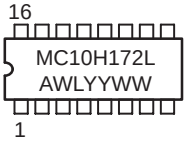
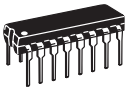
MARKING DIAGRAMS

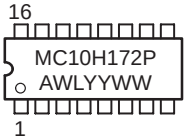


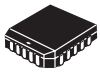
CDIP–16
L SUFFIX
CASE 620



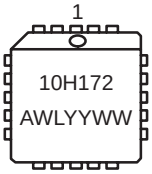


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H172L	CDIP–16	25 Units/Rail
MC10H172P	PDIP–16	25 Units/Rail
MC10H172FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	85	–	77	–	85	mA
I_{inH}	Input Current High	–	425	–	265	–	265	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
t_{pd}	Propagation Delay							ns
	Data	0.5	2.0	0.5	2.1	0.5	2.2	
	Select	0.5	2.6	0.5	2.7	0.5	2.8	
t_r	Rise Time	0.5	1.7	0.5	1.8	0.5	1.9	ns
t_f	Fall Time	0.5	1.7	0.5	1.8	0.5	1.9	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

TRUTH TABLE

Enable Inputs			Inputs		Outputs							
$\overline{E}$	$\overline{E}$1	$\overline{E}$0	A	B	Q1 0	Q1 1	Q1 2	Q1 3	Q0 0	Q0 1	Q0 2	Q0 3
L	H	H	L	L	H	L	L	L	H	L	L	L
L	H	H	L	H	L	H	L	L	L	H	L	L
L	H	H	H	L	L	L	H	L	L	L	H	L
L	H	H	H	H	L	L	L	H	L	L	L	H
L	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	L	L	H	L	L	L	L	L	L	L
H	X	X	X	X	L	L	L	L	L	L	L	L

X = Don't Care

MC10H173

Quad 2-Input Multiplexer/ Latch

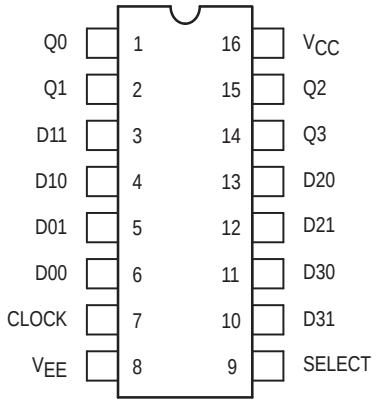
The MC10H173 is a quad 2–input multiplexer with latch. This device is a functional/pinout duplication of the standard MECL 10K part, with 100% improvement in propagation delay and no increase in power supply current.

- Data Propagation Delay, 1.5 ns Typical
- Power Dissipation, 275 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K–Compatible

TRUTH TABLE

SELECT	CLOCK	$Q0_{n+1}$
H	L	D00
L	L	D01
X	H	$Q0_n$

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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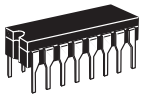
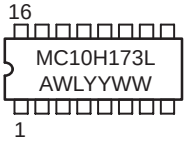
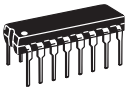
MARKING DIAGRAMS

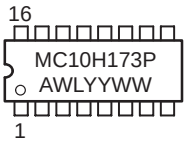


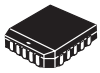
CDIP–16
L SUFFIX
CASE 620



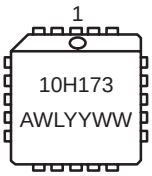


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H173L	CDIP–16	25 Units/Rail
MC10H173P	PDIP–16	25 Units/Rail
MC10H173FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	73	–	66	–	73	mA
I_{inH}	Input Current High Pins 3–7 & 10–13 Pin 9	 – –	 510 475	 – –	 320 300	 – –	 320 300	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

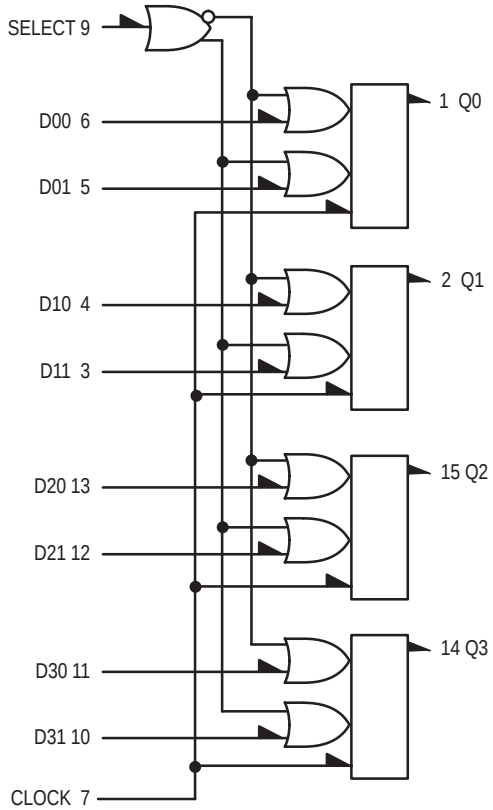
t_{pd}	Propagation Delay Data Clock Select	 0.7 1.0 1.0	 2.3 3.7 3.6	 0.7 1.0 1.0	 2.3 3.7 3.6	 0.7 1.0 1.0	 2.3 3.7 3.6	ns
t_{set}	Set–up Time Data Select	 0.7 1.0	 – –	 0.7 1.0	 – –	 0.7 1.0	 – –	ns
t_{hold}	Hold Time Data Select	 0.7 1.0	 – –	 0.7 1.0	 – –	 0.7 1.0	 – –	ns
t_r	Rise Time	0.7	2.4	0.7	2.4	0.7	2.4	ns
t_f	Fall Time	0.7	2.4	0.7	2.4	0.7	2.4	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

APPLICATION INFORMATION

The MC10173 is a quad two–channel multiplexer with latch. It incorporates common clock and common data select inputs. The select input determines which data input is enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, D31. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

LOGIC DIAGRAM



V_{CC} = PIN 16
V_{EE} = PIN 8

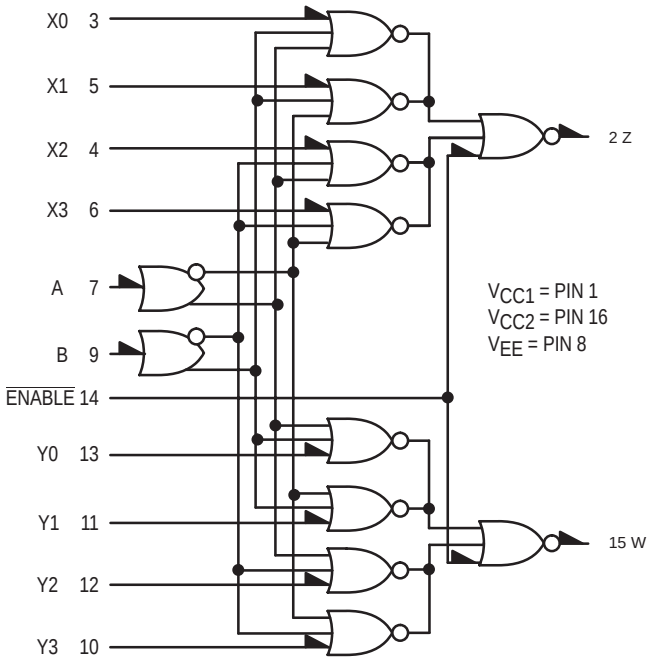
MC10H174

Dual 4 to 1 Multiplexer

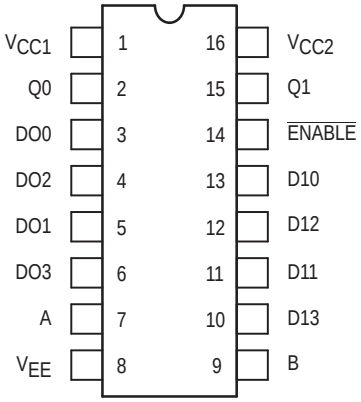
The MC10H174 is a Dual 4–to–1 Multiplexer. This device is a functional/ pinout duplication of the standard MECL 10K part, with 100% improvement in propagation delay and no increase in power supply current.

- Propagation Delay, 1.5 ns Typical
- Power Dissipation, 305 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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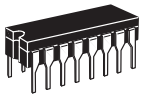
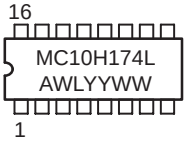
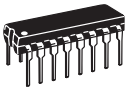
MARKING DIAGRAMS

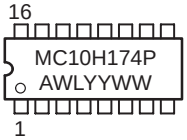


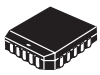
CDIP–16
L SUFFIX
CASE 620





PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

TRUTH TABLE

$\overline{\text{ENABLE}}$	ADDRESS INPUTS		OUTPUTS	
$\overline{E}$	B	A	Z	W
H	X	X	L	L
L	L	L	X0	Y0
L	L	H	X1	Y1
L	H	L	X2	Y2
L	H	H	X3	Y3

ORDERING INFORMATION

Device	Package	Shipping
MC10H174L	CDIP–16	25 Units/Rail
MC10H174P	PDIP–16	25 Units/Rail
MC10H174FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	80	–	73	–	80	mA
I_{inH}	Input Current High Pins 3–7 & 9–13 Pin 14	 – –	 475 670	 – –	 300 420	 – –	 300 420	μAdc
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	μA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay Data Select (A, B) Enable	 0.7 1.0 0.4	 2.4 2.8 1.45	 0.8 1.1 0.4	 2.5 2.9 1.5	 0.9 1.2 0.5	 2.6 3.2 1.7	ns
t_r	Rise Time	0.5	1.5	0.5	1.6	0.5	1.7	ns
t_f	Fall Time	0.5	1.5	0.5	1.6	0.5	1.7	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

MC10H175

Quint Latch

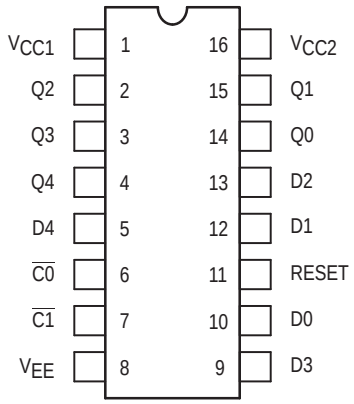
The MC10H175 is a quint D type latch with common reset and clock lines. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power–supply current.

- Propagation Delay, 1.2 ns Typical
- Power Dissipation, 400 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

TRUTH TABLE

D	$\overline{C0}$	$\overline{C1}$	Reset	Q_{n+1}
L	L	L	X	L
H	L	L	X	H
X	H	X	L	Qn
X	X	H	L	Qn
X	H	X	H	L
X	X	H	H	L

DIP
PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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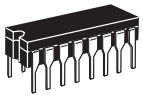
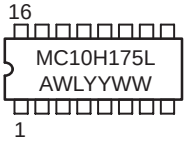
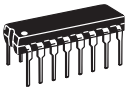
MARKING DIAGRAMS

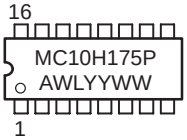


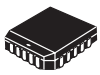
CDIP–16
L SUFFIX
CASE 620



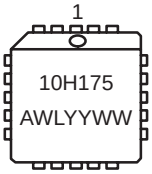


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H175L	CDIP–16	25 Units/Rail
MC10H175P	PDIP–16	25 Units/Rail
MC10H175FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
I_E	Power Supply Current	–	107	–	97	–	107	mA
I_{inH}	Input Current High Pins 5,6,7,9,10,12,13 Pin 11	 – –	 565 1120	 – –	 335 660	 – –	 335 660	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay Data Clock Reset	 0.6 0.7 1.0	 1.6 1.9 2.2	 0.6 0.7 1.0	 1.6 2.0 2.3	 0.6 0.8 1.0	 1.7 2.1 2.4	ns
t_{set}	Set–up Time	1.5	–	1.5	–	1.5	–	ns
t_{hold}	Hold Time	0.8	–	0.8	–	0.8	–	ns
t_r	Rise Time	0.5	1.8	0.5	1.9	0.5	2.0	ns
t_f	Fall Time	0.5	1.8	0.5	1.9	0.5	2.0	ns

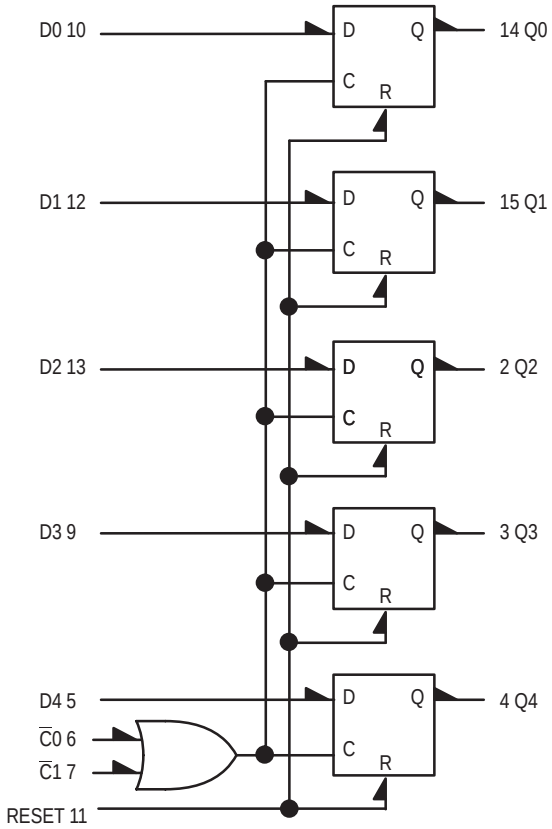
1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

APPLICATION INFORMATION

The MC10H175 is a high speed, low power quint latch. It features five D type latches with common reset and a common two–input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are “OR”ed together.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. **THE RESET INPUT IS ENABLED ONLY WHEN THE CLOCK IS IN THE HIGH STATE**.

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

MC10H176

Hex D Master-Slave Flip-Flop

The MC10H176 contains six master slave type D flip–flops with a common clock. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock frequency and propagation delay and no increase in power–supply current.

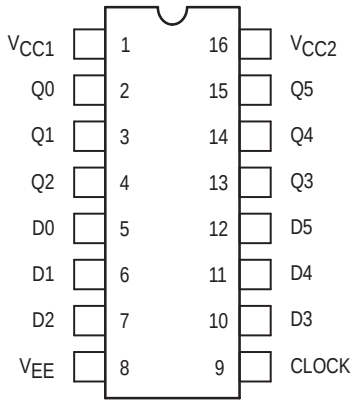
- Propagation Delay, 1.7 ns Typical
- Power Dissipation, 460 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

CLOCKED TRUTH TABLE

C	Q	Q_{n+1}
L	X	Q_n
H *	L	L
H *	H	H

* A clock H is a clock transition from a low to a high state.

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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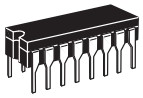
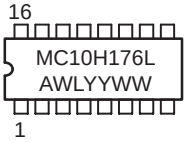
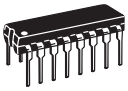
MARKING DIAGRAMS

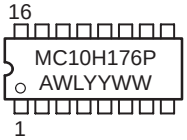


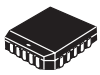
CDIP–16
L SUFFIX
CASE 620



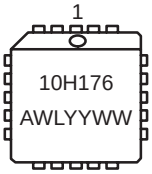


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H176L	CDIP–16	25 Units/Rail
MC10H176P	PDIP–16	25 Units/Rail
MC10H176FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	123	–	112	–	123	mA
I_{inH}	Input Current High Pins 5,6,7,10,11,12 Pin 9	 – –	 425 670	 – –	 265 420	 – –	 265 420	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

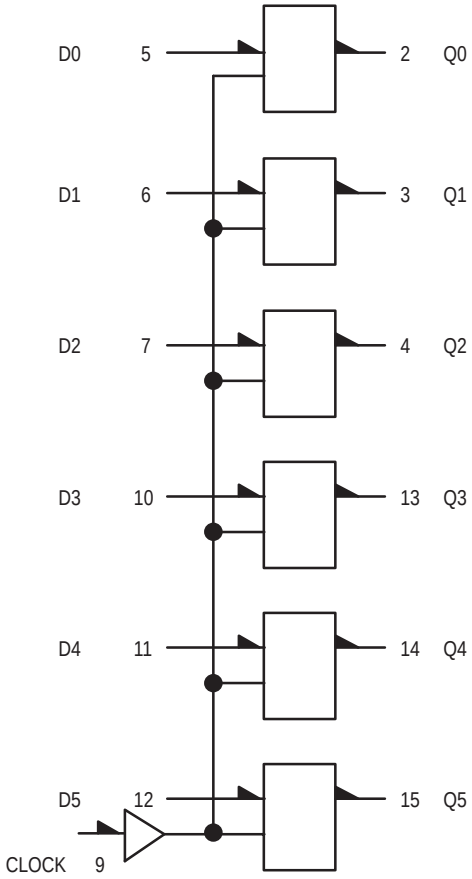
t_{pd}	Propagation Delay	0.9	2.1	0.9	2.2	1.0	2.4	ns
t_{set}	Set–up Time	1.5	–	1.5	–	1.5	–	ns
t_{hold}	Hold Time	0.9	–	0.9	–	1.0	–	ns
t_r	Rise Time	0.5	1.8	0.5	1.9	0.5	2.0	ns
t_f	Fall Time	0.5	1.8	0.5	1.9	0.5	2.0	ns
f_{tog}	Toggle Frequency	250	–	250	–	250	–	MHz

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

APPLICATION INFORMATION

The MC10H176 contains six high–speed, master slave type “D” flip–flops. Data is entered into the master when the clock is low. Master–to–slave data transfer takes place on the positive–going Clock transition. Thus, outputs may change only on a positive–going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master–slave construction of this device.

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

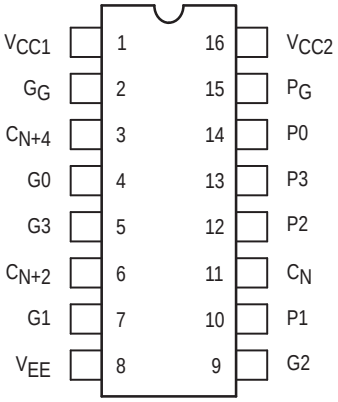
MC10H179

Look-Ahead Carry Block

The MC10H179 is a functional/pinout duplication of the standard MECL 10K part, with 100% improvement in propagation delay and no increase in power supply current.

- Power Dissipation, 300 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

DIP
PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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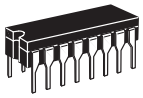
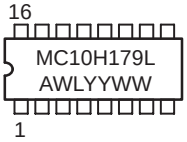
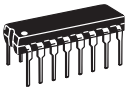
MARKING DIAGRAMS

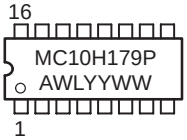


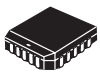
CDIP–16
L SUFFIX
CASE 620



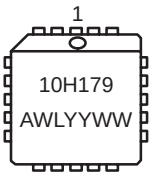


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H179L	CDIP–16	25 Units/Rail
MC10H179P	PDIP–16	25 Units/Rail
MC10H179FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

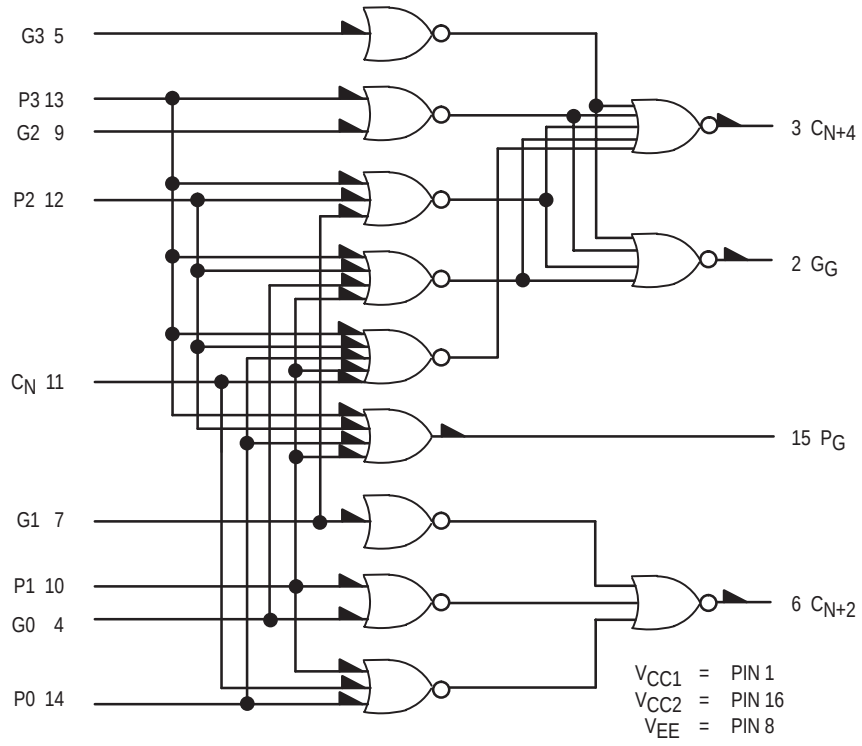
		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	79	–	72	–	79	mA
I_{inH}	Input Current High							μA
	Pins 5 and 9	–	465	–	275	–	275	
	Pins 4, 7 and 11	–	545	–	320	–	320	
	Pin 14	–	705	–	415	–	415	
	Pin 12	–	790	–	465	–	465	
	Pins 10 and 13	–	870	–	510	–	510	
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	μA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay							ns
	P to P_G	0.4	1.4	0.4	1.5	0.5	1.7	
	G, P, C_n to C_n or G_G	0.6	2.3	0.7	2.4	0.8	2.6	
t_r	Rise Time	0.5	1.7	0.5	1.8	0.5	1.9	ns
t_f	Fall Time	0.5	1.7	0.5	1.8	0.5	1.9	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

LOGIC DIAGRAM



P_G = P0 + P1 + P2 + P3

G_G = (G0 + P1 + P2 + P3) (G1 + P2 + P3) (G2 + P3) G3

C_{N+2} = (C_N + P0 + P1) (G0 + P1) G1

C_{N+4} = (C_N + P0 + P1 + P2 + P3) (G0 + P1 + P2 + P3) (G1 + P2 + P3) (G2 + P3) G3

TYPICAL APPLICATIONS

The MC10H179 is a high–speed, low–power, standard MECL complex function that is designed to perform the look–ahead carry function. This device can be used with the MC10H181 4–bit ALU directly, or with the MC10H180 dual arithmetic unit in any computer, instrumentation or digital communication application requiring high speed arithmetic operation on long words.

When used with the MC10H181, the MC10H179 performs a second order or higher look–ahead. Figure 2 shows a 16–bit look–ahead carry arithmetic unit. Second order carry is valuable for longer binary words. As an example, addition of two 32–bit words is improved from 30 nanoseconds with ripple–carry techniques. A block diagram of a 32–bit ALU is shown in Figure 1. The MC10H179 may also be used in many other applications. It can, for example, reduce system package count when used to generate functions of several variables.

FIGURE 1 – 32–BIT ALU WITH CARRY LOOK–AHEAD

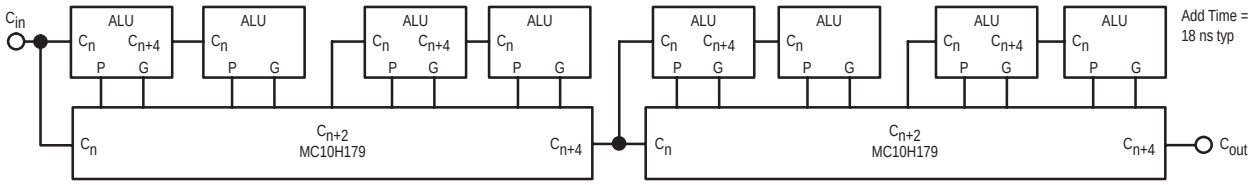
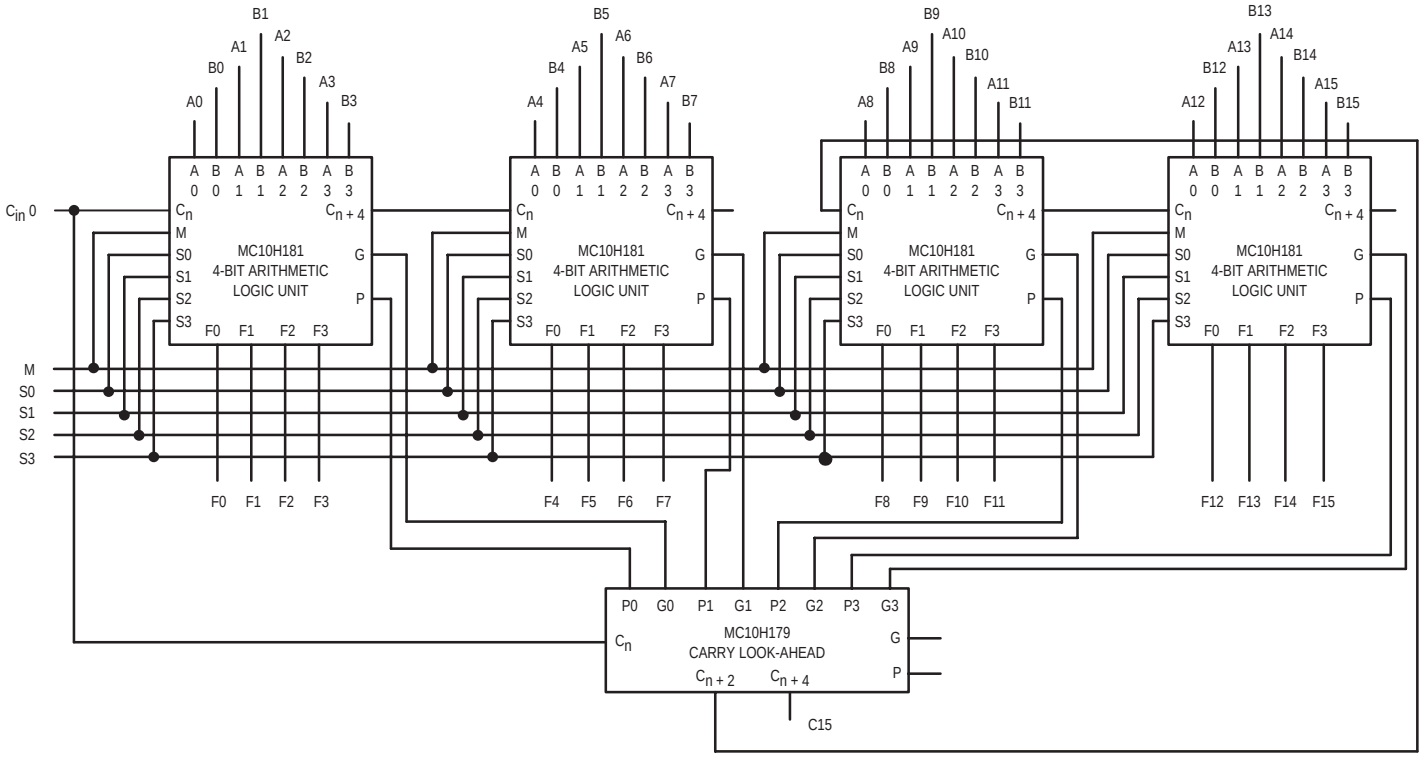


FIGURE 2 – 16–BIT FULL LOOK–AHEAD CARRY ARITHMETIC LOGIC UNIT



MC10H180

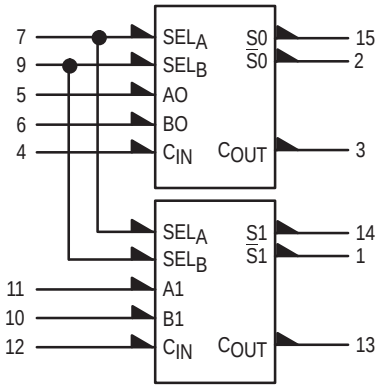
Dual 2-Bit Adder/Subtractor

The MC10H180 is a high–speed, low–power, general–purpose adder/ subtractor. It is designed to be used in special purpose adders/subtractors or in high–speed multiplier arrays.

Inputs for each adder are Carry–in, Operand A, and Operand B; outputs are Sum, $\overline{\text{Sum}}$ and Carry–out. The common select inputs serve as a control line to Invert A for subtract, and a control line to Invert B.

- Propagation Delay, 1.8 ns Typical, Operand and Select to Output
- Power Dissipation, 360 mW Typicalh180
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM

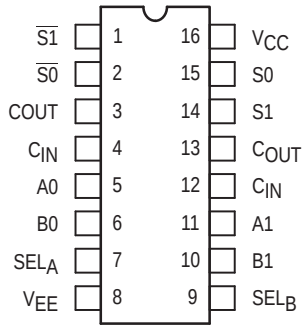


V_{CC} = PIN 16
V_{EE} = PIN 8

POSITIVE LOGIC ONLY

$A' = \overline{A} \oplus \overline{SEL_A} = A \odot SEL_A$
$B' = \overline{B} \oplus \overline{SEL_B} = B \odot SEL_B$
$S = \overline{C_{IN}}(\overline{A'}\,B' + A'\,\overline{B'}) + C_{IN}(A'\,B' + \overline{A'}\,\overline{B'})$
$C_{OUT} = C_{IN}A' + C_{IN}B' + A'\,B'$

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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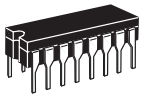
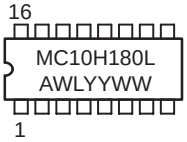
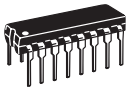
MARKING DIAGRAMS

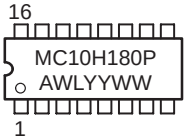


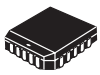
CDIP–16
L SUFFIX
CASE 620



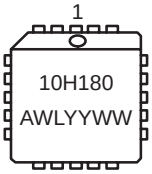


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H180L	CDIP–16	25 Units/Rail
MC10H180P	PDIP–16	25 Units/Rail
MC10H180FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	95	–	86	–	95	mA
I_{inH}	Input Current High Pins 4, 12 Pins 7, 9 Pins 5, 6, 10, 11	 – – –	 665 515 410	 – – –	 417 320 255	 – – –	 417 320 255	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage (1)	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage (1)	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay Operand to Output Select to Output Carry–in to Output	 0.6 0.6 0.4	 2.4 2.2 1.6	 0.7 0.7 0.4	 2.5 2.3 1.7	 0.8 0.8 0.4	 2.8 2.6 1.8	ns
t_r	Rise Time	0.5	2.0	0.5	2.1	0.5	2.2	ns
t_f	Fall Time	0.5	2.0	0.5	2.1	0.5	2.2	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

FUNCTION SELECT TABLE

Sel_A	Sel_B	Function
H	H	S = A plus B
H	L	S = A minus B
L	H	S = B minus A
L	L	S = 0 minus A minus B

TRUTH TABLE

FUNCTION	INPUTS							
	Sel_A	Sel_B	A0	B0	C_{in}	S0	$\overline{S0}$	C_{out}
ADD	H	H	L	L	L	L	H	L
	H	H	L	L	H	H	L	L
	H	H	L	H	L	H	L	L
	H	H	H	H	H	L	H	H
	H	H	H	L	L	H	L	H
	H	H	H	L	H	L	H	H
	H	H	H	H	L	L	H	H
	H	H	H	H	H	H	L	H
SUBTRACT	H	L	L	L	L	L	H	L
	H	L	L	L	H	H	L	H
	H	L	L	H	L	L	H	L
	H	L	L	H	H	H	L	L
	H	L	H	L	L	L	H	H
	H	L	H	L	H	H	L	H
	H	L	H	H	L	L	H	L
	H	L	H	H	H	H	L	L

FUNCTION	INPUTS							
	Sel_A	Sel_B	A0	B0	C_{in}	S0	$\overline{S0}$	C_{out}
REVERSE SUBTRACT	L	H	L	L	L	H	L	L
	L	H	L	L	H	L	H	H
	L	H	L	H	L	H	L	H
	L	H	L	H	H	L	H	L
	L	H	H	L	L	H	L	L
	L	H	H	L	H	H	L	L
	L	H	H	H	L	L	H	L
	L	H	H	H	H	H	L	H
	L	L	L	L	L	L	H	H
	L	L	L	L	H	H	L	H
	L	L	L	H	L	L	H	H
	L	L	L	H	H	H	L	L
	L	L	H	L	L	L	H	L
	L	L	H	L	H	H	L	L
	L	L	H	H	L	L	H	L
	L	L	H	H	H	H	L	L

MC10H181

4-Bit Arithmetic Logic Unit/ Function Generator

The MC10H181 is a high–speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two four–bit words. Full internal carry is incorporated for ripple through operation.

Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast operations on very long words using a second order look–ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

When used with the MC10H179, full–carry look–ahead, as a second order look–ahead block, the MC10H181 provides high–speed arithmetic operations on very long words.

This 10H part is a functional/pinout duplication of the standard MECL 10K family part with 100% improvement in propagation delay and no increase in power supply current.

- Improved Noise Margin, 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K – Compatible

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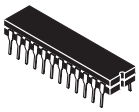
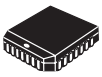
MARKING DIAGRAMS

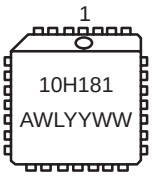


CDIP–24
L SUFFIX
CASE 758

PDIP–24
P SUFFIX
CASE 724



PLCC–28
FN SUFFIX
CASE 776

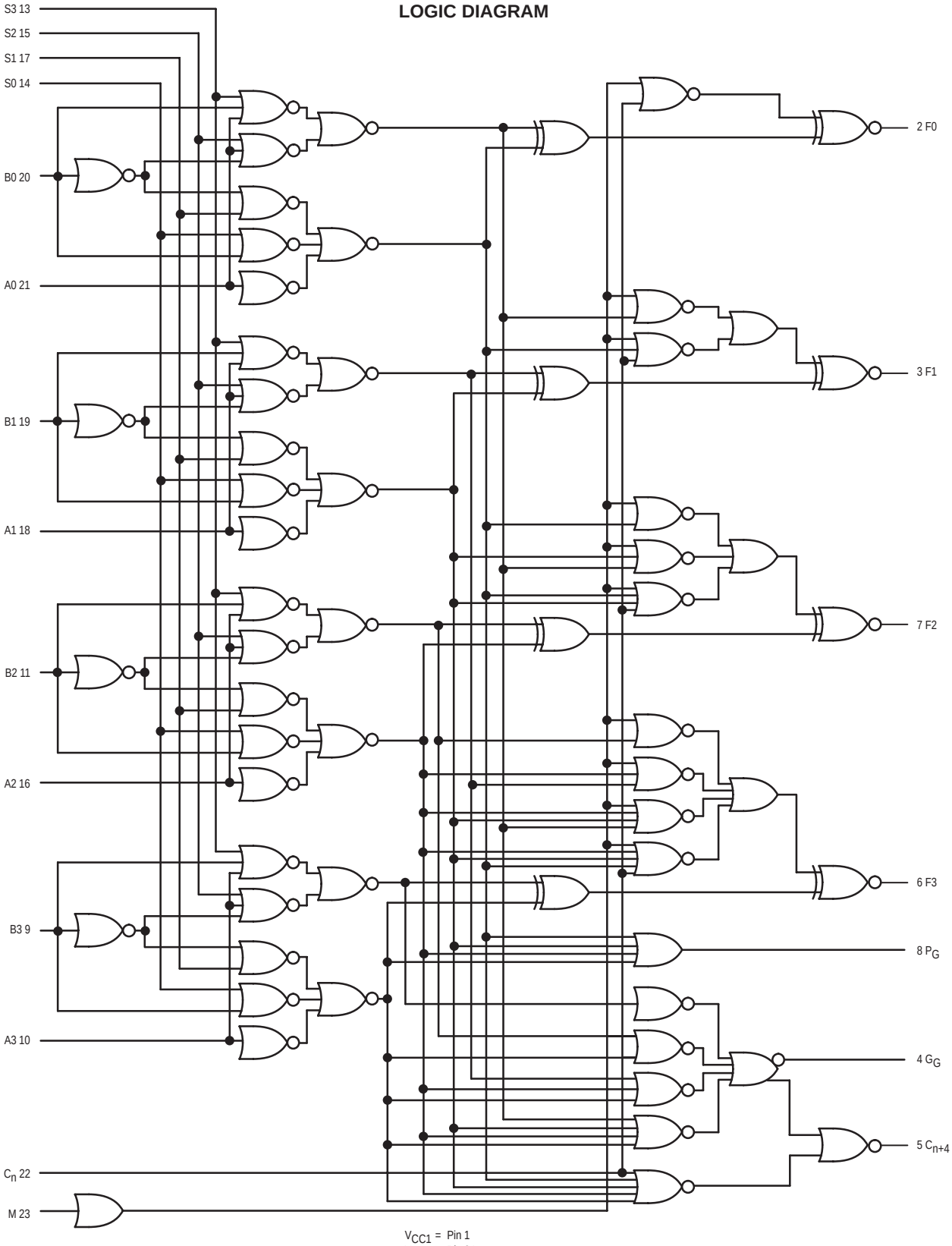


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

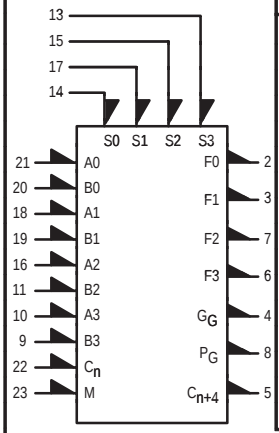
ORDERING INFORMATION

Device	Package	Shipping
MC10H181L	CDIP–24	15 Units/Rail
MC10H181P	PDIP–24	15 Units/Rail
MC10H181FN	PLCC–28	37 Units/Rail

LOGIC DIAGRAM



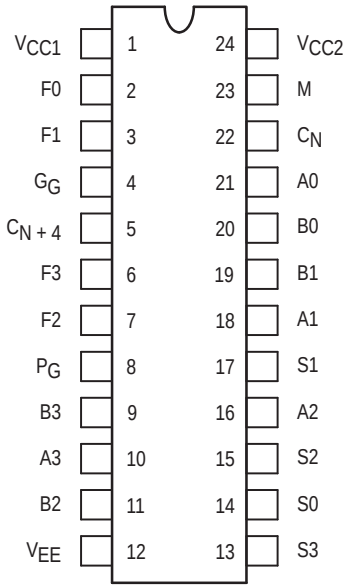
LOGIC DIAGRAM



FUNCTION SELECT TABLE

Function Select S3	S2	S1	S0	Logic Functions M is High C = D.C. F	Arithmetic Operation M is Low C_n is low F
L	L	L	L	$F = \overline{A}$	F = A
L	L	L	H	$F = \overline{A} + \overline{B}$	F = A plus $(A \cdot \overline{B})$
L	L	H	L	$F = \overline{A} + B$	F = A plus $(A \cdot B)$
L	L	H	H	F = Logical "1"	F = A times 2
L	H	L	L	$F = \overline{A} \cdot \overline{B}$	F = (A + B) plus 0
L	H	L	H	$F = \overline{B}$	F = (A + B) plus $(A \cdot \overline{B})$
L	H	H	L	$F = A \odot B$	F = A plus B
L	H	H	H	$F = A + \overline{B}$	F = A plus (A + B)
H	L	L	L	$F = \overline{A} \cdot B$	F = $(A + \overline{B})$ plus 0
H	L	L	H	$F = A \oplus B$	F = A minus B minus 1
H	L	H	L	F = B	F = $(A + \overline{B})$ plus $(A \cdot B)$
H	L	H	H	F = A + B	F = A plus $(A + \overline{B})$
H	H	L	L	F = Logical "0"	F = minus 1 (two's complement)
H	H	L	H	$F = A \cdot \overline{B}$	F = $(A \cdot \overline{B})$ minus 1
H	H	H	L	$F = A \cdot B$	F = $(A \cdot B)$ minus 1
H	H	H	H	F = A	F = A minus 1

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5.0%) (See Note 1.)

Characteristic	Symbol	0°		+25°		+75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	–	159	–	145	–	159	mA
Input Current High	I_{inH}							µA
Pin 22		–	720	–	450	–	450	
Pins 14,23		–	405	–	255	–	255	
Pins 13,15,17		–	515	–	320	–	320	
Pins 10,16,18,21		–	475	–	300	–	300	
Pins 9,11,19,20		–	465	–	275	–	275	
Input Current Low Pins 9–11, 13–22	I_{inL}	0.5	–	0.5	–	0.3	–	µA
High Output Voltage	V_{OH}	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
Low Output Voltage	V_{OL}	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
High Input Voltage	V_{IH}	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
Low Input Voltage	V_{IL}	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

AC PARAMETERS

Characteristic	Symbol	Input	Output	Conditions †	AC Switching Characteristics						Unit
					0°C		+25°C		+75°C		
					Min	Max	Min	Max	Min	Max	
Propagation Delay	t+ +, t– –	C_n	C_{n+4}	A0,A1,A2,A3	0.7	2.0	0.7	2.0	0.7	2.2	ns
Rise Time, Fall Time	t+, t–	C_n	C_{n+4}	A0,A1,A2,A3	0.6	2.0	0.6	2.0	0.7	2.2	ns
Propagation Delay	t+ +, t+ –,	C_n	F1	A0							ns
	t– +, t– –	C_n	F1		1.0	3.0	1.0	3.0	1.2	3.3	
Rise Time, Fall Time	t+, t–	C_n	F1		0.7	2.2	0.7	2.2	0.7	2.4	
Propagation Delay	t+ +, t+ –,	A1	F1								ns
	t– +, t– –	A1	F1		1.5	3.7	1.5	3.7	1.6	4.0	
Rise Time, Fall Time	t+, t–	A1	F1		0.7	2.0	0.7	2.0	0.7	2.2	
Propagation Delay	t+ +, t– –	A1	P_G	S0,S3	1.5	3.7	1.5	3.7	1.6	4.0	ns
Rise Time, Fall Time	t+, t–	A1	P_G	S0,S3	0.9	2.4	0.9	2.4	0.9	2.6	ns
Propagation Delay	t+ +, t– –	A1	G_G	A0,A2,A3,C_n	1.5	3.7	1.5	3.7	1.6	3.9	ns
Rise Time, Fall Time	t+, t–	A1	G_G	A0,A2,A3,C_n	0.7	2.2	0.7	2.2	0.7	2.4	ns
Propagation Delay	t+ –, t– +	A1	C_{n+4}	A0,A2,A3,C_n	1.5	3.6	1.5	3.6	1.6	3.9	ns
Rise Time, Fall Time	t+, t–	A1	C_{n+4}	A0,A2,A3,C_n	0.5	2.0	0.5	2.0	0.5	2.2	ns
Propagation Delay	t+ +, t– +	B1	F1	S3,C_n	2.0	4.5	2.0	4.5	2.1	4.8	ns
Rise Time, Fall Time	t+, t–	B1	F	S3,C_n	0.7	2.3	0.7	2.3	0.7	2.5	ns
Propagation Delay	t+ +, t– –	B1	P_G	S0,A1	1.5	3.8	1.5	3.8	1.6	4.0	ns
Rise Time, Fall Time	t+, t–	B1	P_G	S0,A1	0.7	2.2	0.7	2.2	0.7	2.4	ns
Propagation Delay	t+ +, t– –	B1	G_G	S3,C_n	1.5	3.7	1.5	3.7	1.6	4.0	ns
Rise Time, Fall Time	t+, t–	B1	G_G	S3,C_n	0.7	2.2	0.7	2.2	0.7	2.4	ns
Propagation Delay	t+ –, t– +	B1	C_{n+4}	S3,C_n	2.0	4.0	2.0	4.0	2.1	4.3	ns
Rise Time, Fall Time	t+, t–	B1	C_{n+4}	S3,C_n	0.5	2.0	0.5	2.2	0.5	2.2	ns
Propagation Delay	t+ +, t+ –	M	F1	–	1.5	4.2	1.5	4.2	1.6	4.5	ns
Rise Time, Fall Time	t+, t–	M	F1	–	0.8	2.3	0.8	2.3	0.8	2.5	ns
Propagation Delay	t+ –, t– +	S1	F1	A1,B1	1.5	4.5	1.5	4.5	1.6	4.8	ns
Rise Time, Fall Time	t+, t–	S1	F1	A1,B1	0.7	2.0	0.7	2.0	0.7	2.2	ns
Propagation Delay	t– +, t+ –	S1	P_G	A3,B3	1.5	4.0	1.5	4.0	1.6	4.3	ns
Rise Time, Fall Time	t+, t–	S1	P_G	A3,B3	0.7	2.0	0.7	2.2	0.7	2.4	ns
Propagation Delay	t+ –, t– +	S1	C_{n+4}	A3,B3	1.5	4.1	1.5	4.1	1.6	4.4	ns
Rise Time, Fall Time	t+, t–	S1	C_{n+4}	A3,B3	0.7	2.2	0.7	2.2	0.7	2.4	ns
Propagation Delay	t+ –, t– +	S1	G_G	A3,B3	1.3	4.5	1.3	4.5	1.4	4.8	ns
Rise Time, Fall Time	t+, t–	S1	G_G	A3,B3	0.5	3.2	0.5	3.2	0.5	3.4	ns

† Logic high level (+1.11 Vdc) applied to pins listed. All other input pins are left floating or tied to +0.31 Vdc.
$V_{CC1} = V_{CC2}$ = +2.0 Vdc, V_{EE} = –3.2 Vdc

MC10H186

Hex D Master-Slave Flip-Flop with Reset

The MC10H186 is a hex D type flip–flop with common reset and clock lines. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock toggle frequency and propagation delay and no increase in power–supply current.

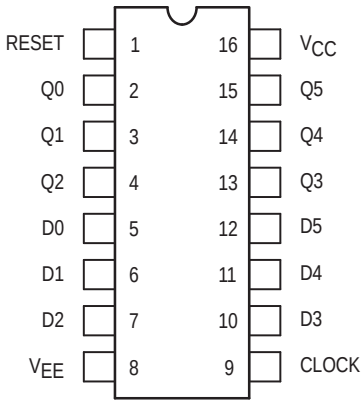
- Propagation Delay, 1.7 ns Typical
- Power Dissipation, 460 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

CLOCKED TRUTH TABLE

R	C	D	Qn+1
L	L	X	Qn
L	H *	L	L
L	H *	H	H
H	L	X	L

* A clock H is a clock transition from a low to a high state.

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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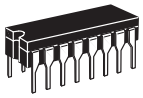
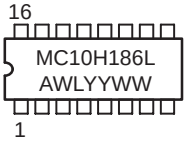
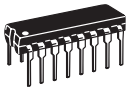
MARKING DIAGRAMS

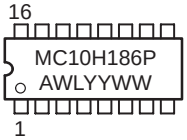


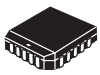
CDIP–16
L SUFFIX
CASE 620



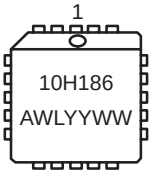


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H186L	CDIP–16	25 Units/Rail
MC10H186P	PDIP–16	25 Units/Rail
MC10H186FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	121	–	110	–	121	mA
I_{inH}	Input Current High Pins 5,6,7,10,11,12 Pin 9 Pin 1	 – – –	 430 670 1250	 – – –	 265 420 765	 – – –	 265 420 765	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

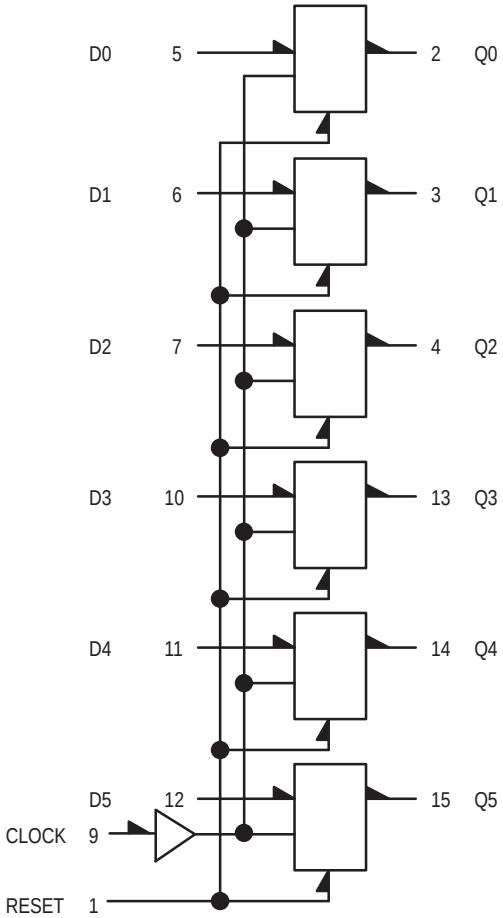
t_{pd}	Propagation Delay	0.7	3.0	0.7	3.0	0.7	3.0	ns
t_{set}	Set–up Time	1.5	–	1.5	–	1.5	–	ns
t_{hold}	Hold Time	1.0	–	1.0	–	1.0	–	ns
t_r	Rise Time	0.7	2.6	0.7	2.6	0.7	2.6	ns
t_f	Fall Time	0.7	2.6	0.7	2.6	0.7	2.6	ns
f_{tog}	Toggle Frequency	250	–	250	–	250	–	MHz
t_{rr}	Reset Recovery Time (t_{1-9+})	3.0	–	3.0	–	3.0	–	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

APPLICATION INFORMATION

The MC10H186 contains six high–speed, master slave type “D” flip–flops. Data is entered into the master when the clock is low. Master–to–slave data transfer takes place on the positive–going Clock transition. Thus outputs may change only on a positive–going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master–slave construction of this device. A common Reset is included in this circuit. **THE RESET ONLY FUNCTIONS WHEN THE CLOCK IS LOW.**

LOGIC DIAGRAM



V_{CC} = PIN 16
V_{EE} = PIN 8

MC10H188

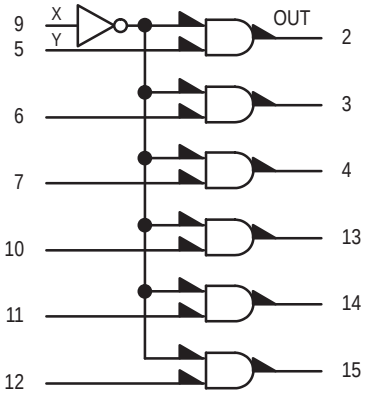
Hex Buffer with Enable

The MC10H188 is a high–speed Hex Buffer with a common Enable input. When Enable is in the high–state, all outputs are in the low–state. When Enable is in the low–state, the outputs take the same state as the inputs.

This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power–supply current.

- Propagation Delay, 1.3 ns Typical Data–to–Output
- Power Dissipation 180 mW Typ/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM

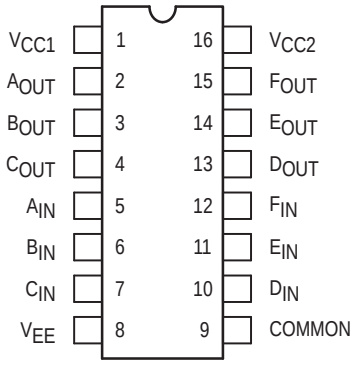


TRUTH TABLE

Inputs		Output
X	Y	OUT
L	L	L
L	H	H
H	L	L
H	H	L

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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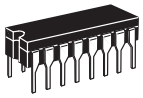
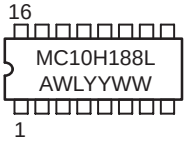
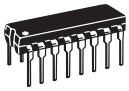
MARKING DIAGRAMS

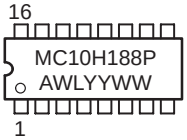


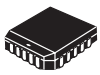
CDIP–16
L SUFFIX
CASE 620



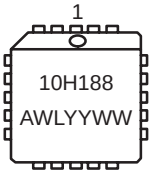


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H188L	CDIP–16	25 Units/Rail
MC10H188P	PDIP–16	25 Units/Rail
MC10H188FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	46	–	42	–	46	mA
I_{inH}	Input Current High	–	495	–	310	–	310	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay Enable Data	 0.7 0.7	 2.2 1.9	 0.7 0.7	 2.2 1.9	 0.7 0.7	 2.2 1.9	ns
t_r	Rise Time	0.7	2.4	0.7	2.4	0.7	2.4	ns
t_f	Fall Time	0.7	2.4	0.7	2.4	0.7	2.4	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

MC10H189

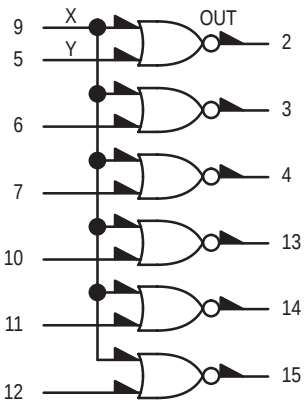
Hex Inverter with Enable

The MC10H189 is a Hex Inverter with a common Enable input. The hex inverting function is provided when Enable is in the low–state. When Enable is in the high–state, all outputs are low.

This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power–supply current.

- Propagation Delay, 1.3 ns Typical Data–to–Output
- Power Dissipation 180 mW Typ/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM

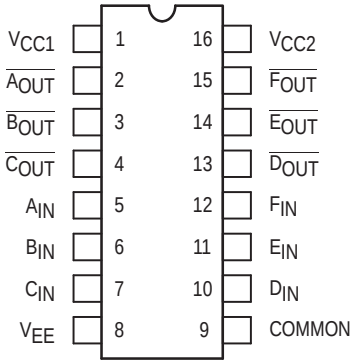


TRUTH TABLE

Inputs		Output
X	Y	OUT
L	L	H
L	H	L
H	L	L
H	H	L

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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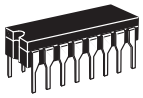
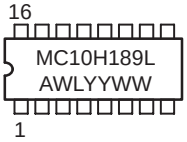
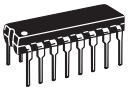
MARKING DIAGRAMS

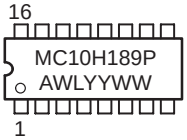


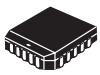
CDIP–16
L SUFFIX
CASE 620



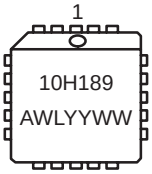


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H189L	CDIP–16	25 Units/Rail
MC10H189P	PDIP–16	25 Units/Rail
MC10H189FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	46	–	42	–	46	mA
I_{inH}	Input Current High	–	495	–	310	–	310	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay Enable Data	 0.7 0.7	 2.2 1.9	 0.7 0.7	 2.2 1.9	 0.7 0.7	 2.3 1.9	ns
t_r	Rise Time	0.7	2.4	0.7	2.4	0.7	2.4	ns
t_f	Fall Time	0.7	2.4	0.7	2.4	0.7	2.4	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

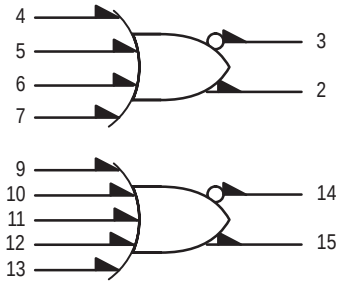
MC10H209

Dual 4-5-Input OR/NOR Gate

The MC10H209 is a Dual 4–5–input OR/NOR gate. This MECL part is a functional/pinout duplication of the MECL III part MC1688.

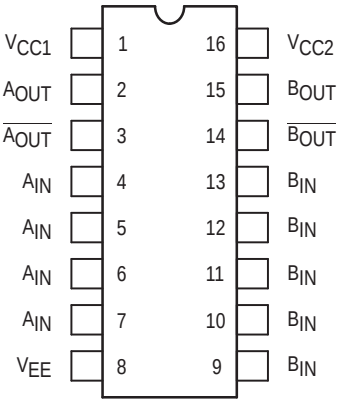
- Propagation Delay Average, 0.75 ns Typical
- Power Dissipation 125 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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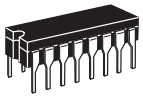
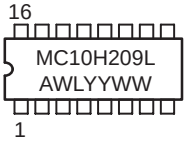
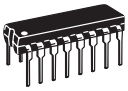
MARKING DIAGRAMS

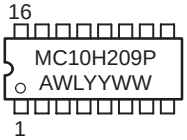


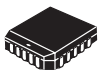
CDIP–16
L SUFFIX
CASE 620



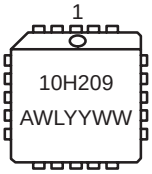


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H209L	CDIP–16	25 Units/Rail
MC10H209P	PDIP–16	25 Units/Rail
MC10H209FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	–	–	30	–	–	mA
I_{inH}	Input Current High	–	640	–	400	–	400	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay	0.4	1.15	0.4	1.15	0.4	1.15	ns
t_r	Rise Time	0.4	1.5	0.4	1.5	0.4	1.6	ns
t_f	Fall Time	0.4	1.5	0.4	1.5	0.4	1.6	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

MC10H210

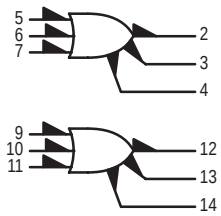
Dual 3-Input 3-Output OR Gate

The MC10H210 is designed to drive up to six transmission lines simultan– eously. The multiple outputs of this device also allow the wire “OR”–ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10H210 particularly useful in clock distribution applications where minimum clock skew is desired.

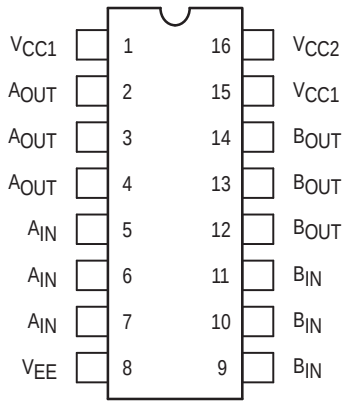
- Propagation Delay Average, 1.0 ns Typical
- Power Dissipation, 160 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



V_{CC1} = PINS 1, 15
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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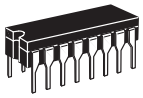
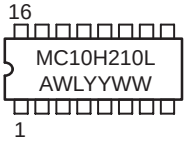
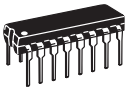
MARKING DIAGRAMS

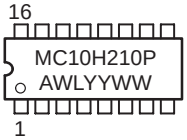


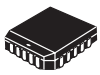
CDIP–16
L SUFFIX
CASE 620



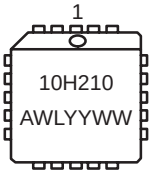


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H210L	CDIP–16	25 Units/Rail
MC10H210P	PDIP–16	25 Units/Rail
MC10H210FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	42	–	38	–	42	mA
I_{inH}	Input Current High	–	720	–	450	–	450	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay	0.5	1.55	0.55	1.55	0.6	1.7	ns
t_r	Rise Time	0.75	1.8	0.75	1.9	0.8	2.0	ns
t_f	Fall Time	0.75	1.8	0.75	1.9	0.8	2.0	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Note: If crosstalk is present, double bypass capacitor to 0.2 µF.

MC10H211

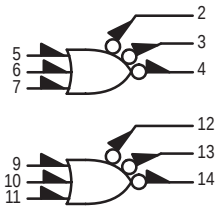
Dual 3-Input 3-Output NOR Gate

The MC10H211 is designed to drive up to six transmission lines simultan– eously. The multiple outputs of this device also allow the wire "OR"–ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10H211 particularly useful in clock distribution applications where minimum clock skew is desired.

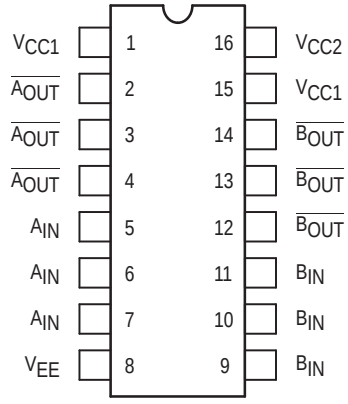
- Propagation Delay, 1.0 ns Typical
- Power Dissipation, 160 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



V_{CC1} = PINS 1, 15
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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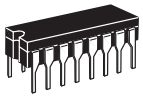
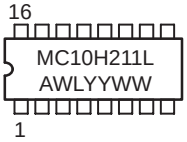
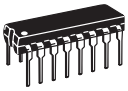
MARKING DIAGRAMS

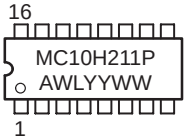


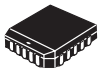
CDIP–16
L SUFFIX
CASE 620





PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H211L	CDIP–16	25 Units/Rail
MC10H211P	PDIP–16	25 Units/Rail
MC10H211FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	42	–	38	–	42	mA
I_{inH}	Input Current High	–	720	–	450	–	450	µA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay	0.7	1.6	0.7	1.6	0.7	1.7	ns
t_r	Rise Time	0.9	2.0	0.9	2.2	0.9	2.4	ns
t_f	Fall Time	0.9	2.0	0.9	2.2	0.9	2.4	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Note: If crosstalk is present, double bypass capacitor to 0.2 µF.

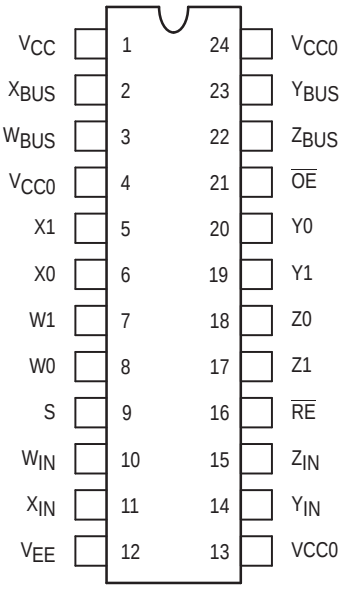
MC10H330

Quad Bus Driver/Receiver with 2-to-1 Output Multiplexers

The MC10H330 is a Quad Bus Driver/Receiver with two–to–one output multiplexers. These multiplexers have a common select and output enable. When disabled, ($\overline{OE}$ = high) the bus outputs go to –2.0 V. Their output can be brought to a low state (V_{OL}) by applying a high level to the receiver enable ($\overline{RE}$ = High). The parameters specified are with 25 Ω loading on the bus drivers and 50 Ω loads on the receivers.

- Propagation Delay, 1.5 ns Typical Data–to–Output
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

DIP
PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Receiver outputs are terminated through a 50–ohm resistor to –2.0 volts dc. Bus outputs are terminated through a 25–ohm resistor to –2.0 volts dc.

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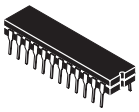
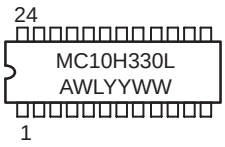
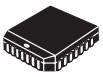
MARKING DIAGRAMS



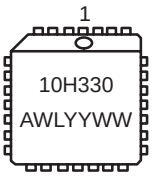
CDIP–24
L SUFFIX
CASE 758



PDIP–24
P SUFFIX
CASE 724



PLCC–28
FN SUFFIX
CASE 776



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H330L	CDIP–24	15 Units/Rail
MC10H330P	PDIP–24	15 Units/Rail
MC10H330FN	PLCC–28	37 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

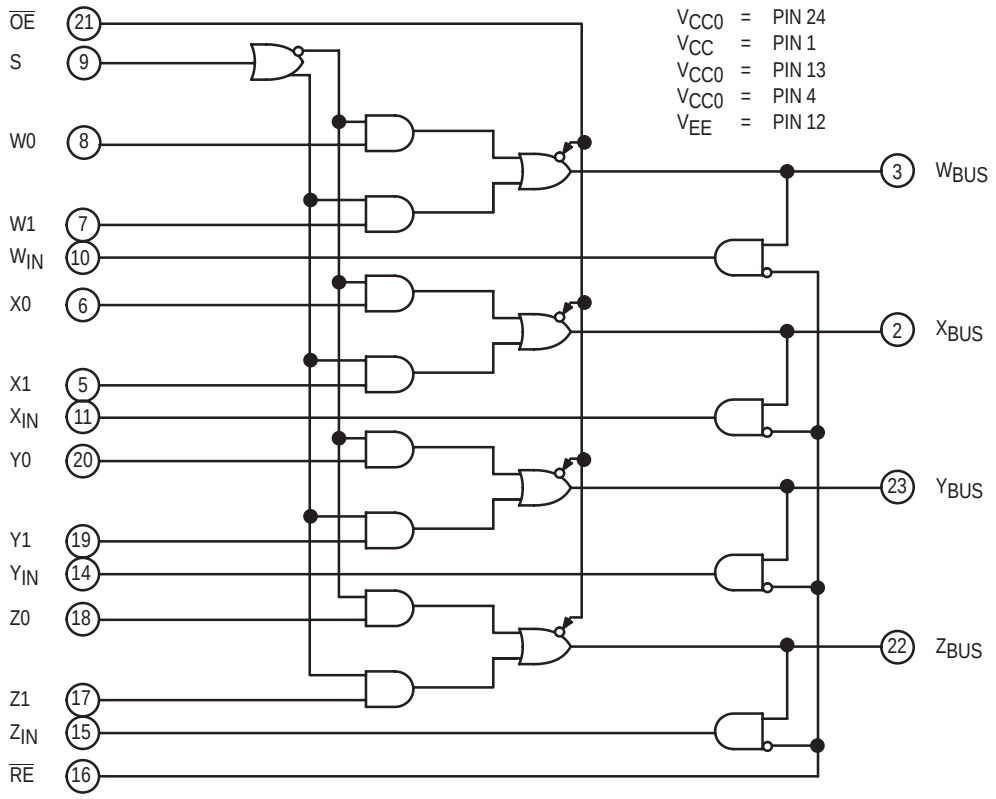
ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	157	–	143	–	157	mA
I_{inH}	Input Current High							µA
	Pins 5–8, 17–20	–	667	–	417	–	417	
	Pins 16, 21	–	514	–	321	–	321	
	Pin 9	–	475	–	297	–	297	
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay							ns
	Select–to–Input	1.8	5.3	1.8	5.3	1.8	5.3	
	Data–to–Bus Output	0.5	2.0	0.5	2.0	0.5	2.0	
	Select–to–Bus Output	1.0	3.2	1.0	3.2	1.0	3.2	
	$\overline{OE}$–to–Bus Output	0.8	2.2	0.8	2.2	0.8	2.2	
	Bus–to–Input	0.8	2.1	0.8	2.1	0.8	2.4	
	$\overline{RE}$–to–Input	0.5	2.2	0.5	2.2	0.5	2.2	
	Data–to–Receiver Input	1.3	4.0	1.3	4.0	1.3	4.0	
t_r	Rise Time	0.5	2.0	0.5	2.0	0.5	2.0	ns
t_f	Fall Time	0.5	2.0	0.5	2.0	0.5	2.0	ns

LOGIC DIAGRAM



MULTIPLEXER TRUTH TABLE

$\overline{OE}$	S	W_{Bus}	X_{Bus}	Y_{Bus}	Z_{Bus}
H	X	–2.0 V	–2.0 V	–2.0 V	–2.0 V
L	L	W0	X0	Y0	Z0
L	H	W1	X1	Y1	Z1

RECEIVER TRUTH TABLE

$\overline{RE}$	W_{in}	X_{in}	Y_{in}	Z_{in}
H	L	L	L	L
L	W_{Bus}	X_{Bus}	Y_{Bus}	Z_{Bus}

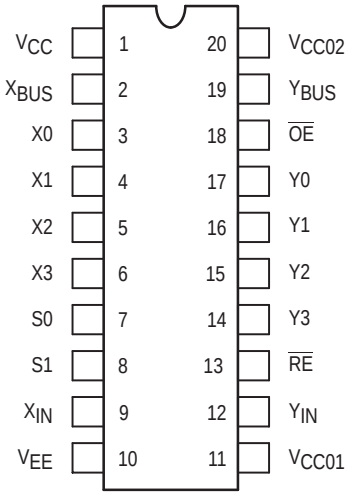
MC10H332

Dual Bus Driver/Receiver with 4-to-1 Output Multiplexers

The MC10H332 is a Dual Bus Driver/Receiver with four–to–one output multiplexers. These multiplexers have common selects and output enable. When disabled, ($\overline{OE}$ = high) the bus outputs go to –2.0 V. The parameters specified are with 25 Ω loading on the bus drivers and 50 Ω loads on the receivers.

- Propagation Delay, 1.5 ns Typical Data–to–Output
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

DIP & PLCC PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Receiver outputs are terminated through a 50–ohm resistor to –2.0 volts dc. Bus outputs are terminated through a 25–ohm resistor to –2.0 volts dc.

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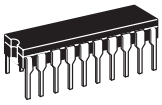
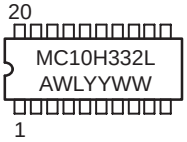
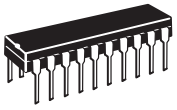
MARKING DIAGRAMS

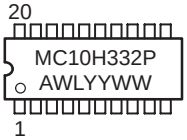


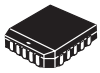
CDIP–20
L SUFFIX
CASE 732



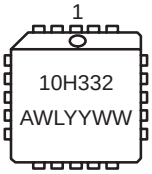


PDIP–20
P SUFFIX
CASE 738





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H332L	CDIP–20	18 Units/Rail
MC10H332P	PDIP–20	18 Units/Rail
MC10H332FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	115	–	110	–	115	mA
I_{inH}	Input Current High							µA
	Pins 3,4,5,6,14, 15,16,17	–	667	–	417	–	417	
	Pins 7,8	–	437	–	273	–	273	
	Pins 13, 18	–	456	–	285	–	285	
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay							ns
	Data–to–Bus Output	0.8	3.0	0.8	3.0	0.8	3.2	
	Select–to–Bus Output	0.8	3.4	0.8	3.4	0.8	3.8	
	$\overline{OE}$–to–Bus Output	0.8	2.4	0.8	2.4	0.8	2.6	
	Bus–to–Receiver	0.8	2.1	0.8	2.1	0.8	2.4	
	Select–to–Receiver	1.8	4.5	1.8	4.5	1.8	5.0	
	$\overline{RE}$–to–Receiver	0.8	2.2	0.8	2.2	0.8	2.5	
	Data–to–Receiver	1.3	4.0	1.3	4.0	1.3	4.5	
t_r	Rise Time	0.5	2.0	0.5	2.0	0.5	2.1	ns
t_f	Fall Time	0.5	2.0	0.5	2.0	0.5	2.1	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

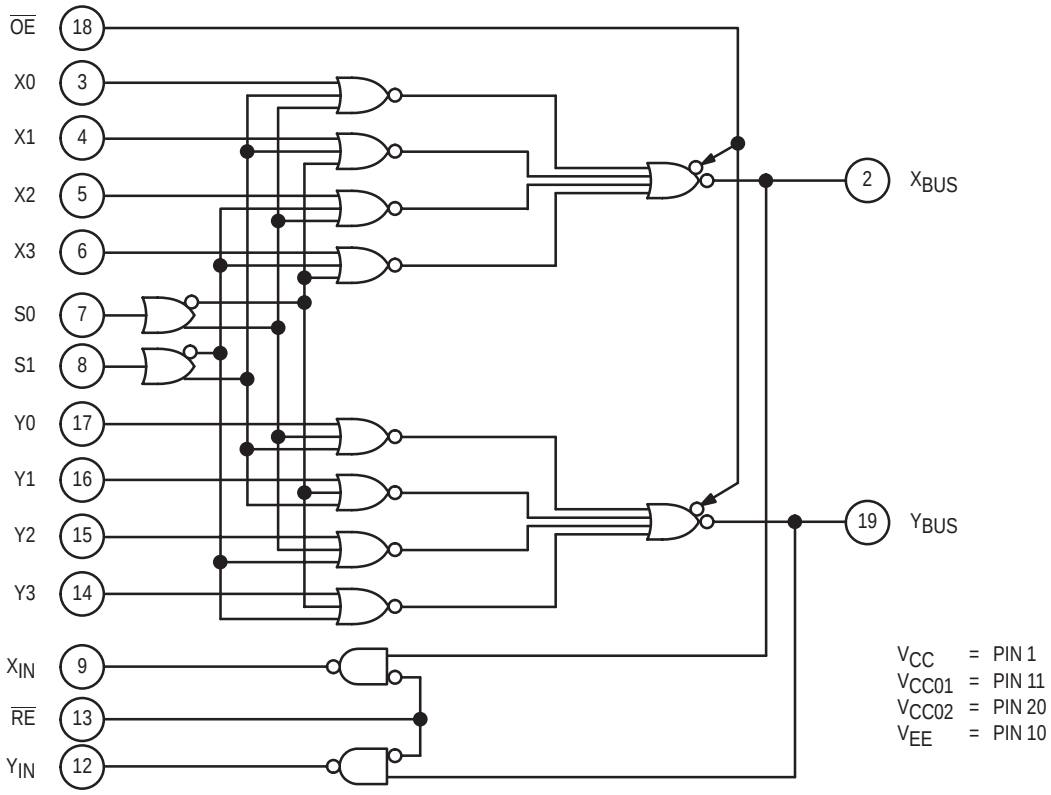
MULTIPLEXER TRUTH TABLE

$\overline{OE}$	S1	S0	X_{Bus}	Y_{Bus}
H	X	X	–2.0V	–2.0V
L	L	L	X0	Y0
L	L	H	X1	Y1
L	H	L	X2	Y2
L	H	H	X3	Y3

RECEIVER TRUTH TABLE

$\overline{RE}$	X_{in}	Y_{in}
H	L	L
L	X_{Bus}	Y_{Bus}

LOGIC DIAGRAM



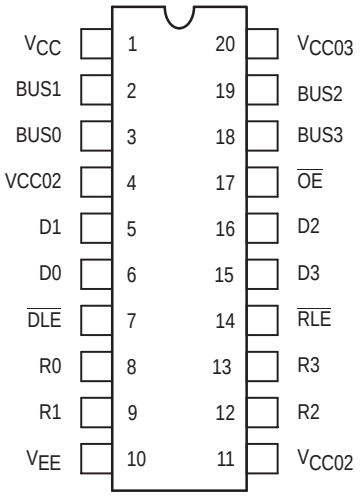
MC10H334

Quad Bus Driver/Receiver with Transmit and Receiver Latches

The MC10H334 is a Quad Bus Driver/Receiver with transmit and receiver latches. When disabled, ($\overline{OE}$ = high) the bus outputs will fall to –2.0 V. Data to be transmitted or received is passed through its respective latch when the respective latch enable ($\overline{DLE}$ and $\overline{RLE}$) is at a low level. Information is latched on the positive transition of $\overline{DLE}$ and $\overline{RLE}$. The parameters specified are with 25 Ω loading on the bus drivers and 50 Ω loads on the receivers.

- Propagation Delay, 1.6 ns Typical Data–to–Output
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

DIP & PLCC PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Receiver outputs are terminated through a 50–ohm resistor to –2.0 volts dc. Bus outputs are terminated through a 25–ohm resistor to –2.0 volts dc.

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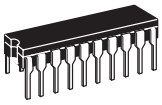
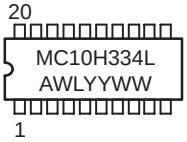
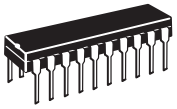
MARKING DIAGRAMS

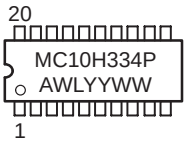


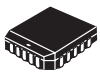
CDIP–20
L SUFFIX
CASE 732



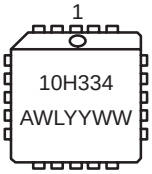


PDIP–20
P SUFFIX
CASE 738





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H334L	CDIP–20	18 Units/Rail
MC10H334P	PDIP–20	18 Units/Rail
MC10H334FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

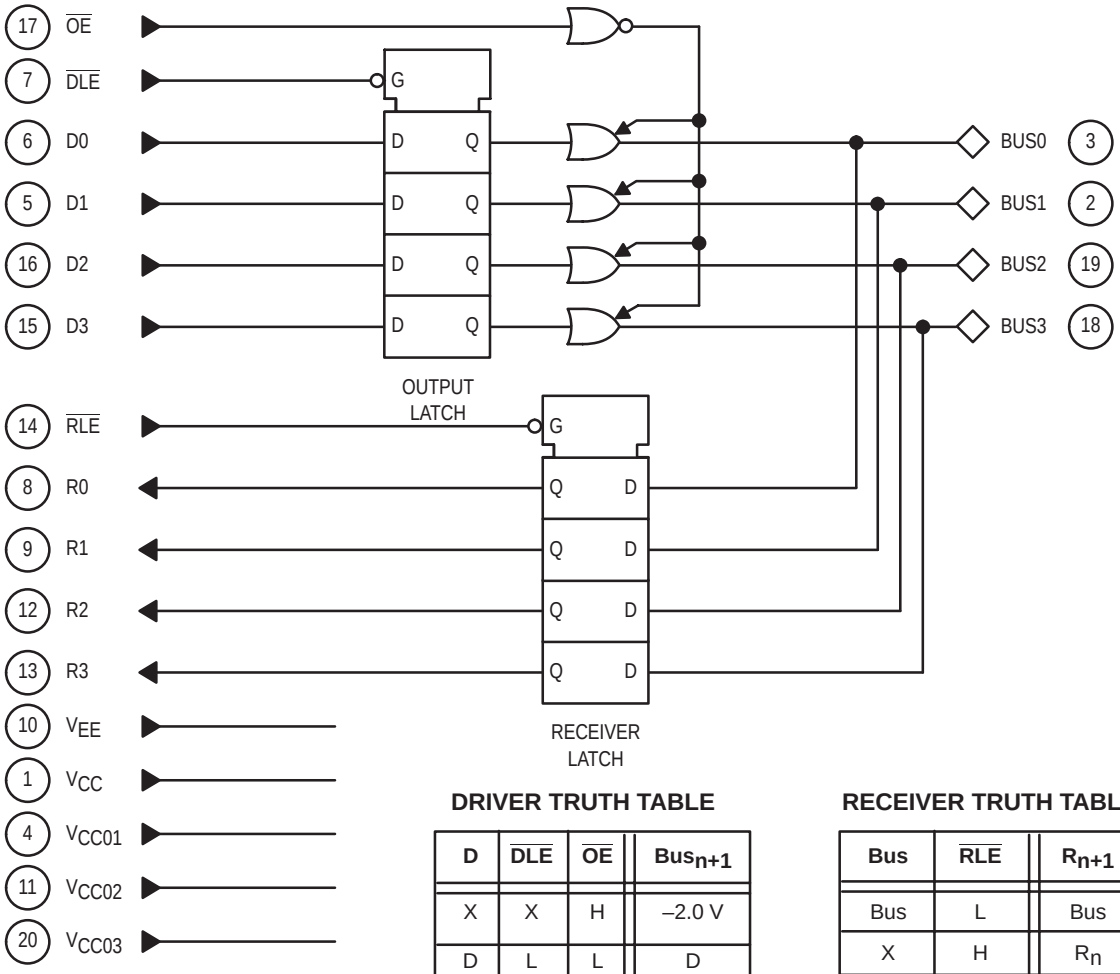
ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	–	161	–	161	–	161	mA
I_{inH}	Input Current High							µA
	Pins 5,6,15,16	–	397	–	273	–	273	
	Pins 7,14	–	460	–	297	–	297	
	Pin 17	–	520	–	357	–	357	
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

t_{pd}	Propagation Delay							ns
	Data–to–Bus Output	0.5	2.5	0.5	2.5	0.5	2.5	
	$\overline{DLE}$–to–Bus Output	1.0	2.7	1.0	2.7	1.0	2.7	
	$\overline{OE}$–to–Bus Output	0.5	2.5	0.5	2.5	0.5	2.5	
	Bus–to–R0	0.5	1.9	0.5	1.9	0.5	1.9	
	$\overline{RLE}$–to–R0	0.5	2.1	0.5	2.1	0.5	2.1	
	Data–to–Receiver R0	1.0	3.8	1.0	3.8	1.0	3.8	
t_r	Rise Time	0.5	2.2	0.5	2.2	0.5	2.2	ns
t_f	Fall Time	0.5	2.2	0.5	2.2	0.5	2.2	ns

LOGIC DIAGRAM



DRIVER TRUTH TABLE

D	$\overline{DLE}$	$\overline{OE}$	Bus_{n+1}
X	X	H	–2.0 V
D	L	L	D
X	H	L	Bus_n

RECEIVER TRUTH TABLE

Bus	$\overline{RLE}$	R_{n+1}
Bus	L	Bus
X	H	R_n

MC10H350

PECL* to TTL Translator

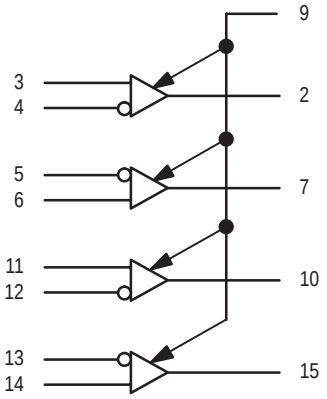
(+5 Vdc Power Supply Only)

The MC10H350 is a member of Motorola's 10H family of high performance ECL logic. It consists of 4 translators with differential inputs and TTL outputs. The 3–state outputs can be disabled by applying a HIGH TTL logic level on the common OE input.

The MC10H350 is designed to be used primarily in systems incorporating both ECL and TTL logic operating off a common power supply. The separate V_{CC} power pins are not connected internally and thus isolate the noisy TTL V_{CC} runs from the relatively quiet ECL V_{CC} runs on the printed circuit board. The differential inputs allow the H350 to be used as an inverting or noninverting translator, or a differential line receiver. The H350 can also drive CMOS with the addition of a pullup resistor.

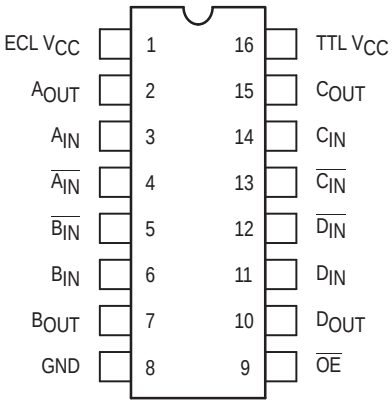
- Propagation Delay, 3.5 ns Typical
- MECL 10K–Compatible

LOGIC DIAGRAM



V_{CC} (+5.0 VDC) = PINS 1 AND 16
GND = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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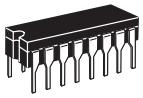
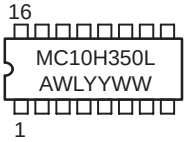
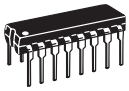
MARKING DIAGRAMS

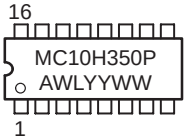


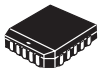
CDIP–16
L SUFFIX
CASE 620



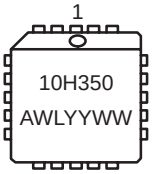


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H350L	CDIP–16	25 Units/Rail
MC10H350P	PDIP–16	25 Units/Rail
MC10H350FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{CC}	Power Supply (V_{EE} = Gnd)	7.0	Vdc
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%) (See Note 1.)

Symbol	Characteristic	T_A = 0°C to 75°C Min	T_A = 0°C to 75°C Max	Unit
I_{CC}	Power Supply Current TTL ECL	– –	20 12	mA
I_{IH} I_{INH}	Input Current High Pin 9 Others	– –	20 50	μA
I_{IL} I_{INL}	Input Current Low Pin 9 Others	– –	–0.6 50	mA μA
V_{IH}	Input Voltage High Pin 9	2.0	–	Vdc
V_{IL}	Input Voltage Low Pin 9	–	0.8	Vdc
V_{DIFF}	Differential Input Voltage (Note 1.) Pins 3–6, 11–14 (1)	350	–	mV
V_{CM}	Voltage Common Mode Pins 3–6, 11–14	2.8	V_{CC}	Vdc
V_{OH}	Output Voltage High I_{OH} = 3.0 mA	2.7	–	Vdc
V_{OL}	Output Voltage Low I_{OL} = 20 mA	–	0.5	Vdc
I_{OS}	Short Circuit Current V_{OUT} = 0 V	–60	–150	mA
I_{OZH}	Output Disable Current High V_{OUT} = 2.7 V	–	50	μA
I_{OZL}	Output Disable Current Low V_{OUT} = 0.5 V	–	–50	μA

1. Common mode input voltage to pins 3–4, 5–6, 11–12, 13–14 must be between the values of 2.8 V and 5.0 V. This common mode input voltage range includes the differential input swing.
2. For single ended use, apply 3.75 V (V_{BB}) to either input depending on output polarity required. Signal level range to other input is 3.3 V to 4.2 V.
3. Any unused gates should have the inverting inputs tied to V_{CC} and the non–inverting inputs tied to ground to prevent output glitching.
4. 1.0 V to 2.0 V w/50 pF into 500 ohms.

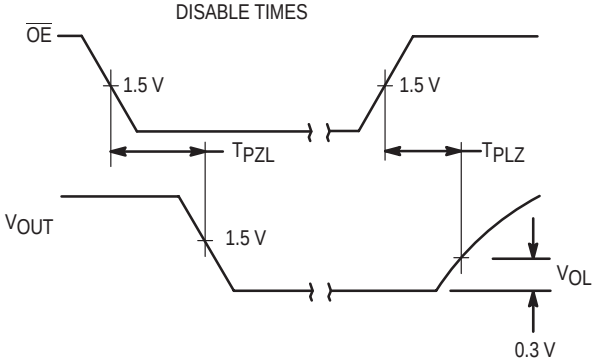
*Positive Emitter Coupled Logic

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%) (See Notes 1 & 4)

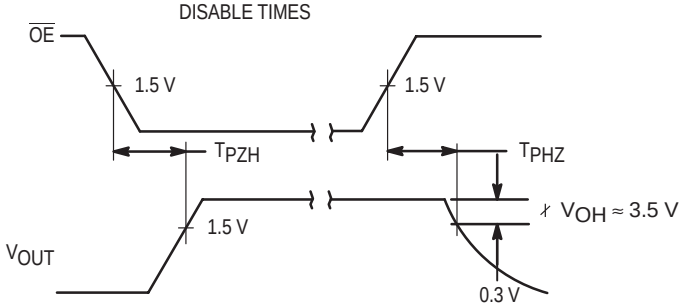
Symbol	Characteristic	T_A = 0°C to 75°C Min	T_A = 0°C to 75°C Max	Unit
AC PARAMETERS (C_L = 50 pF) (V_{CC} = 5.0 ± 5%) (T_A = 0°C to 75°C)				
t_{pd}	Propagation Delay Data (50% to 1.5V)	1.5	5.0	ns
t_r	Rise Time (Note 4.)	0.3	1.6	ns
t_f	Fall Time (Note 4.)	0.3	1.6	ns
t_{pdLZ} t_{pdHZ}	Output Disable Time	2.0 2.0	6.0 6.0	ns
t_{pdZL} t_{pdZH}	Output Enable Time	2.0 2.0	8.0 8.0	ns

3–STATE SWITCHING WAVEFORMS

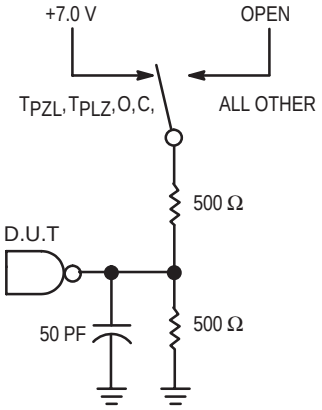
3–STATE OUTPUT LOW ENABLE AND DISABLE TIMES



3–STATE OUTPUT HIGH ENABLE AND DISABLE TIMES



TEST LOAD



*INCLUDES JIG AND PROBE CAPACITANCE

Application Note: Pin 9 is an $\overline{OE}$ and the 10H350 is disabled when $\overline{OE}$ is at V_{IH} or higher.

MC10H351

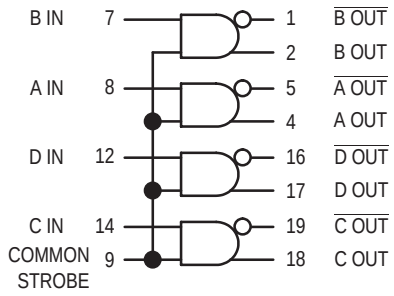
Quad TTL/NMOS to PECL* Translator

The MC10H351 is a quad translator for interfacing data between a saturated logic section and the PECL section of digital systems when only a +5.0 Vdc power supply is available. The MC10H351 has TTL/NMOS compatible inputs and PECL complementary open–emitter outputs that allow use as an inverting/non–inverting translator or as a differential line driver. When the common strobe input is at a low logic level, it forces all true outputs to the PECL low logic state (≈ +3.2 V) and all inverting outputs to the PECL high logic state (≈ +4.1 V).

The MC10H351 can also be used with the MC10H350 to transmit and receive TTL/NMOS information differentially via balanced twisted pair lines.

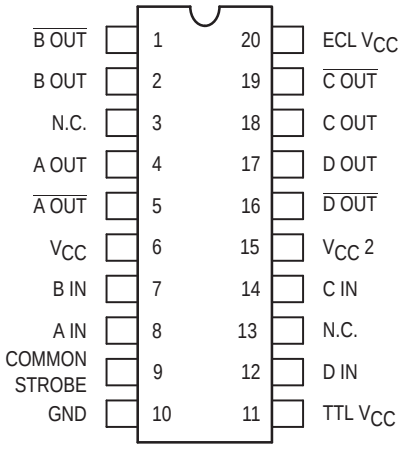
- Single +5.0 Power Supply
- All V_{CC} Pins Isolated On Chip
- Differentially Drive Balanced Lines
- t_{pd} = 1.3 nsec Typical

LOGIC DIAGRAM



V_{CC} (+5.0 VDC) = PINS 6, 11, 15, 20
GND = PIN 10

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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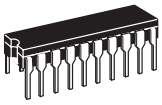
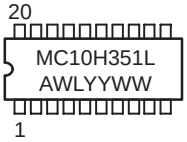
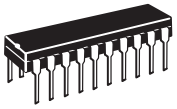
MARKING DIAGRAMS

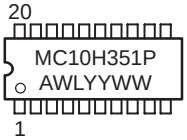


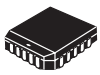
CDIP–20
L SUFFIX
CASE 732



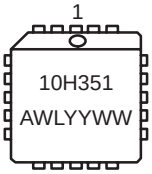


PDIP–20
P SUFFIX
CASE 738





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H351L	CDIP–20	18 Units/Rail
MC10H351P	PDIP–20	18 Units/Rail
MC10H351FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{CC}	Power Supply	0 to +7.0	Vdc
V_I	Input Voltage (V_{CC} = 5.0 V)	0 to V_{CC}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = V_{CC1} = V_{CC2} = 5.0 V ± 5.0%)†

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
ECL	Power Supply Current	–	50	–	45	–	50	mA
TTL		–	20	–	15	–	20	mA
	Reverse Current							µA
I_R	Pins 7, 8, 12, 14	–	25	–	20	–	25	
I_{INH}	Pin 9	–	100	–	80	–	100	
	Forward Current							mA
I_F	Pins 7, 8, 12, 14	–	–0.8	–	–0.6	–	–0.8	
I_{INL}	Pin 9	–	–3.2	–	–2.4	–	–3.2	
$V_{(BR)in}$	Input Breakdown Voltage	5.5	–	5.5	–	5.5	–	Vdc
V_I	Input Clamp Voltage (I_{in} = –18 mA)	–	–1.5	–	–1.5	–	–1.5	Vdc
V_{OH}	High Output Voltage (Note 1.)	3.98	4.16	4.02	4.19	4.08	4.27	Vdc
V_{OL}	Low Output Voltage (1)	3.05	3.37	3.05	3.37	3.05	3.37	Vdc
V_{IH}	High Input Voltage	2.0	–	2.0	–	2.0	–	Vdc
V_{IL}	Low Input Voltage	–	0.8	–	0.8	–	0.8	Vdc

1. With V_{CC} at 5.0 V. V_{OH}/V_{OL} change 1:1 with V_{CC}.

*Positive Emitter Coupled Logic

AC PARAMETERS

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
t_{pd}	Propagation Delay (Note 2)	0.4	2.2	0.4	2.2	0.4	2.1	ns
t_r	Rise Time (20% to 80%)	0.4	1.9	0.4	2.0	0.4	2.1	ns
t_f	Fall Time (80% to 20%)	0.4	1.9	0.4	2.0	0.4	2.1	ns
f_{max}	Maximum Operating Frequency	150	–	150	–	150	–	MHz

2. Propagation delay is measured on this circuit from +1.5 volts on the input waveform to the 50% point on the output waveform.

†Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to V_{CC} –2.0 Vdc.

MC10H352

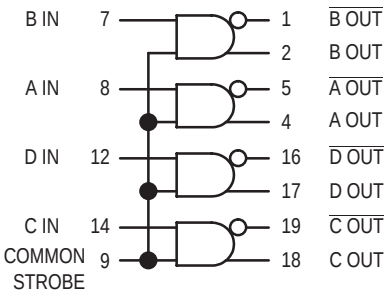
Quad CMOS to PECL* Translator

The MC10H352 is a quad translator for interfacing data between a CMOS logic section and the PECL section of digital systems when only a +5.0 Vdc power supply is available. The MC10H352 has CMOS compatible inputs and PECL complementary open–emitter outputs that allow use as an inverting/non–inverting translator or as a differential line driver. When the common strobe input is at a low logic level, it forces all true outputs to the PECL low logic state (≈ +3.2 V) and all inverting outputs to the PECL high logic state (≈ +4.1 V).

The MC10H352 can also be used with the MC10H350 to transmit and receive CMOS information differentially via balanced twisted pair lines.

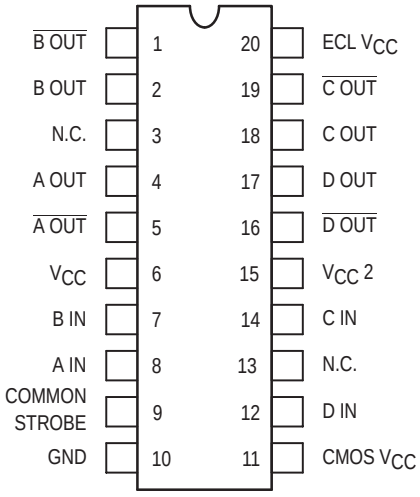
- Single +5.0 V Power Supply
- All V_{CC} Pins Isolated On Chip
- Differentially Drive Balanced Lines
- t_{pd} = 1.3 nsec Typical

LOGIC DIAGRAM



V_{CC} (+5.0 VDC) = PINS 6, 11, 15, 20
GND = PIN 10

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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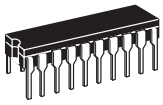
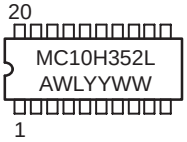
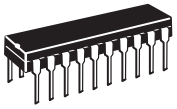
MARKING DIAGRAMS

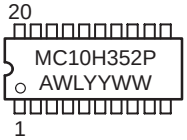


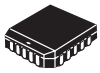
CDIP–20
L SUFFIX
CASE 732



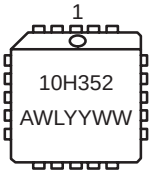


PDIP–20
P SUFFIX
CASE 738





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H352L	CDIP–20	18 Units/Rail
MC10H352P	PDIP–20	18 Units/Rail
MC10H352FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{CC}	Power Supply	0 to +7.0	Vdc
V_I	Input Voltage (V_{CC} = 5.0 V)	0 to V_{CC}	Vdc
I_{out}	Output Current — Continuous — Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range — Plastic — Ceramic	–55 to +150 –55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = V_{CC1} = V_{CC2} = 5.0 V ± 5.0%)†

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
ECL	Power Supply Current	—	50	—	45	—	50	mA
TTL		—	20	—	15	—	20	mA
I_R	Reverse Current Pins 7, 8, 12, 14 Pin 9	 — —	 25 100	 — —	 20 80	 — —	 25 100	µA
I_F	Forward Current Pins 7, 8, 12, 14 Pin 9	 — —	 –0.8 –3.2	 — —	 –0.6 –2.4	 — —	 –0.8 –3.2	mA
$V_{(BR)in}$	Input Voltage Breakdown	5.5	—	5.5	—	5.5	—	Vdc
V_I	Input Clamp Voltage (I_{in} = –18 mA)	—	–1.5	—	–1.5	—	–1.5	Vdc
V_{OH}	High Output Voltage (Note 1.)	3.98	4.16	4.02	4.19	4.08	4.27	Vdc
V_{OL}	Low Output Voltage (Note 1.)	3.05	3.37	3.05	3.37	3.05	3.37	Vdc
V_{IH}	High Input Voltage	3.15	—	3.15	—	3.15	—	Vdc
V_{IL}	Low Input Voltage	—	1.5	—	1.5	—	1.5	Vdc

1. With V_{CC} at 5.0 V. V_{OH}/V_{OL} change 1:1 with V_{CC}.

**Positive Emitter Coupled Logic

AC PARAMETERS

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
t_{pd}	Propagation Delay (Note 2.)	0.4	1.9	0.4	2.0	0.4	2.1	ns
t_r	Rise Time (20% to 80%)	0.4	1.9	0.4	2.0	0.4	2.1	ns
t_f	Fall Time (80% to 20%)	0.4	1.9	0.4	2.0	0.4	2.1	ns
f_{max}	Maximum Operating Frequency	150	—	150	—	150	—	MHz

2. Propagation delay is measured on this circuit from V_{CC}/2 on the input waveform to the 50% point on the output waveform.

†Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to V_{CC} – 2.0 Vdc.

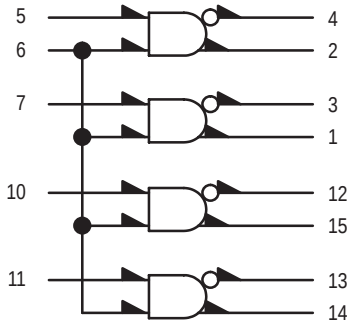
MC10H424

Quad TTL to ECL Translator with ECL Strobe

The MC10H424 is a Quad TTL–to–ECL translator with an ECL strobe. Power supply requirements are ground, +5.0 volts, and –5.2 volts.

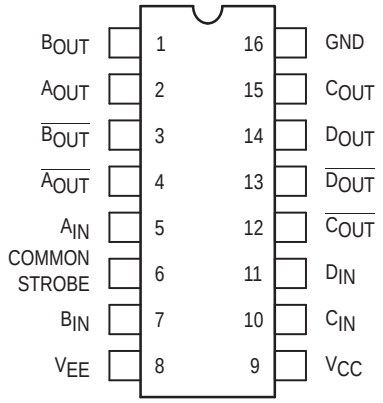
- Propagation Delay, 1.5 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K – Compatible

LOGIC DIAGRAM



GND = PIN 16
V_{CC} (+5.0 VDC) = PIN 9
V_{EE} (–5.2 VDC) = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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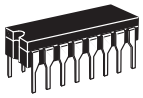
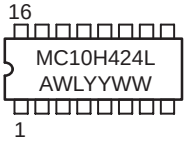
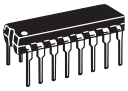
MARKING DIAGRAMS

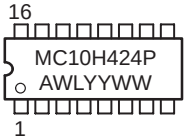


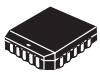
CDIP–16
L SUFFIX
CASE 620





PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H424L	CDIP–16	25 Units/Rail
MC10H424P	PDIP–16	25 Units/Rail
MC10H424FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 5.0 V)	–8.0 to 0	Vdc
V_{CC}	Power Supply (V_{EE} = – 5.2 V)	0 to +7.0	Vdc
V_I	Input Voltage (ECL)	0 to V_{EE}	Vdc
V_I	Input Voltage (TTL)	0 to V_{CC}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ± 5%, V_{CC} = 5.0 V ± 5.0%)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Negative Power Supply Drain Current	–	72	–	66	–	72	mAdc
I_{CCH}	Positive Power Supply Drain Current	–	16	–	16	–	18	mAdc
I_{CCL}		–	25	–	25	–	25	mAdc
I_R	Reverse Current Pin 5,7,10,11	–	50	–	50	–	50	μAdc
I_F	Forward Current Pin 5,7,10,11	–	–3.2	–	–3.2	–	–3.2	mAdc
I_{inH}	Input HIGH Current Pin 6	–	450	–	310	–	310	μAdc
I_{inL}	Input LOW Current Pin 6	0.5	–	0.5	–	0.3	–	μAdc
$V_{(BR)in}$	Input Breakdown Voltage	5.5	–	5.5	–	5.5	–	Vdc
V_I	Input Clamp Voltage	–	–1.5	–	–1.5	–	–1.5	Vdc
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage Pin 5,7,10,11	2.0	–	2.0	–	+2.0	–	Vdc
V_{IL}	Low Input Voltage Pin 5,7,10,11	–	0.8	–	0.8	–	0.8	Vdc
V_{IH}	High Input Voltage Pin 6	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage Pin 6	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

Propagation Delay Data Strobe	t_{pd}	 0.5 0.5	 2.2 2.2	 0.5 0.5	 2.3 2.3	 0.5 0.5	 2.4 2.4	ns
Rise Time	t_r	0.5	2.0	0.5	2.0	0.5	2.2	ns
Fall Time	t_f	0.5	2.0	0.5	2.0	0.5	2.2	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.1 volts.

APPLICATIONS INFORMATION

The MC10H424 has TTL–compatible inputs, an ECL strobe and MECL complementary open–emitter outputs that allow use as an inverting/non–inverting translator or as a differential line driver. When the common strobe input is at the low–logic level, it forces all true outputs to a MECL low–logic state and all inverting outputs to a MECL high–logic state.

An advantage of this device is that TTL–level information can be transmitted differentially, via balanced twisted pair lines, to MECL equipment, where the signal can be received by the MC10H115 or MC10H116 differential line receivers.

MC10H600, MC100H600

9-Bit TTL to ECL Translator

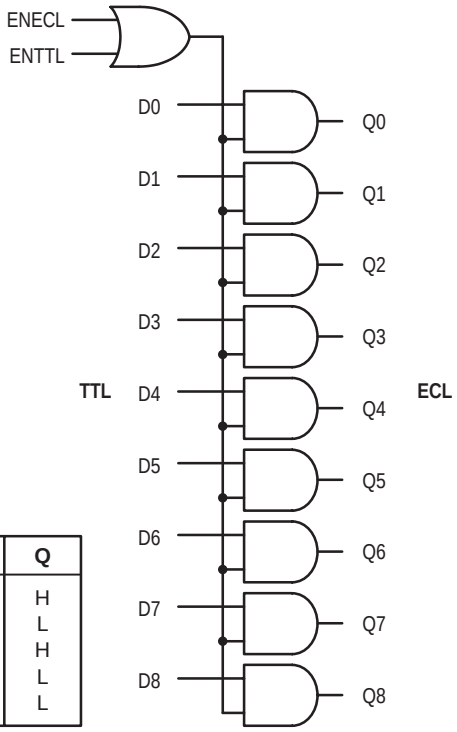
The MC10H/100H600 is a 9–bit, dual supply TTL to ECL translator. Devices in the Motorola 9–bit translator series utilize the 28–lead PLCC for optimal power pinning, signal flow–through and electrical performance.

The H600 features both ECL and TTL logic enable controls for maximum flexibility.

The 10H version is compatible with MECL 10H ECL logic levels. The 100H version is compatible with 100K levels.

- 9–Bit Ideal for Byte–Parity Applications
- Flow–Through Configuration
- Extra TTL and ECL Power/Ground Pins to Minimize Switching Noise
- ECL and TTL Enable Inputs
- Dual Supply
- 3.5 ns Max D to Q
- PNP TTL Inputs for Low Loading
- Choice of ECL Compatibility: MECL 10H (10Hxxx) or 100K (100Hxxx)

LOGIC SYMBOL



TRUTH TABLE

ENECL	ENTTL	D	Q
H	X	H	H
H	X	L	L
X	H	H	H
X	H	L	L
L	L	X	L

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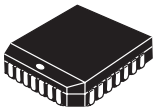
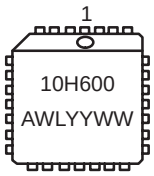


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAM

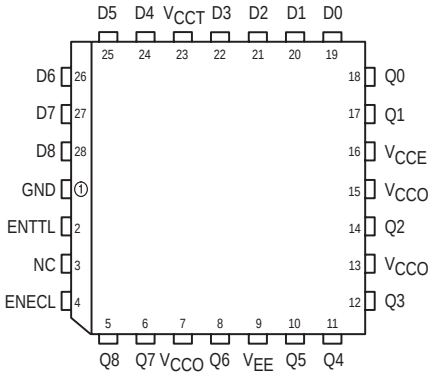


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN NAMES

PIN	FUNCTION
GND	TTL Ground (0 V)
V_{CCE}	ECL V_{CC} (0 V)
V_{CCO}	ECL V_{CC} (0 V) — Outputs
V_{CCT}	TTL Supply (+5.0 V)
V_{EE}	ECL Supply (–5.2/–4.5 V)
D0–D8	Data Inputs (TTL)
Q0–Q8	Data Outputs (ECL)
ENECL	Enable Control (ECL)
ENTTL	Enable Control (TTL)

Pinout: 28–Lead PLCC (Top View)



ORDERING INFORMATION

Device	Package	Shipping
MC10H600FN	PLCC–28	37 Units/Rail
MC100H600FN	PLCC–28	37 Units/Rail

DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ± 5% (10H version); V_{EE} = –4.2 V to –5.5 V (100H version)

Symbol	Parameter		0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
	Power Supply Current									
I_{EE}	ECL	10H 100H		–125 –122		–125 –123		–125 –132	mA	
I_{CCH} I_{CCL}	TTL			48 50		48 50		48 50	mA	

AC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ± 5% (10H version); V_{EE} = –4.2 V to –5.5 V (100H version)

Symbol	Parameter		0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay to Output	D	1.4	3.0	1.5	3.2	1.7	3.5	ns	50 Ω to –2.0 V
		ENECL / ENTTL	1.8	3.7	1.9	3.9	2.0	4.1	ns	50 Ω to –2.0 V
t_R t_F	Output Rise/Fall Time 20%–80%		0.5	1.5	0.5	1.5	0.5	1.5	ns	50 Ω to –2.0 V

10H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ± 5%

Symbol	Parameter	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	145	 0.5	145	µA µA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1170 –1950	–840 –1480	–1130 –1950	–810 –1480	–1070 –1950	–735 –1450	mV	
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	–1020 –1950	–840 –1630	–980 –1950	–810 –1630	–920 –1950	–735 –1600	mV	50 Ω to –2.0 V

100H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –4.2 V to –5.5 V

Symbol	Parameter	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	145	 0.5	145	µA µA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	mV	
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	–1025 –1810	–880 –1620	–1025 –1810	–880 –1620	–1025 –1810	–880 –1620	mV	50 Ω to –2.0 V

TTL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ± 5% (10H version); V_{EE} = –4.2 V to –5.5 V (100H version)

Symbol	Parameter	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0	 0.8	2.0	 0.8	2.0	 0.8	V V	
I_{IH}	Input HIGH Current		20 100		20 100		20 100	µA	V_{IN} = 2.7 V V_{IN} = 7.0 V
I_{IL}	Input LOW Current		–0.6		–0.6		–0.6	mA	V_{IN} = 0.5 V
V_{IK}	Input Clamp Voltage		–1.2		–1.2		–1.2	V	I_{IN} = –18 mA

MC10H601, MC100H601

9-Bit ECL to TTL Translator

The MC10H/100H601 is a 9–bit, dual supply ECL to TTL translator. Devices in the Motorola 9–bit translator series utilize the 28–lead PLCC for optimal power pinning, signal flow–through and electrical performance.

The devices feature a 48 mA TTL output stage, and AC performance is specified into both a 50 pF and 200 pF load capacitance. For the 3–state output disable, both ECL and TTL control inputs are provided, allowing maximum design flexibility.

The 10H version is compatible with MECL 10H ECL logic levels. The 100H version is compatible with 100K levels.

- 9–Bit Ideal for Byte–Parity Applications
- 3–State TTL Outputs
- Flow–Through Configuration
- Extra TTL and ECL Power Pins to Minimize Switching Noise
- ECL and TTL 3–State Control Inputs
- Dual Supply
- 4.8 ns Max Delay into 50 pF, 9.6 ns into 200 pF (all outputs switching)
- PNP TTL Inputs for Low Loading

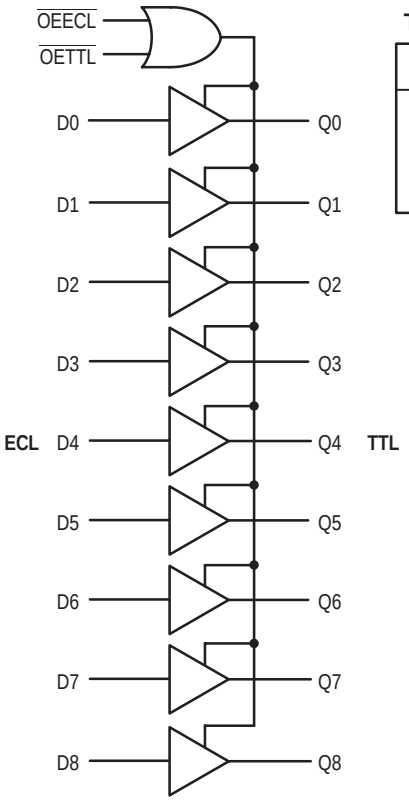


Figure 1. Logic Diagram

TRUTH TABLE

$\overline{OEECL}$	$\overline{OETTL}$	D	Q
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

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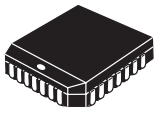
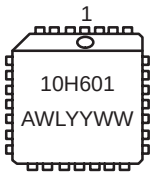


PLCC–28
FN SUFFIX
CASE 776

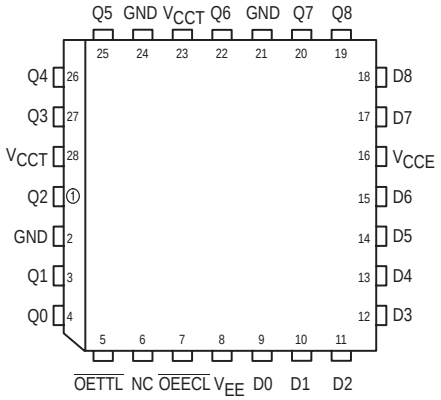
MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN NAMES

PIN	FUNCTION
GND	TTL Ground (0 V)
V_{CCE}	ECL V_{CC} (0 V)
V_{CCT}	TTL Supply (+5.0 V)
V_{EE}	ECL Supply (–5.2/–4.5 V)
D0–D8	Data Inputs (ECL)
Q0–Q8	Data Outputs (TTL)
$\overline{OEECL}$	3–State Control (ECL)
$\overline{OETTL}$	3–State Control (TTL)



Pinout: 28–Lead PLCC (Top View)

ORDERING INFORMATION

Device	Package	Shipping
MC10H601FN	PLCC–28	37 Units/Rail
MC100H601FN	PLCC–28	37 Units/Rail

10H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ± 5%

Symbol	Parameter	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{EE}	Power Supply Current		–51		–51		–51	mA	
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	145	 0.5	145	µA µA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1170 –1950	–840 –1480	–1130 –1950	–810 –1480	–1060 –1950	–720 –1445	mV	

100H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –4.2 V to –5.5 V

Symbol	Parameter	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{EE}	Power Supply Current		–51		–51		–53	mA	
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	145	 0.5	145	µA µA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	mV	

TTL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ± 5% (10H version);
V_{EE} = –4.2 V to –5.5 V (100H version)

Symbol	Parameter	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{CCH}	Power Supply Current		110		110		110	mA	
I_{CCL}			110		110		110		
I_{CCZ}	Power Supply Current		105		105		105		
I_{IH}	Input HIGH Current		20 100		20 100		20 100	µA	V_{IN} = 2.7 V V_{IN} = 7.0 V
I_{IL}	Input LOW Current		–0.6		–0.6		–0.6	mA	V_{IN} = 0.5 V
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0 V
I_{OZH} I_{OZL}	Output Disable Current HIGH Output Disable Current LOW	 –50	50	 –50	50	 –50	50	µA	V_{OUT} = 2.7 V V_{OUT} = 0.5 V
V_{IHT} V_{ILT}	Input HIGH Voltage Input LOW Voltage	2.0	 0.8	2.0	 0.8	2.0	 0.8	V	
V_{OHT}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = –3.0 mA I_{OH} = –15 mA
V_{OLT}	Output LOW Voltage		0.55		0.55		0.55	V	I_{OL} = 48 mA
V_{IK}	Input Clamp Voltage		–1.2		–1.2		–1.2	V	I_{IN} = –18 mA

AC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ± 5% (10H version);
V_{EE} = –4.2 V to –5.5 V (100H version)

Symbol	Parameter		0°C		25°C		85°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output		1.7 3.4	4.8 9.6	1.7 3.4	4.8 9.6	1.7 3.4	4.8 9.6	ns ns	C_L = 50 pF C_L = 200 pF
t_{PLZ} t_{PHZ}	Output Disable Time	$\overline{OEECL}$	3.7 5.4	6.5 13	3.7 5.4	6.5 13	3.7 5.4	6.5 13	ns ns	C_L = 50 pF C_L = 200 pF
t_{PLZ} t_{PHZ}		$\overline{OETTL}$	4.3 7.0	7.5 15	4.3 7.0	7.5 15	4.3 7.0	7.5 15	ns ns	C_L = 50 pF C_L = 200 pF
t_{PZL} t_{PZH}	Output Enable Time	$\overline{OEECL}$	3.5 5.0	6.0 12	3.5 5.0	6.0 12	3.5 5.0	6.0 12	ns ns	C_L = 50 pF C_L = 200 pF
t_{PZL} t_{PZH}		$\overline{OETTL}$	4.2 6.0	7.0 14	4.2 6.0	7.0 14	4.2 6.0	7.0 14	ns ns	C_L = 50 pF C_L = 200 pF
t_R t_F	Output Rise/Fall Time 1.0 V – 2.0 V			1.2 3.0		1.2 3.0		1.2 3.0	ns ns	C_L = 50 pF C_L = 200 pF

MC10H602, MC100H602

9-Bit Latch TTL to ECL Translator

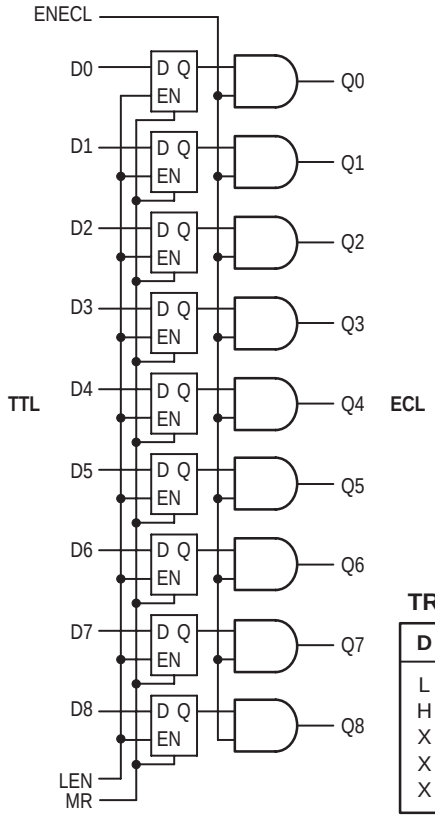
The MC10H/100H602 is a 9–bit, dual supply TTL to ECL translator with latch. Devices in the Motorola 9–bit translator series utilize the 28–lead PLCC for optimal power pinning, signal flow–through and electrical performance.

The H602 features D–type latches. Latching is controlled by Latch Enable (LEN), while the Master Reset input resets the latches. A post–latch logic enable is also provided (ENECL), allowing control of the output state without destroying latch data. All control inputs are ECL level.

The 10H version is compatible with MECL 10H ECL logic levels. The 100H version is compatible with 100K levels.

- 9–Bit Ideal for Byte–Parity Applications
- Flow–Through Configuration
- Extra TTL and ECL Power/Ground Pins to Minimize Switching Noise
- Dual Supply
- 3.5 ns Max D to Q
- PNP TTL Inputs for Low Loading

LOGIC SYMBOL



TRUTH TABLE

D	LEN	MR	ENECL	Q
L	L	L	H	L
H	L	L	H	H
X	H	L	H	Q_0
X	X	H	H	L
X	X	X	L	L

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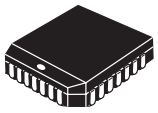
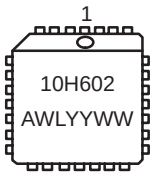


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAM

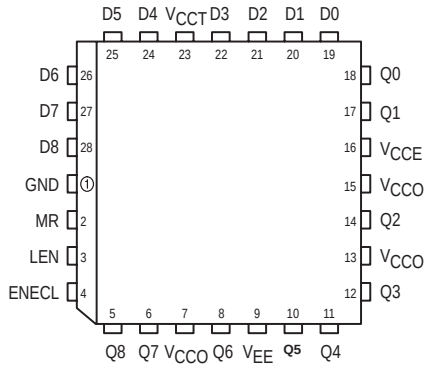


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN NAMES

PIN	FUNCTION
GND	TTL Ground (0 V)
V_{CCE}	ECL V_{CC} (0 V)
V_{CCO}	ECL V_{CC} (0 V) — Outputs
V_{CCT}	TTL Supply (+5.0 V)
V_{EE}	ECL Supply (–5.2/–4.5 V)
D0–D8	Data Inputs (TTL)
Q0–Q8	Data Outputs (ECL)
ENECL	Enable Control (ECL)
LEN	Latch Enable (ECL)
MR	Master Reset (ECL)

Pinout: 28–Lead PLCC (Top View)



ORDERING INFORMATION

Device	Package	Shipping
MC10H602FN	PLCC–28	37 Units/Rail
MC100H602FN	PLCC–28	37 Units/Rail

DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ± 5% (10H version); V_{EE} = –4.2 V to –5.5 V (100H version)

Symbol	Parameter		0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
	Power Supply Current									
I_{EE}	ECL	10H 100H		–125 –122		–125 –123		–125 –132	mA	
I_{CCH} I_{CCL}	TTL			48 50		48 50		48 50	mA	

AC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ± 5% (10H version); V_{EE} = –4.2 V to –5.5 V (100H version)

Symbol	Parameter		0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay to Output	D LEN MR ENECL	1.4 2.0 2.0 1.6	3.0 3.4 3.4 3.2	1.5 2.1 2.1 1.7	3.2 3.5 3.5 3.3	1.7 2.4 2.5 1.8	3.5 3.7 3.9 3.7	ns	
t_S	Set–Up Time, D to LEN		2.0		2.0		2.0		ns	
t_h	Hold Time, D to LEN		1.0		1.0		1.0		ns	
$t_{W}(L)$	LEN Pulse Width, LOW		2.0		2.0		2.0		ns	
t_R t_F	Output Rise/Fall Time 20%–80%		0.5	1.5	0.5	1.5	0.5	1.5	ns	

10H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ± 5%

Symbol	Parameter	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	 0.5	225 	 0.5	145 	 0.5	145 	µA µA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1170 –1950	–840 –1480	–1130 –1950	–810 –1480	–1070 –1950	–735 –1450	mV	
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	–1020 –1950	–840 –1630	–980 –1950	–810 –1630	–920 –1950	–735 –1600	mV	50 Ω to –2.0 V

100H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –4.2 V to –5.5 V

Symbol	Parameter	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	 0.5	225 	 0.5	145 	 0.5	145 	µA µA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	mV	
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	–1025 –1810	–880 –1620	–1025 –1810	–880 –1620	–1025 –1810	–880 –1620	mV	50 Ω to –2.0 V

TTL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ± 5% (10H version); V_{EE} = –4.2 V to –5.5 V (100H version)

Symbol	Parameter	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0 	 0.8	2.0 	 0.8	2.0 	 0.8	V V	
I_{IH}	Input HIGH Current		20 100		20 100		20 100	µA	V_{IN} = 2.7 V V_{IN} = 7.0 V
I_{IL}	Input LOW Current		–0.6		–0.6		–0.6	mA	V_{IN} = 0.5 V
V_{IK}	Input Clamp Voltage		–1.2		–1.2		–1.2	V	I_{IN} = –18 mA

MC10H603, MC100H603

9-Bit Latch ECL to TTL Translator

The MC10H/100H603 is a 9–bit, dual supply ECL to TTL translator. Devices in the Motorola 9–bit translator series utilize the 28–lead PLCC for optimal power pinning, signal flow–through and electrical performance.

The devices feature a 48 mA TTL output stage, and AC performance is specified into both a 50 pF and 200 pF load capacitance. Latching is controlled by Latch Enable (LEN), and Master Reset (MR) resets the latches. A HIGH on $\overline{\text{OEECL}}$ sends the outputs into the high impedance state. All control inputs are ECL level.

The 10H version is compatible with MECL 10H ECL logic levels. The 100H version is compatible with 100K levels.

- 9–Bit Ideal for Byte–Parity Applications
- 3–State TTL Outputs
- Flow–Through Configuration
- Extra TTL and ECL Power Pins to Minimize Switching Noise
- Dual Supply
- 6.0 ns Max Delay into 50 pF, 12 ns into 200 pF (all outputs switching)
- PNP TTL Inputs for Low Loading

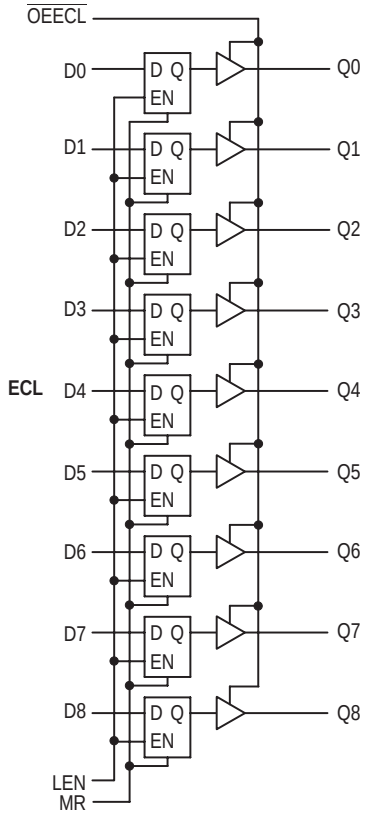


Figure 2. Logic Diagram

TRUTH TABLE

D	LEN	MR	$\overline{\text{OEECL}}$	Q
L	L	L	L	L
H	L	L	L	H
X	H	L	L	Q_0
X	X	H	L	L
X	X	X	H	Z

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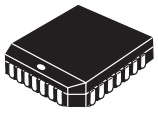
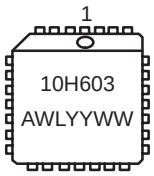


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN NAMES

PIN	FUNCTION
GND	TTL Ground (0 V)
V_{CCE}	ECL V_{CC} (0 V)
V_{CCT}	TTL Supply (+5.0 V)
V_{EE}	ECL Supply (–5.2/–4.5 V)
D0–D8	Data Inputs (ECL)
Q0–Q8	Data Outputs (TTL)
$\overline{\text{OEECL}}$	3-State Control (ECL)
LEN	Latch Enable (ECL)
MR	Master Reset (ECL)

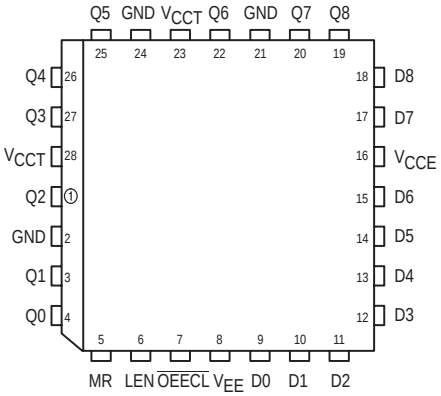


Figure 1. 28–Lead Pinout (Top View)

ORDERING INFORMATION

Device	Package	Shipping
MC10H603FN	PLCC–28	37 Units/Rail
MC100H603FN	PLCC–28	37 Units/Rail

10H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ± 5%

Symbol	Parameter	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{EE}	Power Supply Current		–64		–64		–64	mA	
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	145	 0.5	145	µA µA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1170 –1950	–840 –1480	–1130 –1950	–810 –1480	–1060 –1950	–720 –1445	mV	

100H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –4.2 V to –5.5 V

Symbol	Parameter	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{EE}	Power Supply Current		–63		–64		–68	mA	
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	145	 0.5	145	µA µA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	mV	

TTL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ± 5% (10H version);
V_{EE} = –4.2 V to –5.5 V (100H version)

Symbol	Parameter	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{CCH}	Power Supply Current		110		110		110	mA	
I_{CCL}			110		110		110		
I_{CCZ}	Power Supply Current		110		110		110		
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0 V
I_{OZH} I_{OZL}	Output Disable Current HIGH Output Disable Current LOW		50 –50		50 –50		50 –50	µA	V_{OUT} = 2.7 V V_{OUT} = 0.5 V
V_{OHT}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = –3.0 mA I_{OH} = –15 mA
V_{OLT}	Output LOW Voltage		0.55		0.55		0.55	V	I_{OL} = 48 mA

AC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ± 5% (10H version);
V_{EE} = –4.2 V to –5.5 V (100H version)

Symbol	Parameter		0°C		25°C		85°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output	D	3.0 6.4	6.0 12	3.0 6.4	6.0 12	3.0 6.4	6.0 12	ns ns	C_L = 50 pF C_L = 200 pF
		LEN	3.5 7.0	6.5 13	3.5 7.0	6.5 13	3.5 7.0	6.5 13	ns ns	C_L = 50 pF C_L = 200 pF
		MR	3.0 6.0	6.0 12	3.0 6.0	6.0 12	3.0 6.0	6.0 12	ns ns	C_L = 50 pF C_L = 200 pF
t_{PLZ} t_{PHZ}	Output Disable Time		2.5 4.2	6.5 13	2.5 4.2	6.5 13	2.5 4.2	6.5 13	ns ns	C_L = 50 pF C_L = 200 pF
t_{PZL} t_{PZH}	Output Enable Time		2.0 4.0	5.0 10	2.0 4.0	5.0 10	2.0 4.0	5.0 10	ns ns	C_L = 50 pF C_L = 200 pF
t_s	Setup Time	D to LEN	1.5		1.5		1.5		ns	
t_h	Hold Time	D to LEN	0.8		0.8		0.8		ns	
$t_{w(L)}$	LEN Pulse Width, LOW		2.0		2.0		2.0		ns	
t_R t_F	Output Rise/Fall Time 1.0 V–2.0 V		0.2 0.2	1.2 3.0	0.2 0.2	1.2 3.0	0.2 0.2	1.2 3.0	ns ns	C_L = 50 pF C_L = 200 pF

MC10H604, MC100H604

Registered Hex TTL to ECL Translator

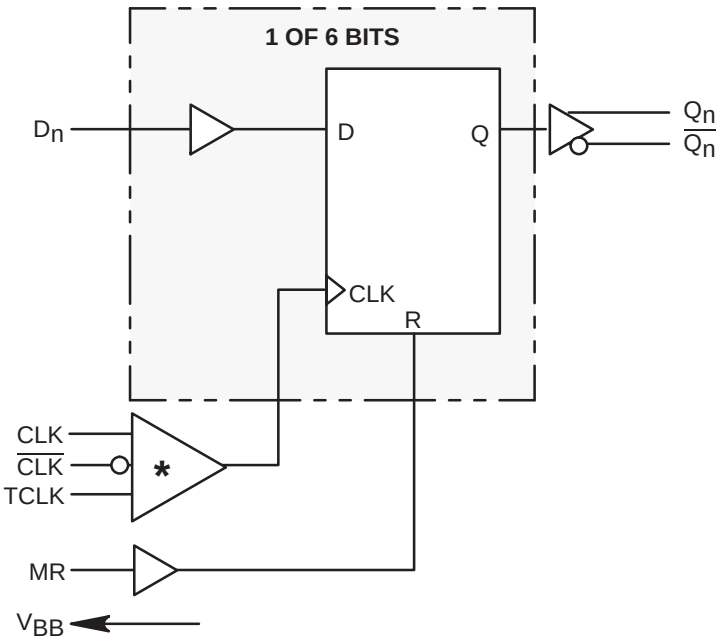
The MC10H/100H604 is a 6–bit, registered, dual supply TTL to ECL translator. The device features differential ECL outputs as well as a choice between either a differential ECL clock input or a TTL clock input. The asynchronous master reset control is an ECL level input..

With its differential ECL outputs and TTL inputs the H604 device is ideally suited for the transmit function of a HPPI bus type board–to–board interface application. The on chip registers simplify the task of synchronizing the data between the two boards.

The device is available in either ECL standard: the 10H device is compatible with MECL 10KH logic levels while the 100H device is compatible with 100K logic levels.

- Differential 50Ω ECL Outputs
- Choice Between Differential ECL or TTL Clock Input
- Dual Power Supply
- Multiple Power and Ground Pins to Minimize Noise
- Specified Within–Device Skew

LOGIC SYMBOL



* 1. When using MECL inputs, TCLK must be tied to ground (0V).
2. When using only one MECL input, the unused MECL input must be tied to V_{BB}, and TCLK must be tied to ground (0V).
3. When using TCLK, both MECL inputs must be tied to V_{EE} (–5.2V).

TRUTH TABLE

Dn	MR	TCLK/CLK	Qn+1
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition

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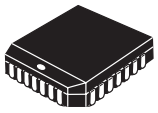
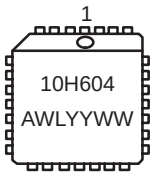


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAM

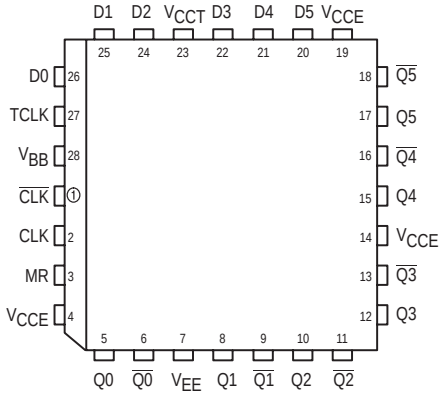


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN NAMES

PIN	FUNCTION
D0–D5	TTL Data Inputs
CLK, $\overline{CLK}$	Differential ECL Clock Input
TCLK	TTL Clock Input
MR	ECL Master Reset Input
Q0–Q5	True ECL Outputs
$\overline{Q0}$–$\overline{Q5}$	Inverted ECL Outputs
V_{CCE}	ECL V_{CC} (0V)
V_{CCT}	TTL V_{CC} (+5.0V)
V_{EE}	ECL V_{EE} (–5.2V)

Pinout: 28–Lead PLCC (Top View)



ORDERING INFORMATION

Device	Package	Shipping
MC10H604FN	PLCC–28	37 Units/Rail
MC100H604FN	PLCC–28	37 Units/Rail

DC CHARACTERISTICS: VEE = VEE(Min) to VEE(Max); VCCE = GND; VCCT = 5.0V +10%

Symbol	Parameter	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{EE}	ECL Power Supply Current 10H 100H		130 130		130 140		130 150	mA	
I_{CCH} I_{CCL}	TTL Power Supply Current		35 45		35 45		35 45	mA	

10H ECL DC CHARACTERISTICS: V_{CCT} = +5.0 V ± 10%; V_{EE} = –5.20 V ±5%

Symbol	Parameter	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	0.5	225	0.5	145	0.5	145	µA µA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1170 –1950	–840 –1480	–1130 –1950	–810 –1480	–1060 –1950	–720 –1480	mV	
V_{BB}	Output Bias Voltage	–1400	–1290	–1370	–1270	–1330	–1210	mV	
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	–1020 –1950	–840 –1630	–980 –1950	–810 –1630	–910 –1950	–720 –1595	mV	50 Ω to –2.0 V

100H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –4.2 V to –5.5 V

Symbol	Parameter	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	0.5	225	0.5	145	0.5	145	µA µA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	mV	
V_{BB}	Output Bias Voltage	–1400	–1280	–1400	–1280	–1400	–1280	mV	
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	–1025 –1810	–880 –1620	–1025 –1810	–880 –1620	–1025 –1810	–880 –1620	mV	50 Ω to –2.0 V

TTL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ± 5% (10H version); V_{EE} = –4.2 V to –5.5 V (100H version)

Symbol	Parameter	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0	0.8	2.0	0.8	2.0	0.8	V V	
I_{IH}	Input HIGH Current		20 100		20 100		20 100	µA	V_{IN} = 2.7 V V_{IN} = 7.0 V
I_{IL}	Input LOW Current		–0.6		–0.6		–0.6	mA	V_{IN} = 0.5 V
V_{IK}	Input Clamp Voltage		–1.2		–1.2		–1.2	V	I_{IN} = –18 mA

AC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ± 5% (10H version); V_{EE} = –4.2 V to –5.5 V (100H version)

Symbol	Parameter	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay CLK to Q to Output TCLK to Q MR to Q	1.5 2.0 1.5		3.5 4.0 4.0	1.5 2.0 1.5		3.5 4.0 4.0	1.5 2.0 1.5		3.5 4.0 4.0	ns	50Ω to –2.0V
t_S	Setup Time	1.5	0.5		1.5	0.5		1.5	0.5		ns	50Ω to –2.0V
t_H	Hold Time	1.5	0.5		1.5	0.5		1.5	0.5		ns	50Ω to –2.0V
t_{PW}	Minimum Pulse Width CLK, MR		1.0			1.0			1.0		ns	50Ω to –2.0V
V_{PP}	Minimum Input Swing					150					mV	
t_r t_f	Rise/Fall Times	0.3	1.0	2.0	0.3	1.0	2.0	0.3	1.0	2.0	ns	20% – 80%

MC10H605, MC100H605

Registered Hex ECL to TTL Translator

The MC10/100H605 is a 6–bit, registered, dual supply ECL to TTL translator. The device features differential ECL inputs for both data and clock. The TTL outputs feature balanced 24mA sink/source capabilities for driving transmission lines.

With its differential ECL inputs and TTL outputs the H605 device is ideally suited for the receive function of a HPPI bus type board–to–board interface application. The on chip registers simplify the task of synchronizing the data between the two boards.

A V_{BB} reference voltage is supplied for use with single–ended data or clock. For single–ended applications the V_{BB} output should be connected to the "bar" inputs ($\overline{Dn}$ or $\overline{CLK}$) and bypassed to ground via a 0.01μF capacitor. To minimize the skew of the device differential clocks should be used.

The ECL level Master Reset pin is asynchronous and common to all flip–flops. A "HIGH" on the Master Reset forces the Q outputs "LOW".

The device is available in either ECL standard: the 10H device is compatible with MECL 10H™ logic levels while the 100H device is compatible with 100K logic levels.

- Differential ECL Data and Clock Inputs
- 24mA Sink, 24mA Source TTL Outputs
- Dual Power Supply
- Multiple Power and Ground Pins to Minimize Noise
- 2.0ns Part–to–Part Skew

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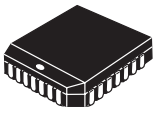
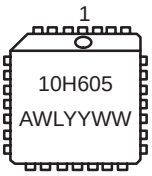


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAM

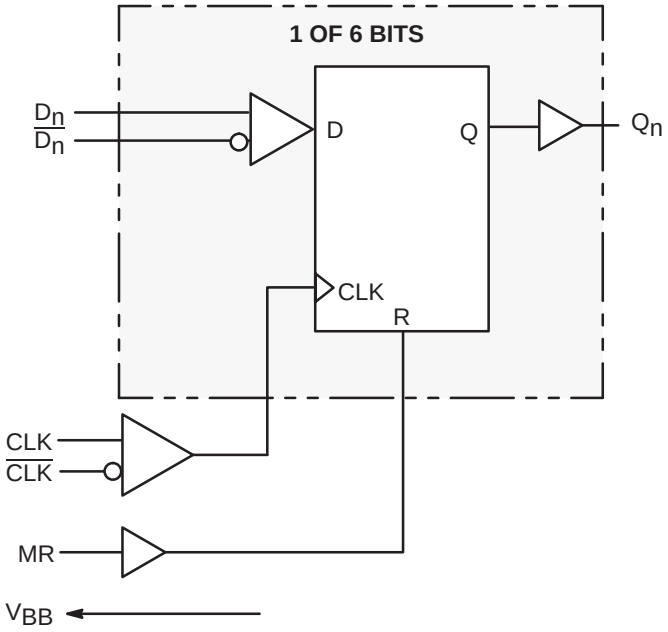


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H605FN	PLCC–28	37 Units/Rail
MC100H605FN	PLCC–28	37 Units/Rail

LOGIC DIAGRAM

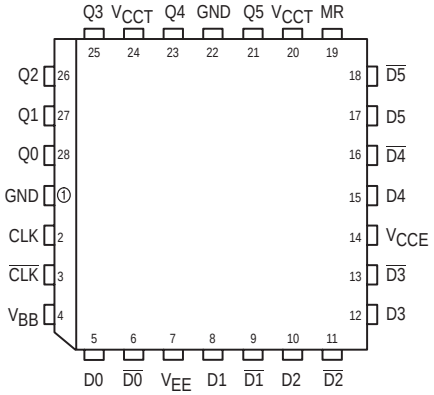


TRUTH TABLE

Dn	MR	TCLK/CLK	Qn+1
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition

Pinout: 28–Lead PLCC (Top View)



PIN NAMES

PIN	FUNCTION
D0–D5	True ECL Data Inputs
D0–D5	Inverted ECL Data Inputs
CLK, CLK	Differential ECL Clock Input
MR	ECL Master Reset Input
Q0–Q5	TTL Outputs
V_{CCE}	ECL V_{CC}
V_{CCT}	TTL V_{CC}
GND	TTL Ground
V_{EE}	ECL V_{EE}

10H ECL DC CHARACTERISTICS (V_{CCT} = +5.0V ±10%; V_{EE} = –5.20V ±5%)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{EE}	Supply Current		63	75		63	75		61	75	mA	
I_{INH}	Input HIgh Current			225			145			145	µA	
I_{INL}	Input Low Current	0.5			0.5			0.5			µA	
V_{IH}	Input High Voltage	–1170		–840	–1130		–810	–1060		–720	mV	
V_{IL}	Input Low Voltage	–1950		–1480	–1950		–1480	–1950		–1480	mV	
V_{BB}	Output Bias Voltage	–1400		–1280	–1370		–1270	–1330		–1210	mV	
V_{Diff}	Input Differential Voltage	150			150			150			mV	
V_{max} CMRR	Input Common Mode Reject Range			0			0			0	mV	
V_{min} CMRR	Input Common Mode Reject Range	–2800 –3000 –3300			–2800 –3000 –3300			–2800 –3000 –3300			mV	V_{EE} = –4.94 V_{EE} = –5.20 V_{EE} = –5.46

100H ECL DC CHARACTERISTICS (V_{CCT} = +5.0V ±5%; V_{EE} = –4.2V to 5.5V)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{EE}	Supply Current		65	75		65	75		70	85	mA	
I_{INH}	Input HIgh Current			225			145			145	µA	
I_{INL}	Input Low Current	0.5			0.5			0.5			µA	
V_{IH}	Input High Voltage	–1165		–880	–1165		–880	–1165		–880	mV	
V_{IL}	Input Low Voltage	–1810		–1475	–1810		–1475	–1810		–1475	mV	
V_{BB}	Reference Voltage	–1400		–1280	–1400		–1280	–1400		–1200	mV	
V_{Diff}	Input Differential Voltage	150			150			150			mV	
V_{max} CMRR	Input Common Mode Reject Range			0			0			0	mV	
V_{min} CMRR	Input Common Mode Reject Range	–2000 –2200 –2400			–2000 –2200 –2400			–2000 –2200 –2400			mV	V_{EE} = –4.20 V_{EE} = –4.50 V_{EE} = –4.80

* NOTE: DO NOT short the ECL inputs to the TTL V_{CC}.

TTL DC CHARACTERISTICS (V_{CCT} = +5.0V ±10%; V_{EE} = –5.2V ±5% (10H); V_{EE} = –4.2V to 5.5V (100H))

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{CCL}	Supply Current		65	75		65	75		65	75	mA	Outputs Low
I_{CCH}	Supply Current		65	75		65	75		65	75	mA	Outputs High
V_{OL}	Output Low Voltage			500			500			500	mV	I_{OL} = 24mA
V_{OH}	Output High Voltage	2.5			2.5			2.5			mV	I_{OH} = 24mA
I_{OS}	Output Short Circuit Current	100		225	100		225	100		225	mA	V_{OUT} = 0V

AC TEST LIMITS (V_{CCT} = +5.0V ±10%; V_{EE} = –5.2V ±5% (10H); V_{EE} = –4.2V to 5.5V (100H))

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH}	Propagation Delay CLK to Q (Diff) CLK to Q (SE)	 4.5 4.3	 5.3 5.3	 6.5 6.7	 4.5 4.3	 5.4 5.4	 6.5 6.7	 4.5 4.3	 5.6 5.6	 6.5 6.7	ns	Across P.S. and Temp C_L = 50pF
t_{PHL}	Propagation Delay CLK to Q (Diff) CLK to Q (SE)	 4.0 3.8	 5.0 5.0	 6.0 6.2	 4.0 3.8	 5.1 5.1	 6.0 6.2	 4.0 3.8	 5.5 5.5	 6.0 6.2	ns	Across P.S. and Temp C_L = 50pF
t_{PHL}	Propagation Delay MR to Q	2.5	4.9	7.0	2.5	5.2	7.0	3.0	5.8	7.5	ns	Across P.S. and Temp C_L = 50pF
t_{SKEW}	Device Skew Part–to–Part (Diff) Within–Device		 1.0 0.3	 2.0 0.7		 1.0 0.3	 2.0 0.7		 1.0 0.3	 2.0 0.7	ns	C_L = 50pF
t_S	Setup Time	1.5			1.5			1.5			ns	
t_H	Hold Time	1.5			1.5			1.5			ns	
t_{PW}	Minimum Pulse Width CLK	1.0			1.0			1.0			ns	
t_{PW}	Minimum Pulse Width MR	1.0			1.0			1.0			ns	
V_{PP}	Minimum Input Swing	150			150			150			mV	Peak–to–Peak
t_r	Rise Time	0.7	1.0	1.5	0.7	1.0	1.5	0.7	1.0	1.5	ns	1V to 2V
t_f	Fall Time	0.5	0.7	1.2	0.5	0.7	1.2	0.5	0.7	1.2	ns	1V to 2V
t_{RR}	Reset/Recovery Time	2.5			2.5			2.5			ns	

MC10H606, MC100H606

Registered Hex TTL to PECL Translator

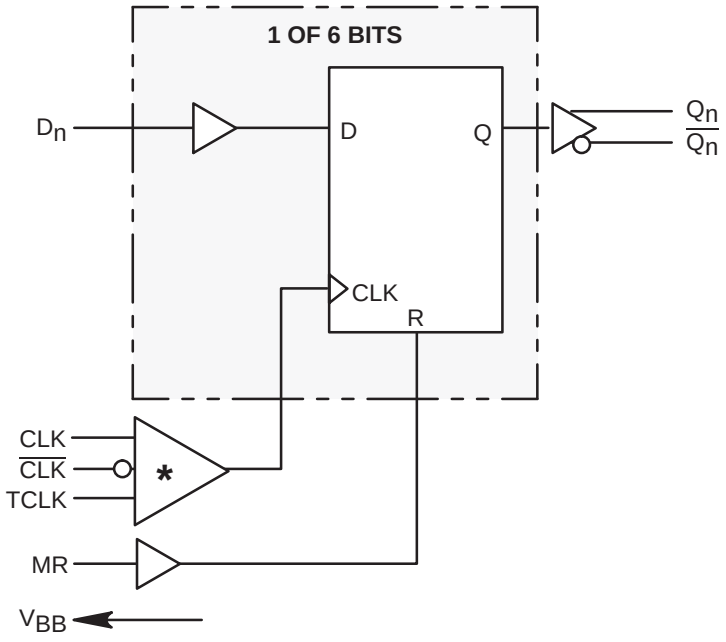
The MC10/100H606 is a 6–bit, registered, single supply TTL to PECL translator. The device features differential PECL outputs as well as a choice between either a differential PECL clock input or a TTL clock input. The asynchronous master reset control is a PECL level input.

With its differential PECL outputs and TTL inputs the H606 device is ideally suited for the transmit function of a HPPI bus type board–to–board interface application. The on chip registers simplify the task of synchronizing the data between the two boards.

The device is available in either ECL standard: the MECL™ 10H device is compatible with MECL 10KH logic levels, with a V_{CC} of +5 volts while the 100H device is compatible with 100K logic levels, with a V_{CC} of +5 volts.

- Differential 50Ω ECL Outputs
- Choice Between Differential PECL or TTL Clock Input
- Single Power Supply
- Multiple Power and Ground Pins to Minimize Noise

LOGIC SYMBOL



* 1. When using PECL inputs, TCLK must be tied to ground (0V).
2. When using only one PECL input, the unused PECL input must be tied to V_{BB}, and TCLK must be tied to ground (0V).
3. When using TCLK, both PECL inputs must be tied to ground (0V).

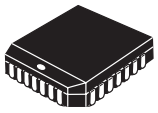
TRUTH TABLE

Dn	MR	TCLK/CLK	Qn+1
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition

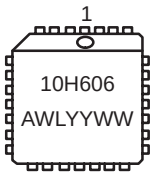
ON Semiconductor

http://onsemi.com



PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAM

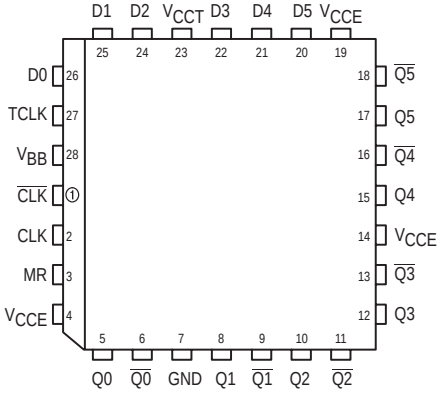


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN NAMES

PIN	FUNCTION
D0–D5	TTL Data Inputs
CLK, $\overline{CLK}$	Differential PECL Clock Input
TCLK	TTL Clock Input
MR	PECL Master Reset Input
Q0–Q5	True PECL Outputs
$\overline{Q0}$–$\overline{Q5}$	Inverted PECL Outputs
V_{CCE}	PECL V_{CC} (+5.0V)
V_{CCT}	TTL V_{CC} (+5.0V)
GND	TTL/PECL Ground

Pinout: 28–Lead PLCC (Top View)



ORDERING INFORMATION

Device	Package	Shipping
MC10H606FN	PLCC–28	37 Units/Rail
MC100H606FN	PLCC–28	37 Units/Rail

DC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0V ±5%)

Symbol	Characteristic	T_A = 0°C			T_A = + 25°C			T_A = + 85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{CCL}	Supply Current		18	30		18	30		18	30	mA	Outputs LOW
I_{CCH}	Supply Current		13	25		13	25		13	25	mA	Outputs HIGH
I_{GND}	Supply Current		75	90		75	90		75	95	mA	

TTL DC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0V ±5%)

Symbol	Characteristic	T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH}	Input HIGH Voltage	2.0		2.0		2.0		V	
V_{IL}	Input LOW Voltage		0.8		0.8		0.8	V	
V_{IK}	Input Clamp Voltage		–1.2		–1.2		–1.2	V	I_{IN} = –18mA
I_{IH}	Input HIGH Current		20 100		20 100		20 100	V	V_{IN} = 2.7V V_{IN} = 7.0V
I_{IL}	Input LOW Current		–0.6		–0.6		–0.6	mA	V_{IN} = 0.5V

10H PECL DC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0V ±5%)

Symbol	Characteristic	T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{INH}	Input HIGH Current		255		145		145	μA	
I_{INL}	Input LOW Current		0.5		0.5		0.5	μA	
V_{IH}	Input HIGH Voltage (Note 1.)	3830	4160	3870	4190	3930	4280	mV	V_{CCT} = 5.0V
V_{IL}	Input LOW Voltage (Note 1.)	3050	3520	3050	3520	3050	3555	mV	V_{CCT} = 5.0V
V_{OH}	Output HIGH Voltage (Note 1.)	3980	4160	4020	4190	4080	4270	mV	V_{CCT} = 5.0V
V_{OL}	Output LOW Voltage (Note 1.)	3050	3370	3050	3370	3050	3400	mV	V_{CCT} = 5.0V
V_{BB}	Reference Voltage (Note 1.)	3600	3710	3630	3730	3670	3790	mV	V_{CCT} = 5.0V

1. PECL V_{IL}, V_{IH}, V_{OL}, V_{OH} V_{BB} are given for V_{CCT} = V_{CCE} = 5.0V and will vary 1:1 with the power supply.

100H PECL DC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0V ±5%)

Symbol	Characteristic	T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{INH}	Input HIGH Current		255		145		145	μA	
I_{INL}	Input LOW Current		0.5		0.5		0.5	μA	
V_{IH}	Input HIGH Voltage (Note 2.)	3835	4120	3835	4120	3835	4120	mV	V_{CCT} = 5.0V
V_{IL}	Input LOW Voltage (Note 2.)	3190	3525	3190	3525	3190	3525	mV	V_{CCT} = 5.0V
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4120	3975	4120	3975	4120	mV	V_{CCT} = 5.0V
V_{OL}	Output LOW Voltage (Note 2.)	3190	3380	3190	3380	3190	3380	mV	V_{CCT} = 5.0V
V_{BB}	Output Bias Voltage (Note 2.)	3600	3720	3600	3720	3600	3720	mV	V_{CCT} = 5.0V

2. PECL V_{IL}, V_{IH}, V_{OL}, V_{OH} V_{BB} are given for V_{CCT} = V_{CCE} = 5.0V and will vary 1:1 with the power supply.

AC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0V ±5%)

Symbol	Characteristic	T_A = 0°C			T_A = + 25°C			T_A = + 85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PD}	Propagation Delay TCLK++	1.75		3.75	1.75	3.00	3.75	1.75		3.75	ns	50Ω to –2.0V
t_{PD}	Propagation Delay TCLK+–	1.75		3.75	1.75	3.00	3.75	1.75		3.75	ns	50Ω to –2.0V
t_{PD}	Propagation Delay CLK++	1.50		3.50	1.50	2.50	3.50	1.50		3.50	ns	50Ω to –2.0V
t_{PD}	Propagation Delay CLK+–	1.50		3.50	1.50	2.50	3.50	1.50		3.50	ns	50Ω to –2.0V
t_{PD}	Propagation Delay MR+–	1.50		3.50	1.50	2.50	3.50	1.75		3.75	ns	50Ω to –2.0V
t_{SKEW}	Device Skew Part–to–Part Within Device			 2.0 0.5		 1.0 0.3	 2.0 0.5			 2.0 0.5	ns	50Ω to –2.0V
t_S	Setup Time	1.5	0.5		1.5	0.5		1.5	0.5		ns	50Ω to –2.0V
t_H	Hold Time	1.5	0.5		1.5	0.5		1.5	0.5		ns	50Ω to –2.0V
t_{PW}	Minimum Pulse Width CLK	1.5			1.5	1.0		1.5			ns	50Ω to –2.0V
t_{PW}	Minimum Pulse Width MR	1.5			1.5			1.5			ns	50Ω to –2.0V
t_r	Rise Time			2.0		1.0	2.0			2.0	ns	50Ω to –2.0V
t_f	Fall Time			2.0		1.0	2.0			2.0	ns	50Ω to –2.0V
$t_{RES/REC}$	Reset/Recovery Time	2.5	2.0		2.5	2.0		2.5	2.0		ns	50Ω to –2.0V

MC10H607, MC100H607

Registered Hex PECL to TTL Translator

The MC10H/100H607 is a 6–bit, registered PECL to TTL translator. The device features differential PECL inputs for both data and clock. The TTL outputs feature 48mA sink, 24mA source drive capability for driving high fanout loads or transmission lines. The asynchronous master reset control is an ECL level input.

With its differential PECL inputs and TTL outputs the H607 device is ideally suited for the receive function of a HPPI bus type board–to–board interface application. The on chip registers simplify the task of synchronizing the data between the two boards.

The device is available in either ECL standard: the 10H device is compatible with MECL 10H™ logic levels, with a V_{CC} of +5.0 volts, while the 100H device is compatible with 100K logic levels, with a V_{CC} of +5.0 volts.

- Differential ECL Data and Clock Inputs
- 48mA Sink, 24mA Source TTL Outputs
- Single Power Supply
- Multiple Power and Ground Pins to Minimize Noise

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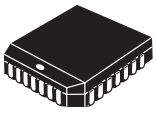
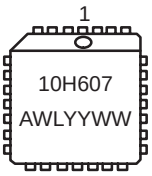


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAM

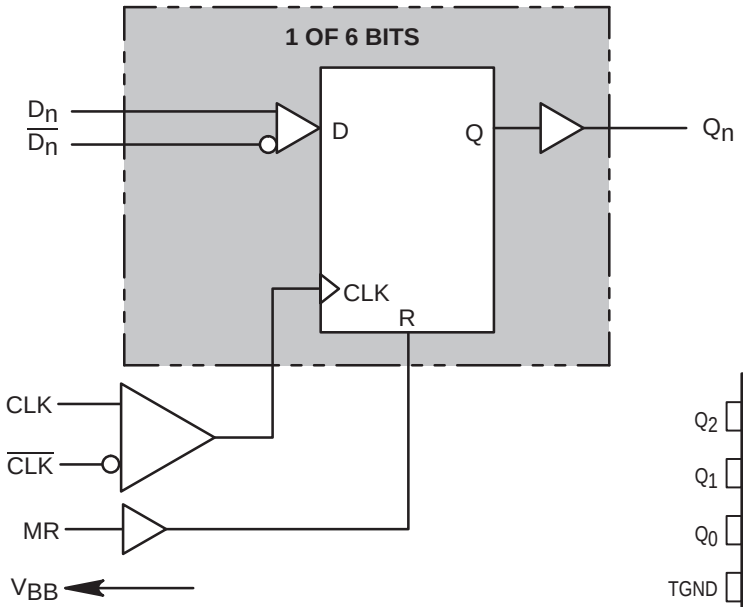


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

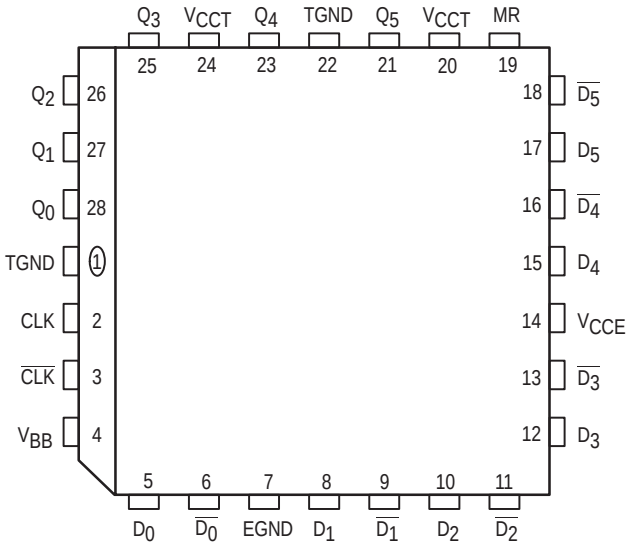
ORDERING INFORMATION

Device	Package	Shipping
MC10H607FN	PLCC–28	37 Units/Rail
MC100H607FN	PLCC–28	37 Units/Rail

LOGIC DIAGRAM



Pinout: 28–Lead PLCC (Top View)



PIN NAMES

Pin	Function
$D_0 - D_5$ $\overline{D_0} - \overline{D_5}$ CLK, $\overline{CLK}$ MR $Q_0 - Q_5$	True PECL Data Inputs Inverted PECL Data Inputs Differential PECL Clock Input PECL Master Reset Input TTL Outputs
V_{CCE} V_{CCT} TGND EGND	PECL V_{CC} TTL V_{CC} TTL Ground PECL Ground

TRUTH TABLE

D_n	MR	TCLK/CLK	$Q_n + 1$
L	L	Z	L
H	L	Z	H
X	H	X	L
Open Input	X	X	L

Z = LOW to HIGH Transition

DC CHARACTERISTICS ($V_{CCT} = V_{CCE} = 5.0V \pm 5\%$)

Symbol	Characteristic	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{EE}	ECL Power Supply Current 10H 100H		70 65	85 80		70 70	85 85		70 75	85 95	mA	
I_{CCL}	TTL Supply Current		100	120		100	120		100	120	mA	
I_{CCH}	TTL Supply Current		100	120		100	120		100	120	mA	

10H PECL DC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0V ±5%)

Symbol	Characteristic	T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{INH}	Input HIGH Current		255		145		145	μA	
I_{INL}	Input LOW Current		0.5		0.5		0.5	μA	
V_{IH}	Input HIGH Voltage	3830	4160	3870	4190	3930	4280	mV	V_{CCT} = 5.0V
V_{IL}	Input LOW Voltage	3050	3520	3050	3520	3050	3555	mV	V_{CCT} = 5.0V
V_{BB}	Output Bias Voltage	3600	3710	3630	3730	3670	3790	mV	V_{CCT} = 5.0V

NOTE: PECL V_{IL}, V_{IH}, V_{OL}, V_{OH}, V_{BB} are given for V_{CCT} = V_{CCE} = 5.0V and will vary 1:1 with power supply.

100H PECL DC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0V ±5%)

Symbol	Characteristic	T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input HIGH Current		255		145		145	μA	
I_{IL}	Input LOW Current		0.5		0.5		0.5	μA	
V_{IH}	Input HIGH Voltage	3835	4120	3835	4120	3835	4120	mV	V_{CCT} = 5.0V
V_{IL}	Input LOW Voltage	3190	3525	3190	3525	3190	3525	mV	V_{CCT} = 5.0V
V_{BB}	Output Bias Voltage	3600	3720	3600	3720	3600	3720	mV	V_{CCT} = 5.0V

NOTE: PECL V_{IL}, V_{IH}, V_{OL}, V_{OH}, V_{BB} are given for V_{CCT} = V_{CCE} = 5.0V and will vary 1:1 with power supply.

10H/100H TTL DC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0V ±5%)

Symbol	Characteristic	T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = –15mA I_{OH} = –24mA
V_{OL}	Output LOW Voltage		0.55		0.55		0.55	V	I_{OL} = 48mA

NOTE: DC levels such as V_{OH}, V_{OL}, etc., are standard for PECL and FAST devices, with the exceptions of: I_{OL} = 48mA at 0.5V_{OL}; and I_{OH} = –24mA at 2.0V_{OH}.

AC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0V ±5%)

Symbol	Characteristic	T_A = 0°C		T_A = + 25°C		T_A = + 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHH}	Propagation Delay to Output CLK to Q	5.5 4.6	7.7 7.7	6.0 4.9	8.2 8.3	6.7 5.9	10.0 10.0	ns	CL = 50pF
t_{PHL}	Propagation Delay to Output MR to Q	4.4	7.5	4.7	8.1	5.8	10.5	ns	CL = 50pF
t_{PW}	Minimum Pulse Width CLK, MR	1.0		1.0		1.0		ns	
t_r	Rise Time	0.5	2.0	0.5	2.0	0.5	2.0	ns	1.0V to 2.0V
t_f	Fall Time	0.5	2.0	0.5	2.0	0.5	2.0	ns	1.0V to 2.0V
t_S	Setup Time	1.5		1.5		1.5		ns	
t_H	Hold Time	1.5		1.5		1.5		ns	
V_{PP}	Minimum Input Swing	200		200		200		mV	

1. Numbers are for both ++ and – – delay MR to Q.

MC10H640, MC100H640

68030/040 PECL to TTL Clock Driver

The MC10H/100H640 generates the necessary clocks for the 68030, 68040 and similar microprocessors. It is guaranteed to meet the clock specifications required by the 68030 and 68040 in terms of part–to–part skew, within–part skew and also duty cycle skew.

The user has a choice of using either TTL or PECL (ECL referenced to +5.0V) for the input clock. TTL clocks are typically used in present MPU systems. However, as clock speeds increase to 50MHz and beyond, the inherent superiority of ECL (particularly differential ECL) as a means of clock signal distribution becomes increasingly evident. The H640 also uses differential PECL internally to achieve its superior skew characteristic.

The H640 includes divide–by–two and divide–by–four stages, both to achieve the necessary duty cycle skew and to generate MPU clocks as required. A typical 50MHz processor application would use an input clock running at 100MHz, thus obtaining output clocks at 50MHz and 25MHz (see Logic Diagram).

The 10H version is compatible with MECL 10H™ ECL logic levels, while the 100H version is compatible with 100K levels (referenced to +5.0V).

- Generates Clocks for 68030/040
- Meets 030/040 Skew Requirements
- TTL or PECL Input Clock
- Extra TTL and PECL Power/Ground Pins
- Asynchronous Reset
- Single +5.0V Supply

Function

Reset (R): LOW on RESET forces all Q outputs LOW and all $\overline{Q}$ outputs HIGH.

Power–Up: The device is designed to have the POS edges of the ÷2 and ÷4 outputs synchronized at power up.

Select (SEL): LOW selects the ECL input source (DE/$\overline{DE}$). HIGH selects the TTL input source (DT).

The H640 also contains circuitry to force a stable state of the ECL input differential pair, should both sides be left open. In this case, the DE side of the input is pulled LOW, and $\overline{DE}$ goes HIGH.

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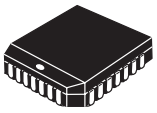
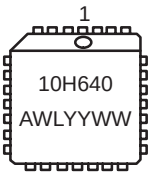


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAM

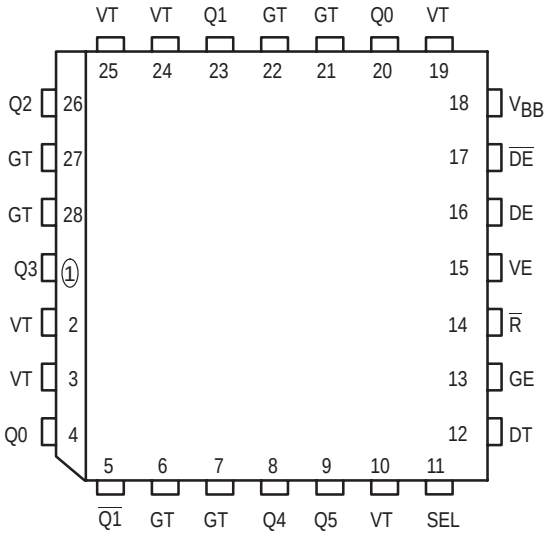


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

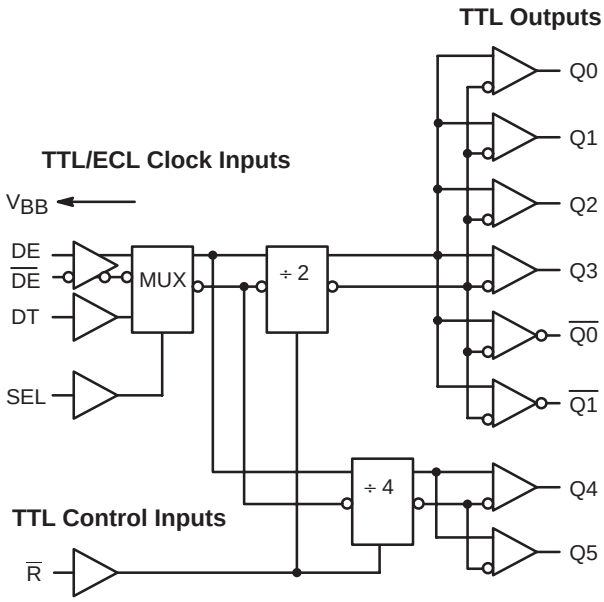
ORDERING INFORMATION

Device	Package	Shipping
MC10H640FN	PLCC–28	37 Units/Rail
MC100H640FN	PLCC–28	37 Units/Rail

Pinout: 28–Lead PLCC
(Top View)



LOGIC DIAGRAM



PIN NAMES

PIN	FUNCTION
GT	TTL Ground (0 V)
VT	TTL V_{CC} (+5.0 V)
VE	ECL V_{CC} (+5.0 V)
GE	ECL Ground (0 V)
DE, $\overline{DE}$	ECL Signal Input (positive ECL)
V_{BB}	V_{BB} Reference Output
DT	TTL Signal Input
Qn, $\overline{Qn}$	Signal Outputs (TTL)
SEL	Input Select (TTL)
$\overline{R}$	Reset (TTL)

AC CHARACTERISTICS (VT = VE = 5.0V ±5%)

Symbol	Characteristic		0°C		25°C		85°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay ECL D to Output	Q0–Q3	4.9	5.9	4.9	5.9	5.2	6.2	ns	CL = 25pF
t_{PLH}	Propagation Delay TTL D to Output		5.0	6.0	5.0	6.0	5.3	6.3	ns	CL = 25pF
tskwd*	Within–Device Skew			0.5		0.5		0.5	ns	CL = 25pF
t_{PLH}	Propagation Delay ECL D to Output	$\overline{Q0}$, $\overline{Q1}$	4.9	5.9	4.9	5.9	5.2	6.2	ns	CL = 25pF
t_{PLH}	Propagation Delay TTL D to Output		5.0	6.0	5.0	6.0	5.3	6.3	ns	CL = 25pF
t_{PLH}	Propagation Delay ECL D to Output	Q4, Q5	4.9	5.9	4.9	5.9	5.2	6.2	ns	CL = 25pF
t_{PLH}	Propagation Delay TTL D to Output		5.0	6.0	5.0	6.0	5.3	6.3	ns	CL = 25pF
t_{PD}	Propagation Delay R to Output	All Outputs	4.3	6.3	4.3	6.3	5.0	7.0	ns	CL = 25pF
t_R t_F	Output Rise/Fall Time 0.8 V – 2.0 V	All Outputs		2.5 2.5		2.5 2.5		2.5 2.5	ns	CL = 25pF
f_{max}	Maximum Input Frequency		135		135		135		MHz	CL = 25pF
t_{pw}	Minimum Pulse Width		1.50		1.50		1.50		ns	
t_{rr}	Reset Recovery Time		1.25		1.25		1.25		ns	

* Within–Device Skew defined as identical transitions on similar paths through a device.

V_{CC} and C_L RANGES TO MEET DUTY CYCLE REQUIREMENTS ($0°C \le T_A \le 85°C$ Output Duty Cycle Measured Relative to 1.5V)

Symbol	Characteristic		Min	Nom	Max	Unit	Condition
	Range of V_{CC} and CL to meet minimum pulse width (HIGH or LOW) = 11.5 ns at $f_{out} \le 40$ MHz	V_{CC} CL	4.75 10	5.0	5.25 50	V pF	Q0–Q3 $\overline{Q0}$–$\overline{Q1}$
	Range of V_{CC} and CL to meet minimum pulse width (HIGH or LOW) = 9.5 ns at $40 < f_{out} \le 50$ MHz	V_{CC} CL	4.875 15	5.0	5.125 27	V pF	Q0–Q3

DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic		0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
I_{EE}	Power Supply Current	ECL		57		57		57	mA	VE Pin
I_{CCH}		TTL		30		30		30	mA	Total all VT pins
I_{CCL}				30		30		30	mA	

TTL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0	 0.8	2.0	 0.8	2.0	 0.8	V	
I_{IH}	Input HIGH Current		20 100		20 100		20 100	µA	V_{IN} = 2.7V V_{IN} = 7.0V
I_{IL}	Input LOW Current		–0.6		–0.6		–0.6	mA	V_{IN} = 0.5V
V_{OH}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = –3.0mA I_{OH} = –15mA
V_{OL}	Output LOW Voltage		0.5		0.5		0.5	V	I_{OL} = 24mA
V_{IK}	Input Clamp Voltage		–1.2		–1.2		–1.2	V	I_{IN} = –18mA
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0V

10H PECL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	175	 0.5	175	µA	
V_{IH}* V_{IL}*	Input HIGH Voltage Input LOW Voltage	3.83 3.05	4.16 3.52	3.87 3.05	4.19 3.52	3.94 3.05	4.28 3.555	V	VE = 5.0V
V_{BB}*	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	

*NOTE: PECL levels are referenced to V_{CC} and will vary 1:1 with the power supply. The values shown are for V_{CC} = 5.0V.

100H PECL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	175	 0.5	175	µA	
V_{IH}* V_{IL}*	Input HIGH Voltage Input LOW Voltage	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	V	VE = 5.0V
V_{BB}*	Output Reference Voltage	3.62	3.74	3.62	3.74	3.62	3.74	V	

*NOTE: PECL levels are referenced to V_{CC} and will vary 1:1 with the power supply. The values shown are for V_{CC} = 5.0V.

10/100H640
DUTY CYCLE CONTROL

To maintain a duty cycle of ±5% at 50MHz, limit the load capacitance and/or power supply variation as shown in Figures 1 and 2. For a ±2.5% duty cycle limit, see Figures 3 and 4. Figures 5 and 6 show duty cycle variation with temperature. Figure 7 shows typical TPD versus load. Figure 8 shows reset recovery time. Figure 9 shows output states after power up.

Best duty cycle control is obtained with a single µP load and minimum line length.

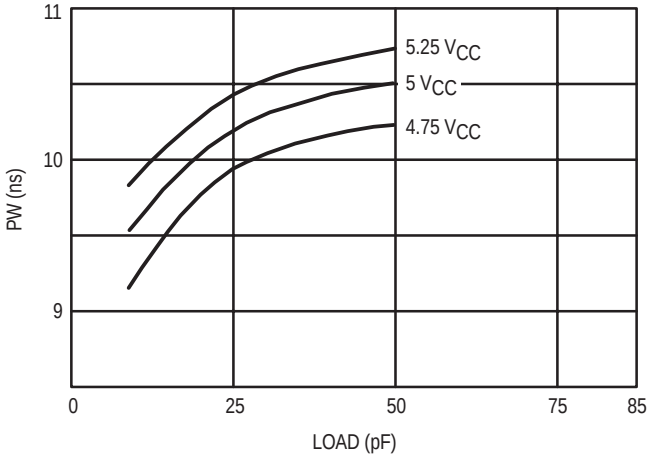


Figure 1. Positive Pulse Width at 25°C Ambient and 50 MHz Out

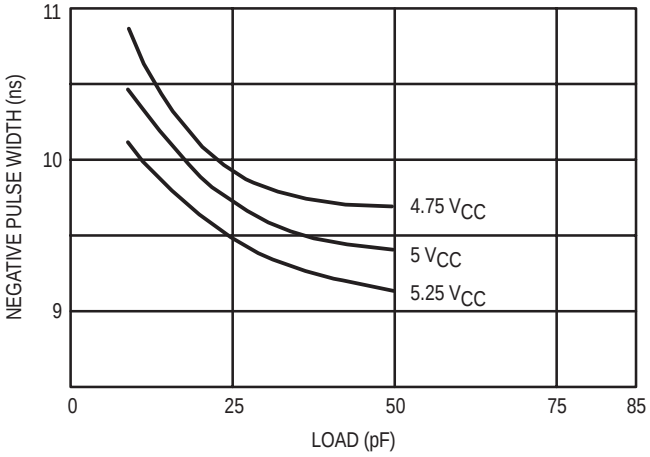


Figure 2. Negative Pulse Width @ 50 MHz Out and 25°C Ambient

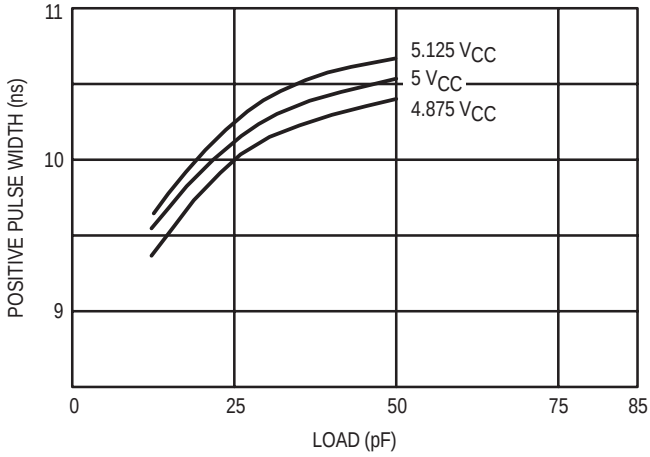


Figure 3. Positive Pulse Width at 25°C Ambient at 50 MHz Out

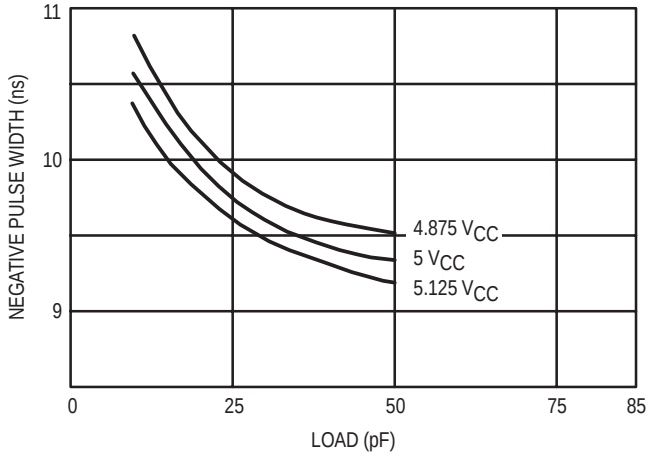


Figure 4. Negative Pulse Width @ 50 MHz Out and 25°C Ambient

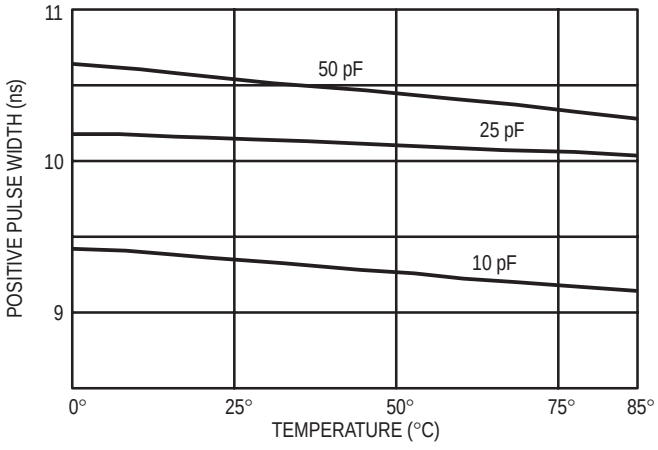


Figure 5. Temperature versus Positive Pulse Width for 100H640 at 50 MHz and +5.0 V V_{CC}

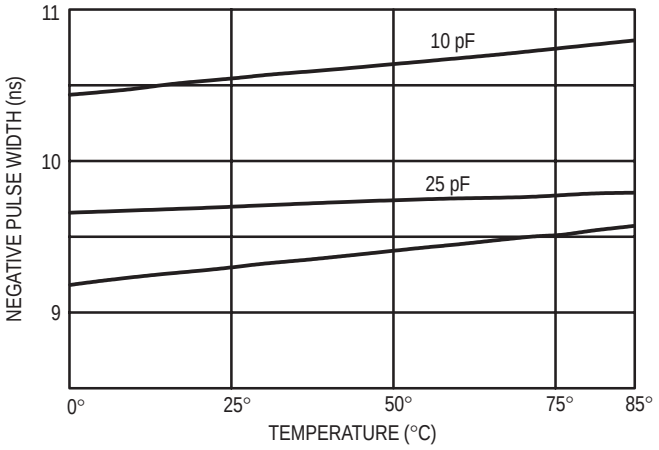


Figure 6. Temperature versus Negative Pulse Width for MC100H640 @ 50 MHz and +5.0 V V_{CC}

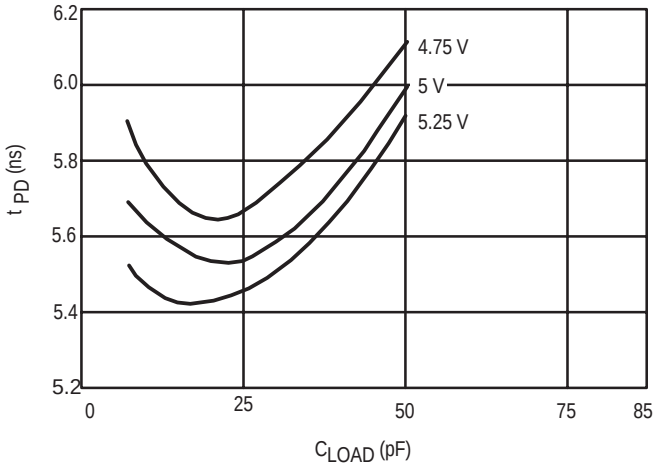


Figure 7. t_{PD} versus Load Typical at T_A = 25°C

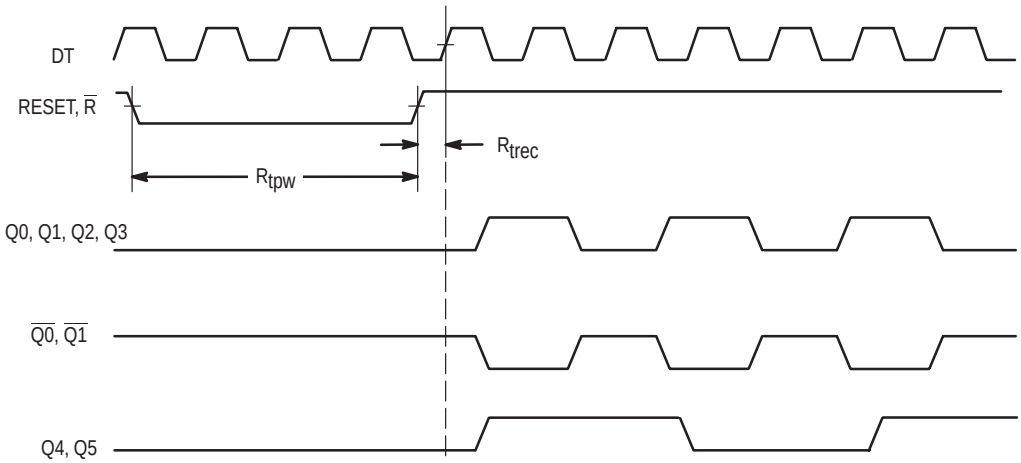
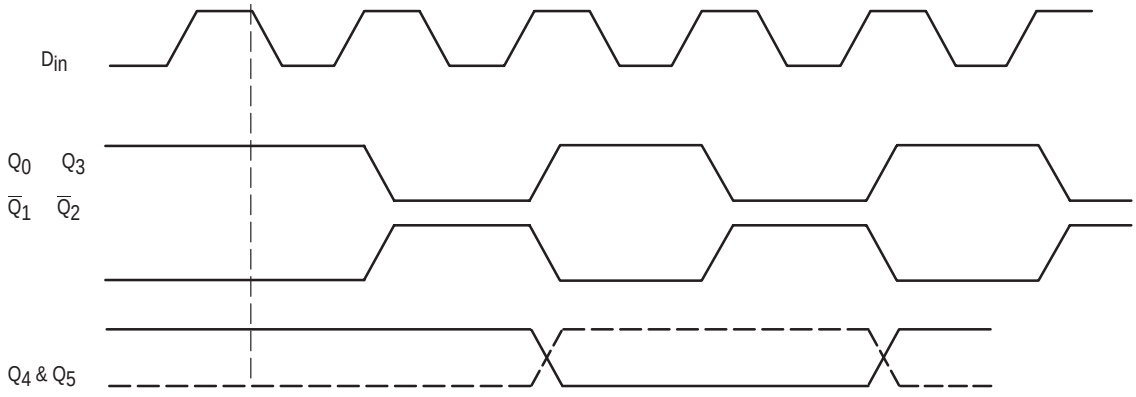


Figure 8. MC10H/100H640 Clock Phase and Reset Recovery Time After Reset Pulse



AFTER POWER UP
OUTPUTS Q_4 & Q_5 WILL SYN WITH POSITIVE EDGES OF D_{in} & Q_0 Q_3 & NEGATIVE EDGES OF $\overline{Q}_0$ & $\overline{Q}_1$

Figure 9. Output Timing Diagram

MC10H641, MC10H641

Single Supply PECL to TTL 1:9 Clock Distribution Chip

The MC10H/100H641 is a single supply, low skew translating 1:9 clock driver. Devices in the Motorola H600 translator series utilize the 28–lead PLCC for optimal power pinning, signal flow through and electrical performance.

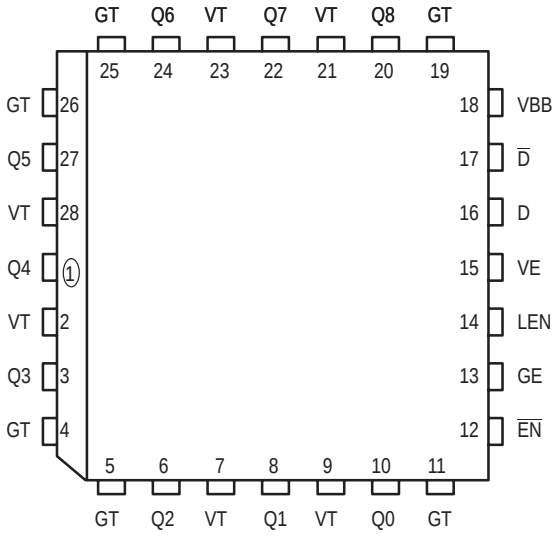
The device features a 24mA TTL output stage, with AC performance specified into a 50pF load capacitance. A latch is provided on–chip. When LEN is LOW (or left open, in which case it is pulled LOW by the internal pulldown) the latch is transparent. A HIGH on the enable pin ($\overline{EN}$) forces all outputs LOW. Both the LEN and $\overline{EN}$ pins are positive ECL inputs.

The V_{BB} output is provided in case the user wants to drive the device with a single–ended input. For single–ended use the V_{BB} should be connected to the $\overline{D}$ input and bypassed with a 0.01μF capacitor.

The 10H version of the H641 is compatible with positive MECL 10H™ logic levels. The 100H version is compatible with positive 100K levels.

- PECL–TTL Version of Popular ECLinPS E111
- Low Skew
- Guaranteed Skew Spec
- Latched Input
- Differential ECL Internal Design
- V_{BB} Output for Single–Ended Use
- Single +5V Supply
- Logic Enable
- Extra Power and Ground Supplies
- Separate ECL and TTL Supply Pins

Pinout: 28–Lead PLCC (Top View)



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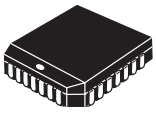
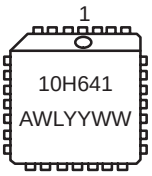


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

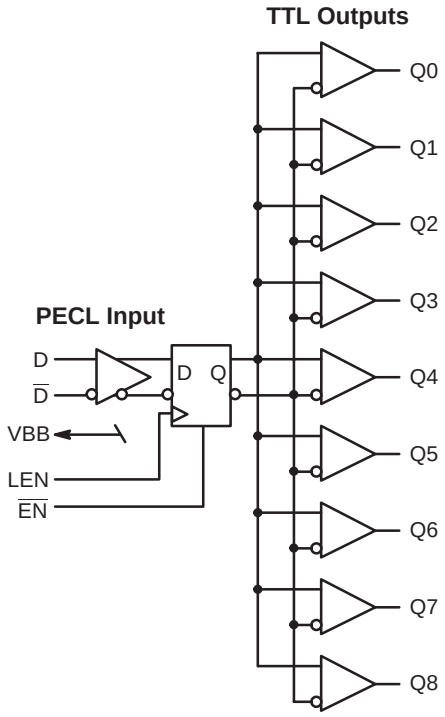
PIN NAMES

Pins	Function
GT, VT	TTL GND, TTL V_{CC}
GE, VE	ECL GND, ECL V_{CC}
D, $\overline{D}$	Signal Input (Positive ECL)
V_{BB}	V_{BB} Reference Output (Positive ECL)
Q0–Q8	Signal Outputs (TTL)
$\overline{EN}$	Enable Input (Positive ECL)
LEN	Latch Enable Input (Positive ECL)

ORDERING INFORMATION

Device	Package	Shipping
MC10H641FN	PLCC–28	37 Units/Rail
MC100H641FN	PLCC–28	37 Units/Rail

LOGIC DIAGRAM



DC CHARACTERISTICS (VT = VE = 5.0V ±5%)

Symbol	Characteristic	T_A = 0°C			T_A = + 25°C			T_A = + 85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{EE}	Power Supply Current PECL		24	30		24	30		24	30	mA	
I_{CCH}	TTL		24	30		24	30		24	30	mA	
I_{CCL}			27	35		27	35		27	35	mA	

TTL DC CHARACTERISTICS (VT = VE = 5.0V ±5%)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage	2.5		2.5		2.5		V	I_{OH} = –15mA
V_{OL}	Output LOW Voltage		0.5		0.5		0.5	V	I_{OL} = 24mA
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0V

10H PECL DC CHARACTERISTICS

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input HIGH Current		225		175		175	µA	
I_{IL}	Input LOW Current	0.5		0.5		0.5		µA	
V_{IH}	Input HIGH Voltage	3.83	4.16	3.87	4.19	3.94	4.28	V	VE = 5.0V[1]
V_{IL}	Input LOW Voltage	3.05	3.52	3.05	3.52	3.05	3.55	V	VE = 5.0V[1]
V_{BB}	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	VE = 5.0V[1]

1. PECL V_{IH}, V_{IL}, and V_{BB} are referenced to VE and will vary 1:1 with the power supply. The levels shown are for VE = 5.0V.

100H PECL DC CHARACTERISTICS

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{INH}	Input HIGH Curren		225		175		175	μA	
I_{INL}	Input LOW Current	0.5		0.5		0.5		μA	
V_{IH}	Input HIGH Voltage	3.835	4.120	3.835	4.120	3.835	4.120	V	VE = 5.0V[1]
V_{IL}	Input LOW Voltage	3.190	3.525	3.190	3.525	3.190	3.525	V	VE = 5.0V[1]
V_{BB}	Output Reference Voltage	3.62	3.74	3.62	3.74	3.62	3.74	V	VE = 5.0V[1]

1. PECL V_{IH}, V_{IL}, and V_{BB} are referenced to VE and will vary 1:1 with the power supply. The levels shown are for VE = 5.0V.

AC CHARACTERISTICS (VT = VE = 5.0V ±5%)

Symbol	Characteristic	T_J = 0°C			T_J = + 25°C			T_J = + 85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay D to Q	5.00 5.36	5.50 5.86	6.00 6.36	4.86 5.27	5.36 5.77	5.86 6.27	5.08 5.43	5.58 5.93	6.08 6.43	ns	CL = 50 pF[1]
t_{skew}	Device Skew Part–to–Part Single V_{CC} Output–to–Output			 1000 750 350			 1000 750 350			 1000 750 350	ps	 CL = 50pF[2] CL = 50 pF[3] CL = 50 pF[4]
t_{PLH} t_{PHL}	Propagation Delay LEN to Q	4.9		6.9	4.9		6.9	5.0		7.0	ns	CL = 50 pF
t_{PLH} t_{PHL}	Propagation Delay $\overline{EN}$ to Q	5.0		7.0	4.9		6.9	5.0		7.0	ns	CL = 50 pF
t_r t_f	Output Rise/Fall 0.8V to 2.0V			1.7 1.6			1.7 1.6			1.7 1.6	ns	CL = 50 pF
f_{MAX}	Max Input Frequency	65			65			65			MHz	CL = 50 pF[5]
t_S	Setup Time	0.75	0.50		0.75	0.50		0.75	0.50		ns	
t_H	Hold Time	0.75	0.50		0.75	0.50		0.75	0.50		ns	

1. Propagation delay measurement guaranteed for junction temperatures. Measurements performed at 50MHz input frequency.
2. Skew window guaranteed for a single temperature across a $V_{CC} = V_T = V_E$ of 4.75V to 5.25V (See Application Note in this datasheet).
3. Skew window guaranteed for a single temperature and single $V_{CC} = V_T = V_E$
4. Output–to–output skew is specified for identical transitions through the device.
5. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.

Determining Skew for a Specific Application

The H641 has been designed to meet the needs of very low skew clock distribution applications. In order to optimize the device for this application special considerations are necessary in the determining of the part–to–part skew specification limits. Older standard logic devices are specified with relatively slack limits so that the device can be guaranteed over a wide range of potential environmental conditions. This range of conditions represented all of the potential applications in which the device could be used. The result was a specification limit that in the vast majority of cases was extremely conservative and thus did not allow for an optimum system design. For non–critical skew designs this practice is acceptable, however as the clock speeds of systems increase overly conservative specification limits can kill a design.

The following will discuss how users can use the information provided in this data sheet to tailor a part–to–part skew specification limit to their application. The skew determination process may appear somewhat tedious and time consuming, however if the utmost in performance is required this procedure is necessary. For applications which do not require this level of skew performance a generic part–to–part skew limit of 2.5ns can be used. This limit is good for the entire ambient temperature range, the guaranteed V_{CC} (V_T, V_E) range and the guaranteed operating frequency range.

Temperature Dependence

A unique characteristic of the H641 data sheet is that the AC parameters are specified for a junction temperature rather than the usual ambient temperature. Because very few designs will actually utilize the entire commercial temperature range of a device a tighter propagation delay window can be established given the smaller temperature range. Because the junction temperature and not the ambient temperature is what affects the performance of the device the parameter limits are specified for junction temperature. In addition the relationship between the ambient and junction temperature will vary depending on the frequency, load and board environment of the application. Since these factors are all under the control of the user it is impossible to provide specification limits for every possible application. Therefore a baseline specification was established for specific junction temperatures and the information that follows will allow these to be tailored to specific applications.

Since the junction temperature of a device is difficult to measure directly, the first requirement is to be able to "translate" from ambient to junction temperatures. The standard method of doing this is to use the power dissipation of the device and the thermal resistance of the package. For a TTL output device the power dissipation will be a function of the load capacitance and the frequency of the output. The total power dissipation of a device can be described by the following equation:

$$P_D \text{ (watts)} = I_{CC} \text{ (no load)} * V_{CC} + V_S * V_{CC} * f * C_L * \# \text{ Outputs}$$

where:

V_S = Output Voltage Swing = 3V
f = Output Frequency
C_L = Load Capacitance
$I_{CC} = I_{EE} + I_{CCH}$

Figure 1 plots the I_{CC} versus Frequency of the H641 with no load capacitance on the output. Using this graph and the information specific to the application a user can determine the power dissipation of the H641.

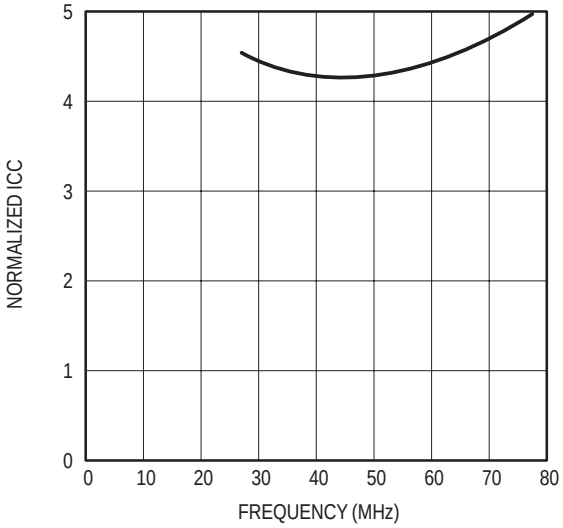


Figure 1. I_{CC} versus f (No Load)

Figure 2 illustrates the thermal resistance (in °C/W) for the 28–lead PLCC under various air flow conditions. By reading the thermal resistance from the graph and multiplying by the power dissipation calculated above the junction temperature increase above ambient of the device can be calculated.

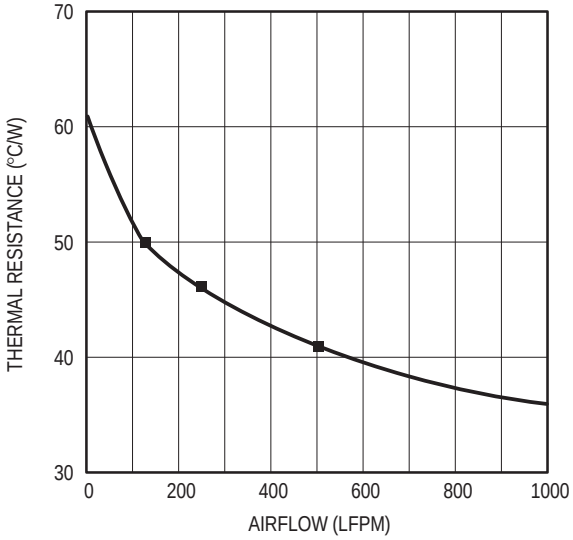


Figure 2. $\varnothing_{JA}$ versus Air Flow

Finally taking this value for junction temperature and applying it to Figure 3 allows the user to determine the propagation delay for the device in question. A more common use would be to establish an ambient temperature range for the H641's in the system and utilize the above methodology to determine the potential increased skew of the distribution network. Note that for this information if the T_{PD} versus Temperature curve were linear the calculations would not be required. If the curve were linear over all temperatures a simple temperature coefficient could be provided.

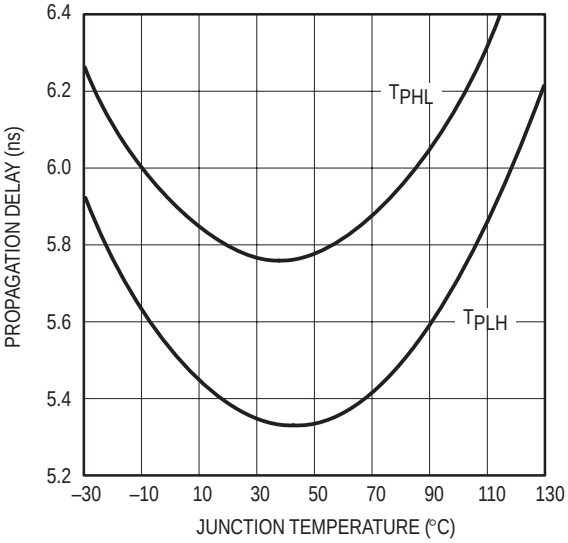


Figure 3. T_{PD} versus Junction Temperature

V_{CC} Dependence

TTL and CMOS devices show a significant propagation delay dependence with V_{CC}. Therefore the V_{CC} variation in a system will have a direct impact on the total skew of the clock distribution network. When calculating the skew between two devices on a single board it is very likely an assumption of identical V_{CC}'s can be made. In this case the number provided in the data sheet for part–to–part skew would be overly conservative. By using Figure 4 the skew given in the data sheet can be reduced to represent a smaller or zero variation in V_{CC}. The delay variation due to the specified V_{CC} variation is ≈270ps. Therefore, the 1ns window on the data sheet can be reduced by 270ps if the devices in question will always experience the same V_{CC}. The distribution of the propagation delay ranges given in the data sheet is actually a composite of three distributions whose means are separated by the fixed difference in propagation delay at the typical, minimum and maximum V_{CC}.

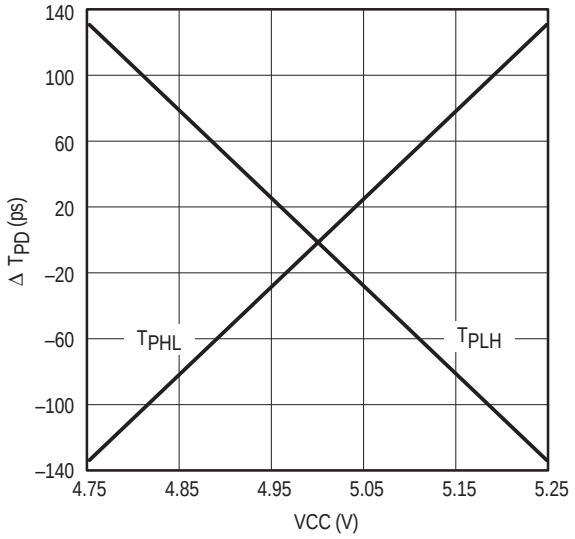


Figure 4. ΔT_{PD} versus V_{CC}

Capacitive Load Dependence

As with V_{CC} the propagation delay of a TTL output is intimately tied to variation in the load capacitance. The skew specifications given in the data sheet, of course, assume equal loading on all of the outputs. However situations could arise where this is an impossibility and it may be necessary to estimate the skew added by asymmetric loading. In addition the propagation delay numbers are provided only for 50pF loads, thus necessitating a method of determining the propagation delay for alternative loads.

Figure 5 shows the relationship between the two propagation delays with respect to the capacitive load on the output. Utilizing this graph and the 50pF limits the specification of the H641 can be mapped into a spec for either a different value load or asymmetric loads.

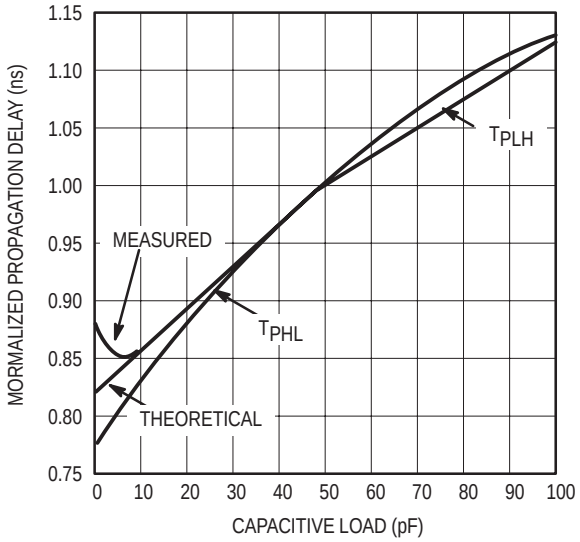


Figure 5. T_{PD} versus Load

Rise/Fall Skew Determination

The rise–to–fall skew is defined as simply the difference between the T_{PLH} and the T_{PHL} propagation delays. This skew for the H641 is dependent on the V_{CC} applied to the device. Notice from Figure 4 the opposite relationship of T_{PD} versus V_{CC} between T_{PLH} and T_{PHL}. Because of this the rise–to–fall skew will vary depending on V_{CC}. Since in all likelihood it will be impossible to establish the exact value for V_{CC}, the expected variation range for V_{CC} should be used. If this variation will be the ±5% shown in the data sheet the rise–to–fall skew could be established by simply subtracting the fastest T_{PLH} from the slowest T_{PHL}; this exercise yields 1.41ns. If a tighter V_{CC} range can be realized Figure 4 can be used to establish the rise–to–fall skew.

Specification Limit Determination Example

The situation pictured in Figure 6 will be analyzed as an example. The central clock is distributed to two different cards; on one card a single H641 is used to distribute the clock while on the second card two H641's are required to supply the needed clocks. The data sheet as well as the graphical information of this section will be used to calculate the skew between H641a and H641b as well as the skew between all three of the devices. Only the T_{PLH} will be analyzed, the T_{PHL} numbers can be found using the same technique. The following assumptions will be used:

- All outputs will be loaded with 50pF
- All outputs will toggle at 30MHz
- The V_{CC} variation between the two boards is ±3%
- The temperature variation between the three devices is ±15°C around an ambient of 45°C.
- 500LFPM air flow

The first task is to calculate the junction temperature for the devices under these conditions. Using the power equation yields:

$P_D = I_{CC}$ (no load) * V_{CC} +
$V_{CC} * V_S * f * C_L$ * # outputs
= 4.3 * 48mA * 5V + 5V * 3V * 30MHz *
50pF * 9
= 432mW + 203mW = 635mW

Using the thermal resistance graph of Figure 2 yields a thermal resistance of 41°C/W which yields a junction temperature of 71°C with a range of 56°C to 86°C. Using the T_{PD} versus Temperature curve of Figure 3 yields a propagation delay of 5.42ns and a variation of 0.19ns.

Since the design will not experience the full ±5% V_{CC} variation of the data sheet the 1ns window provided will be unnecessarily conservative. Using the curve of Figure 4 shows a delay variation due to a ±3% V_{CC} variation of ±0.075ns. Therefore the 1ns window can be reduced to 1ns – (0.27ns – 0.15ns) = 0.88ns. Since H641a and H641b are on the same board we will assume that they will always be at the same V_{CC}; therefore the propagation delay window will only be 1ns – 0.27ns = 0.73ns.

Putting all of this information together leads to a skew between all devices of

0.19ns + 0.88ns
(temperature + supply, and inherent device),

while the skew between devices A and B will be only

0.19ns + 0.73ns
(temperature + inherent device only).

In both cases, the propagation delays will be centered around 5.42ns, resulting in the following t_{PLH} windows:

T_{PLH} = 4.92ns – 5.99ns; 1.07ns window
(all devices)
T_{PLH} = 5.00ns – 5.92ns; 0.92ns window
(devices a & b)

Of course the output–to–output skew will be as shown in the data sheet since all outputs are equally loaded.

This process may seem cumbersome, however the delay windows, and thus skew, obtained are significantly better than the conservative worst case limits provided at the beginning of this note. For very high performance designs, this extra information and effort can mean the difference between going ahead with prototypes or spending valuable engineering time searching for alternative approaches.

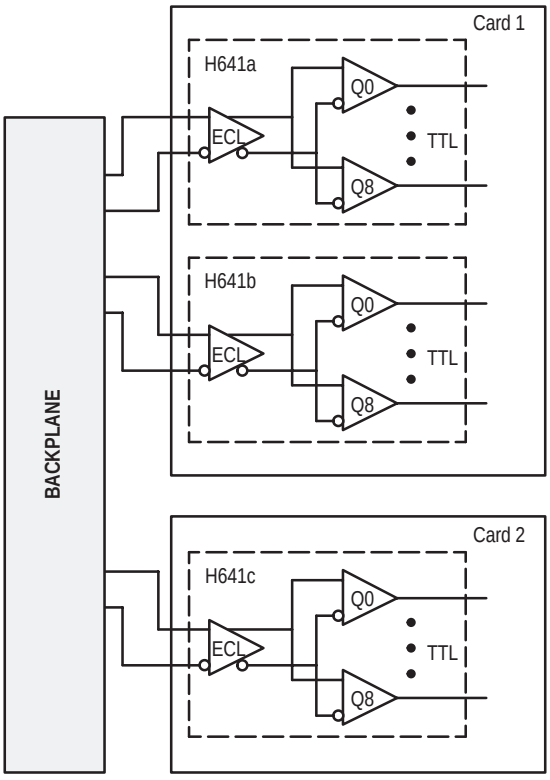


Figure 6. Example Application

MC10H642, MC100H642

68030/040 PECL to TTL Clock Driver

The MC10H/100H642 generates the necessary clocks for the 68030, 68040 and similar microprocessors. It is guaranteed to meet the clock specifications required by the 68030 and 68040 in terms of part–to–part skew, within–part skew and also duty cycle skew.

The user has a choice of using either TTL or PECL (ECL referenced to +5.0V) for the input clock. TTL clocks are typically used in present MPU systems. However, as clock speeds increase to 50MHz and beyond, the inherent superiority of ECL (particularly differential ECL) as a means of clock signal distribution becomes increasingly evident. The H642 also uses differential PECL internally to achieve its superior skew characteristic.

The H642 includes divide–by–two and divide–by–four stages, both to achieve the necessary duty cycle skew and to generate MPU clocks as required. A typical 50MHz processor application would use an input clock running at 100MHz, thus obtaining output clocks at 50MHz and 25MHz (see Logic Diagram).

The 10H version is compatible with MECL 10H™ ECL logic levels, while the 100H version is compatible with 100K levels (referenced to +5.0V).

- Generates Clocks for 68030/040
- Meets 030/040 Skew Requirements
- TTL or PECL Input Clock
- Extra TTL and PECL Power/Ground Pins
- Asynchronous Reset
- Single +5.0V Supply

Function

Reset(R): LOW on RESET forces all Q outputs LOW.

Select(SEL): LOW selects the ECL input source (DE/$\overline{DE}$). HIGH selects the TTL input source (DT).

The H642 also contains circuitry to force a stable input state of the ECL differential input pair, should both sides be left open. In this Case, the DE side of the input is pulled LOW, and $\overline{DE}$ goes HIGH.

Power Up: The device is designed to have positive edges of the ÷2 and ÷4 outputs synchronized at Power Up.

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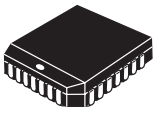
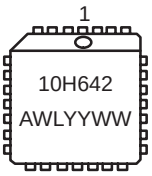


PLCC–28
FN SUFFIX
CASE 776

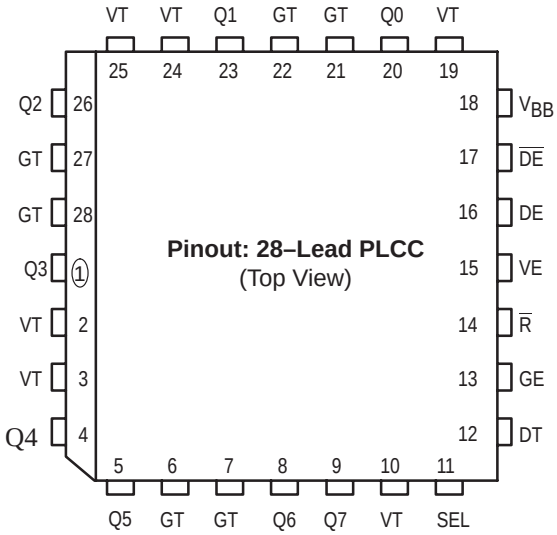
MARKING DIAGRAM



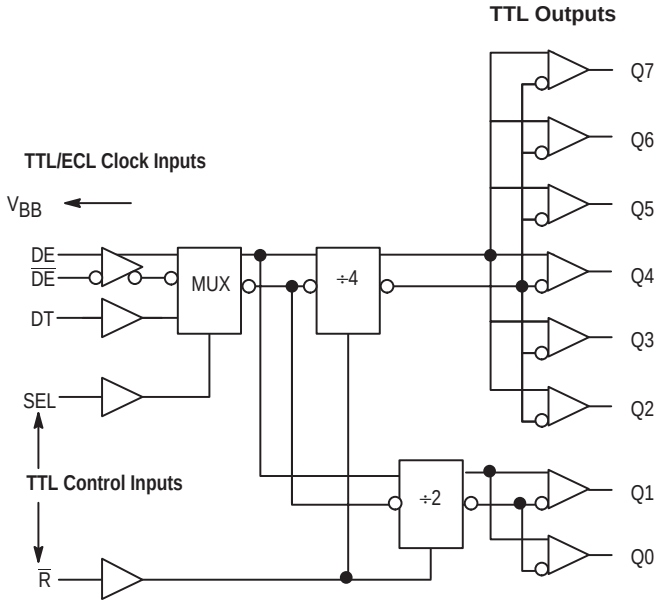
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H642FN	PLCC–28	37 Units/Rail
MC100H642FN	PLCC–28	37 Units/Rail



LOGIC DIAGRAM



PIN NAMES

Pin	Symbol	Description	Pin	Symbol	Description
1	Q3	Signal Output (TTL)**	15	VE	ECL V_{CC} (+5.0V)
2	VT	TTL V_{CC} (+5.0V)	16	DE	ECL Signal Input (Non–Inverting)
3	VT	TTL V_{CC} (+5.0V)	17	$\overline{DE}$	ECL Signal Input (Inverting)
4	Q4	Signal Output (TTL)**	18	V_{BB}	V_{BB} Reference Output
5	Q5	Signal Output (TTL)**	19	VT	TTL V_{CC} (+5.0V)
6	GT	TTL Ground (0V)	20	Q0	Signal Output (TTL)*
7	GT	TTL Ground (0V)	21	GT	TTL Ground (0V)
8	Q6	Signal Output (TTL)**	22	GT	TTL Ground (0V)
9	Q7	Signal Output (TTL)**	23	Q1	Signal Output (TTL)*
10	VT	TTL V_{CC} (+5.0V)	24	VT	TTL V_{CC} (+5.0V)
11	SEL	Input Select (TTL)	25	VT	TTL V_{CC} (+5.0V)
12	DT	TTL Signal Input	26	Q2	Signal Output (TTL)**
13	GE	ECL Ground (0V)	27	GT	TTL Ground (0V)
14	R	Reset (TTL)	28	GT	TTL Ground (0V)

*Divide by 2
**Divide by 4

AC CHARACTERISTICS (VT = VE = 5.0V ±5%)

Symbol	Characteristic		T_A = 0°C Min	T_A = 0°C Max	T_A = 25°C Min	T_A = 25°C Max	T_A = 85°C Min	T_A = 85°C Max	Unit	Condition
t_{PLH}	Propagation Delay D to Output	Q2–Q7 C ECL C TTL	 4.70 4.70	 5.70 5.70	 4.75 4.75	 5.75 5.75	 4.60 4.50	 5.60 5.50	ns	CL = 25pF
tskpp	Part–to–Part Skew			1.0		1.0		1.0	ns	
tskwd*	Within–Device Skew			0.5		0.5		0.5	ns	
t_{PLH}	Propagation Delay D to Output	Q0, Q1 C ECL C TTL	 4.30 4.30	 5.30 5.30	 4.50 4.50	 5.50 5.50	 4.25 4.25	 5.25 5.25	ns	CL = 25pF
tskpp	Part–to–Part Skew	All Outputs		2.0		2.0		2.0	ns	CL = 25pF
tskwd	Within–Device Skew			1.0		1.0		1.0	ns	CL = 25pF
t_{PD}	Propagation Delay R to Output	All Outputs	4.3	6.3	4.0	6.0	4.5	6.5	ns	CL = 25pF
t_R t_F	Output Rise/Fall Time 0.8 V to 2.0 V	All Outputs		2.5 2.5		2.5 2.5		2.5 2.5	ns	CL = 25pF
f_{MAX}**	Maximum Input Frequency		100		100		100		MHz	CL = 25pF
RPW	Reset Pulse Width		1.5		1.5		1.5		ns	
RRT	Reset Recovery Time		1.25		1.25		1.25		ns	

* Within–Device Skew defined as identical transactions on similar paths through a device.

** NOTE: MAX Frequency is 135MHz.

10H PECL CHARACTERISTICS (VT = VE = 5.0V ±5%)

Symbol	Characteristic	T_A = 0°C Min	T_A = 0°C Max	T_A = 25°C Min	T_A = 25°C Max	T_A = 85°C Min	T_A = 85°C Max	Unit	Condition
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	175	 0.5	175	μA	
	* NOTE								
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	3.83 3.05	4.16 3.52	3.87 3.05	4.19 3.52	3.94 3.05	4.28 3.555	V	V_{EE} = 5.0V
	* NOTE								
V_{BB}	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	

100H PECL CHARACTERISTICS (VT = VE = 5.0V ±5%)

Symbol	Characteristic	T_A = 0°C Min	T_A = 0°C Max	T_A = 25°C Min	T_A = 25°C Max	T_A = 85°C Min	T_A = 85°C Max	Unit	Condition
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	175	 0.5	175	μA	
	* NOTE								
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	3.835 3.190	4.120 3.525	3.835 3.190	4.120 3.525	3.835 3.190	4.120 3.525	V	V_{EE} = 5.0V
	* NOTE								
V_{BB}	Output Reference Voltage	3.620	3.740	3.620	3.740	3.620	3.740	V	

*NOTE: PECL LEVELS are referenced to V_{CC} and will vary 1:1 with the power supply. The VALUES shown are for V_{CC} = 5.0V.

10H/100H DC CHARACTERISTICS (VT = VE = 5.0V ±5%)

Symbol	Characteristic		T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
I_{EE}	Power Supply Current	PECL		57		57		57	mA	VE Pin
I_{CCH}		TTL		30		30		30	mA	Total All VT Pins
I_{CCL}				30		30		30	mA	

10H/100H TTL DC CHARACTERISTICS (VT = VE = 5.0V ±5%)

Symbol	Characteristic	T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0	 0.8	2.0	 0.8	2.0	 0.8	V	
I_{IH}	Input HIGH Current		20 100		20 100		20 100	μA	V_{IN} = 2.7V V_{IN} = 7.0V
I_{IL}	Input LOW Current		–0.6		–0.6		–0.6	mA	V_{IN} = 0.5V
V_{OH}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = –3.0mA I_{OH} = –15mA
V_{OL}	Output LOW Voltage		0.5		0.5		0.5	V	I_{OL} = 24mA
V_{IK}	Input Clamp Voltage		–1.2		–1.2		–1.2	V	I_{IN} = –18mA
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0V

10/100H642
DUTY CYCLE CONTROL

To maintain a duty cycle of ±5% at 50 MHz, limit the load capacitance and/or power supply variation as shown in Figures 1 and 2. For a ±2.5% duty cycle limit, see Figures 3 and 4. Figures 5 and 6 show duty cycle variation with temperature. Figure 7 shows typical TPD versus load. Figure 8 shows reset recovery time. Figure 9 shows output states after power up.

Best duty cycle control is obtained with a single μP load and minimum line length.

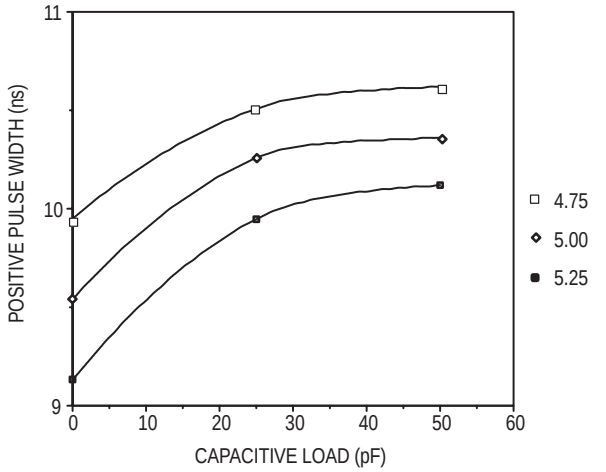


Figure 1. MC10H642 Positive PW versus Load @ ±5% V_{CC}, T_A = 25°C

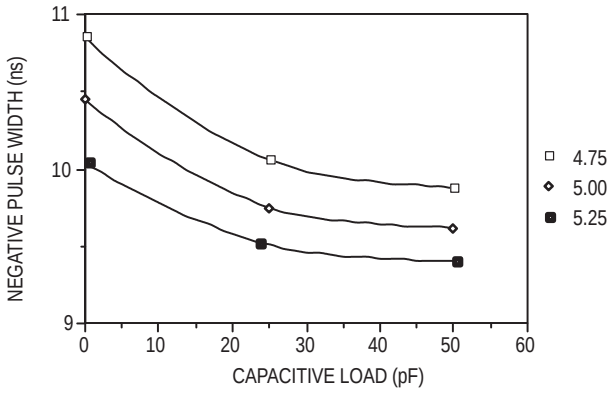


Figure 2. MC10H642 Negative PW versus Load @ ±5% V_{CC}, T_A = 25°C

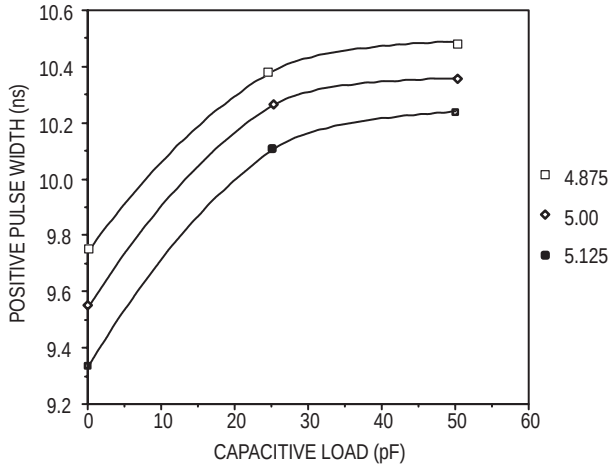


Figure 3. MC10H642 Positive PW versus Load @ ±2.5% V_{CC}, T_A = 25°C

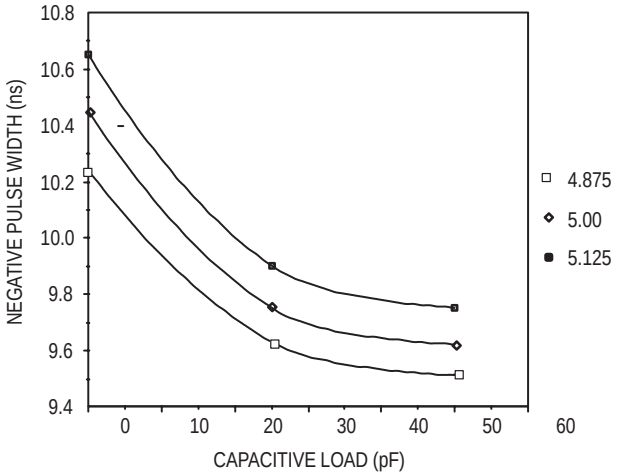


Figure 4. MC10H642 Negative PW versus Load @ ±2.5% V_{CC}, T_A = 25°C

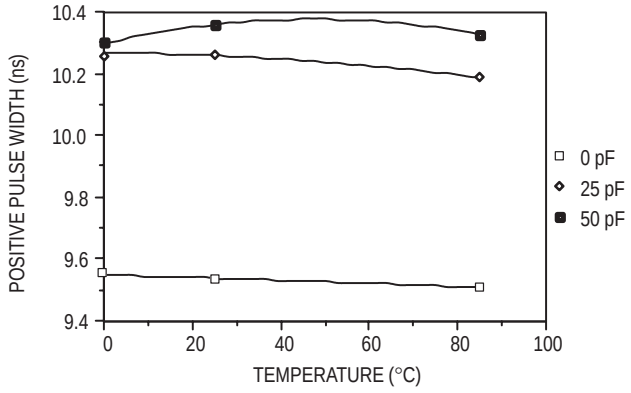


Figure 5. MC10H642 Positive PW versus Temperature, V_{CC} = 5.0V

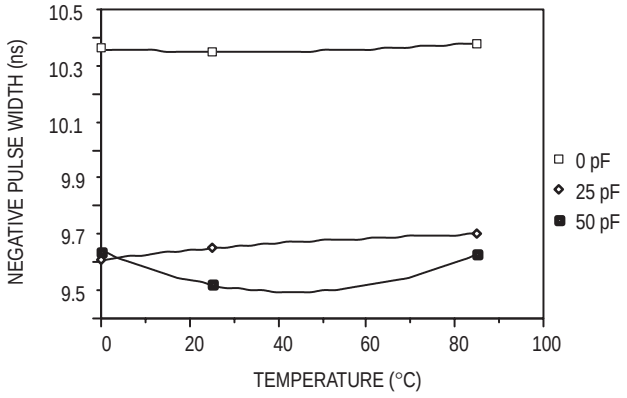


Figure 6. MC10H642 Negative PW versus Temperature, V_{CC} = 5.0V

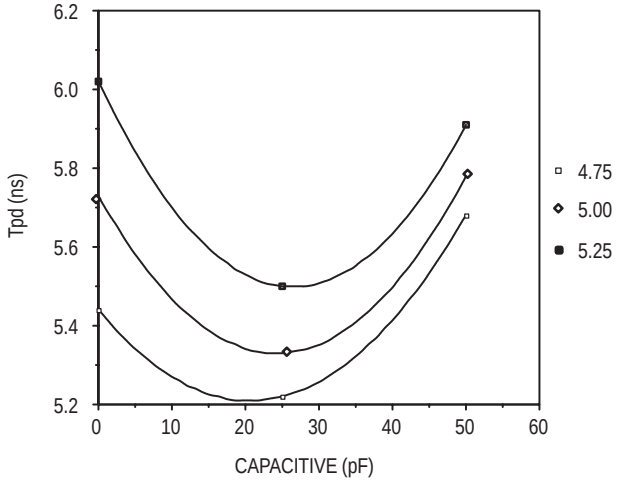


Figure 7. MC10H642 + Tpd versus Load, V_{CC} ±5%, T_A = 25°C (Overshoot at 50 MHz with no load makes graph non linear)

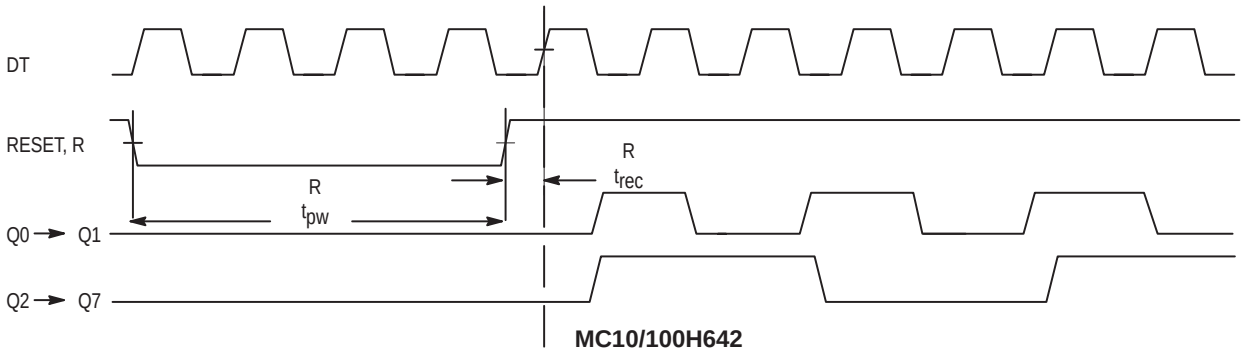


Figure 8. Clock Phase and Reset Recovery Time After Reset Pulse

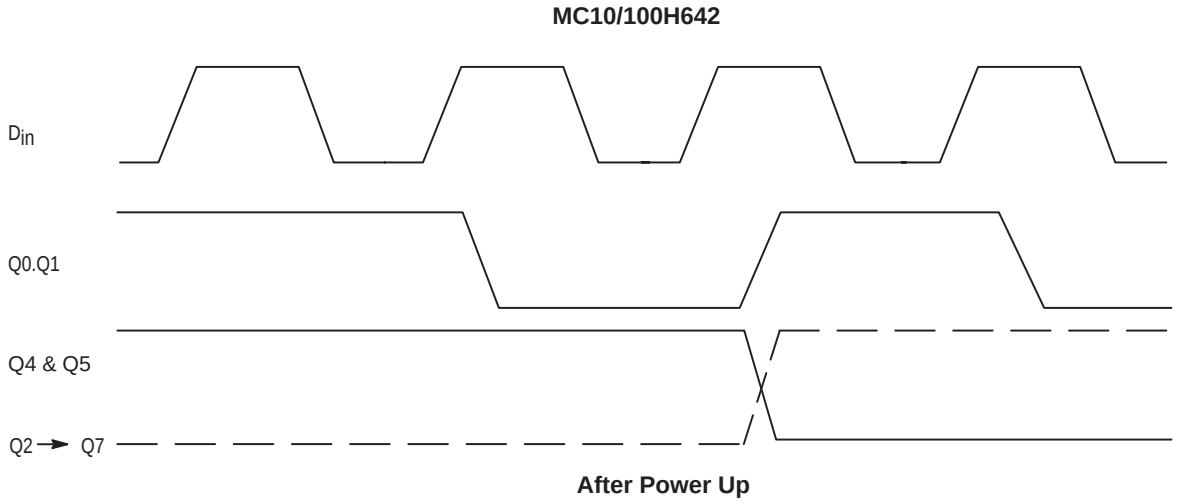
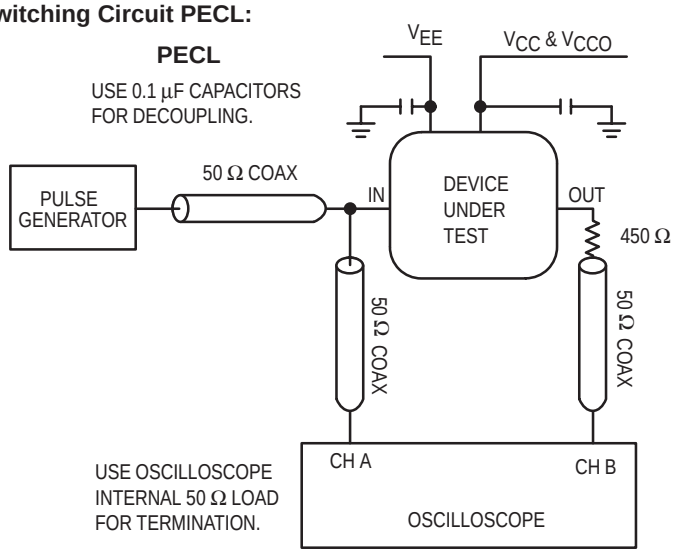


Figure 9. Outputs Q2 → Q7 will Synchronize with Pos Edges of D_{in} & Q0 → Q1

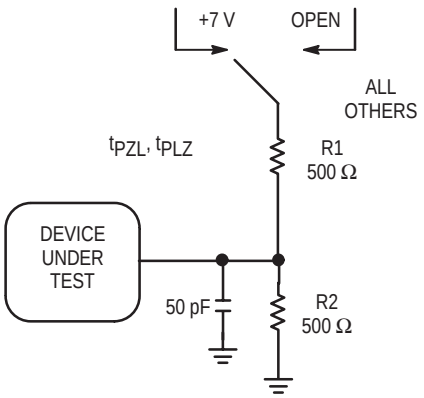
SWITCHING CIRCUIT AND WAVEFORMS

Switching Circuit PECL:

PECL



TTL

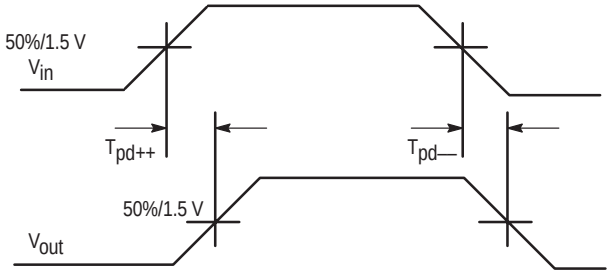


WAVEFORMS: Rise and Fall Times

PECL/TTL

Propagation Delay — Single Ended

PECL/TTL



MC10H643, MC100H643

Dual Supply ECL to TTL 1:8 Clock Driver

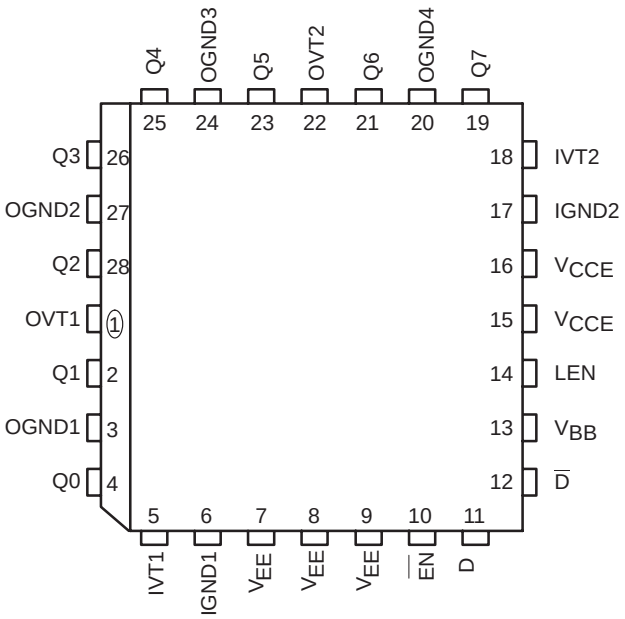
The MC10H/100H643 is a dual supply, low skew translating 1:8 clock driver. Devices in the Motorola H600 translator series utilize the 28–lead PLCC for optimal power pinning, signal flow through and electrical performance. The dual–supply H643 is similar to the H641, which is a single–supply 1:9 version of the same function.

The device features a 48mA TTL output stage, with AC performance specified into a 50pF load capacitance. A Latch is provided on–chip. When LEN is LOW (or left open, in which case it is pulled LOW by the internal pulldowns) the latch is transparent. A HIGH on the enable pin ($\overline{EN}$) forces all outputs LOW.

The 10H version is compatible with MECL 10H™ ECL logic levels. The 100H version is compatible with 100K levels.

- ECL/TTL Version of Popular ECLinPS™ E111
- Low Skew Within Device 0.5ns
- Guaranteed Skew Spec Part–to–Part 1.0ns
- Latch
- Differential Internal Design
- V_{BB} Output
- Dual Supply
- Reset/Enable
- Multiple TTL and ECL Power/Ground Pins

Pinout: 28–Lead PLCC (Top View)



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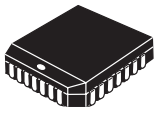
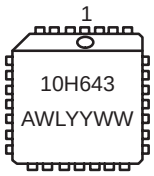


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

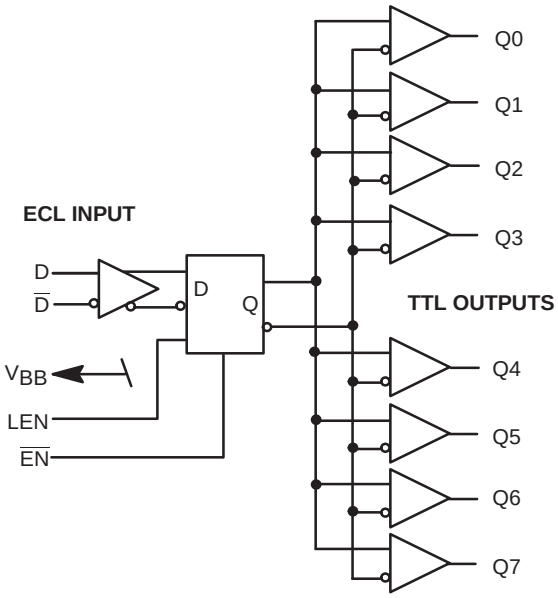
PIN NAMES

PIN	FUNCTION
OGND	TTL Output Ground (0V)
OVT	TTL Output V_{CC} (+5.0V)
IGND	Internal TTL GND (0V)
IVT	Internal TTL V_{CC} (+5.0V)
V_{EE}	ECL V_{EE} (–5.2/–4.5V)
V_{CCE}	ECL Ground (0V)
D, $\overline{D}$	Signal Input (ECL)
V_{BB}	V_{BB} Reference Output
Q0–Q7	Signal Outputs (TTL)
$\overline{EN}$	Enable Input (ECL)
LEN	Latch Enable Input (ECL)

ORDERING INFORMATION

Device	Package	Shipping
MC10H643FN	PLCC–28	37 Units/Rail
MC100H643FN	PLCC–28	37 Units/Rail

LOGIC DIAGRAM



DC CHARACTERISTICS (IVT = OVT = 5.0V ±5%; V_{EE} = –5.2V ±5% (10H Version); V_{EE} = –4.2V to 5.5V (100H Version))

Symbol	Characteristic		0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
I_{EE}	Power Supply Current	ECL	–	42	–	42	–	42	mA	V_{EE} Pins
I_{CCL}		TTL	–	106	–	106	–	106	mA	Total all OVT
I_{CCH}			–	95	–	95	–	95	mA	and IVT pins

AC CHARACTERISTICS (IVT = OVT = 5.0V ±5%; V_{EE} = –5.2V ±10% (10H); –4.2V to 5.5V (100H); V_{CCE} = GND)

Symbol	Characteristic	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
t_{PLH}	Propagation Delay to Output								
	D	4.0	5.0	4.1	5.1	4.4	5.4		
	LEN	3.5	5.5	3.5	5.5	3.9	5.9	ns	CL = 50pF
	$\overline{EN}$	3.5	5.5	3.5	5.5	3.9	5.9		
t_{SKEW}	Within–Device Skew	–	0.5	–	0.5		0.5	ns	Note 1
tw	Pulse Width Out								CL = 50pF
	HIGH or LOW	9.0	11.0	9.0	11.0	9.0	11.0	ns	
	@ f_{out} = 50MHz								Note 2
t_S	Setup Time								
	D	0.75	–	0.75	–	0.75	–	ns	
t_h	Hold Time								
	D	0.75	–	0.75	–	0.75	–	ns	
t_{RR}	Recovery Time								
	LEN	1.25	–	1.25	–	1.25	–	ns	
	$\overline{EN}$	1.25	–	1.25	–	1.25	–		
t_{pw}	Minimum Pulse Width								
	LEN	1.5	–	1.5	–	1.5	–	ns	
	$\overline{EN}$	1.5	–	1.5	–	1.5	–		
t_r	Rise / Fall Times								
t_f	0.8 V – 2.0 V	–	1.2	–	1.2	–	1.2	ns	CL = 50pF

1. Within–Device skew defined as identical transitions on similar paths through a device.
2. Pulse width is defined relative to 1.5V measurement points on the ouput waveform.

TRUTH TABLE

D	LEN	EN	Q
L	L	L	L
H	L	L	H
X	H	L	Q_O
X	X	H	L

DC TTL CHARACTERISTICS

(IVT = OVT = 5.0V ±5%; V_{EE} = –5.2V ±5% (10H Version); V_{EE} = –4.2V to 5.5V (100H Version))

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage	2.5 2.0	– –	2.5 2.0	– –	2.5 2.0	– –	V	I_{OH} = –3.0mA I_{OH} = –15mA
V_{OL}	Output LOW Voltage	–	0.5	–	0.5	–	0.5	V	I_{OH} = 48mA
IOS	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0V

10H ECL DC CHARACTERISTICS

(IVT = OVT = 5.0V ±5%; V_{EE} = –5.2V ±5% (10H Version); V_{EE} = –4.2V to 5.5V (100H Version))

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	– 0.5	225 –	– 0.5	175 –	– 0.5	175 –	μA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1170 –1950	–840 –1480	–1130 –1950	–810 –1480	–1070 –1950	–735 –1450	mV	
V_{BB}	Output Reference Voltage	–1380	–1270	–1350	–1250	–1310	–1190	mV	

100H ECL DC CHARACTERISTICS (IVT = OVT = 5.0V ±5%; V_{EE} = –5.2V ±5% (10H); V_{EE} = –4.2V to 5.5V (100H))

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	– 0.5	225 –	– 0.5	175 –	– 0.5	175 –	μA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	mV	
V_{BB}	Output Reference Voltage	–1380	–1260	–1380	–1260	–1380	–1260	mV	

MC10H644, MC10H644

68030/040 PECL to TTL Clock Driver

The MC10H/100H644 generates the necessary clocks for the 68030, 68040 and similar microprocessors. The device is functionally equivalent to the H640, but with fewer outputs in a smaller outline 20–lead PLCC package. It is guaranteed to meet the clock specifications required by the 68030 and 68040 in terms of part–to–part skew, within–part skew and also duty cycle skew.

The user has a choice of using either TTL or PECL (ECL referenced to +5.0V) for the input clock. TTL clocks are typically used in present MPU systems. However, as clock speeds increase to 50MHz and beyond, the inherent superiority of ECL (particularly differential ECL) as a means of clock signal distribution becomes increasingly evident. The H644 also uses differential ECL internally to achieve its superior skew characteristic.

The H644 includes divide–by–two and divide–by–four stages, both to achieve the necessary duty cycle and skew to generate MPU clocks as required. A typical 50MHz processor application would use an input clock running at 100MHz, thus obtaining output clocks at 50MHz and 25MHz (see Logic Symbol).

The 10H version is compatible with MECL 10H™ ECL logic levels, while the 100H version is compatible with 100K levels (referenced to +5.0V).

- Generates Clocks for 68030/040
- Meets 68030/040 Skew Requirements
- TTL or PECL Input Clock
- Extra TTL and ECL Power/Ground Pins
- Within Device Skew on Similar Paths is 0.5 ns
- Asynchronous Reset
- Single +5.0V Supply

Function

Reset (R): LOW on RESET forces all Q outputs LOW and all $\overline{Q}$ outputs HIGH.

Synchronized Outputs: The device is designed to have the POS edges of the ÷2 and ÷4 outputs synchronized.

Select (SEL): LOW selects the PECL input source (DE/$\overline{DE}$). HIGH selects the TTL input source (DT).

The H644 also contains circuitry to force a stable state of the PECL input differential pair, should both sides be left open. In this case, the DE side of the input is pulled LOW, and $\overline{DE}$ goes HIGH.

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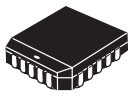
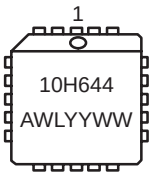


PLCC–20
FN SUFFIX
CASE 775

MARKING DIAGRAM

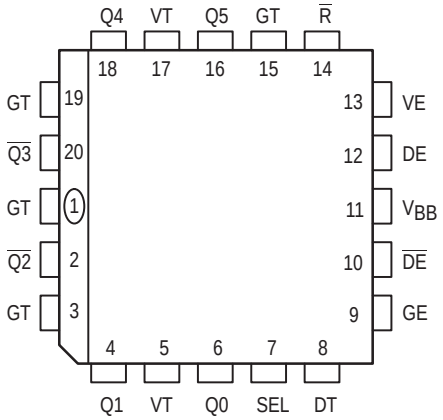


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

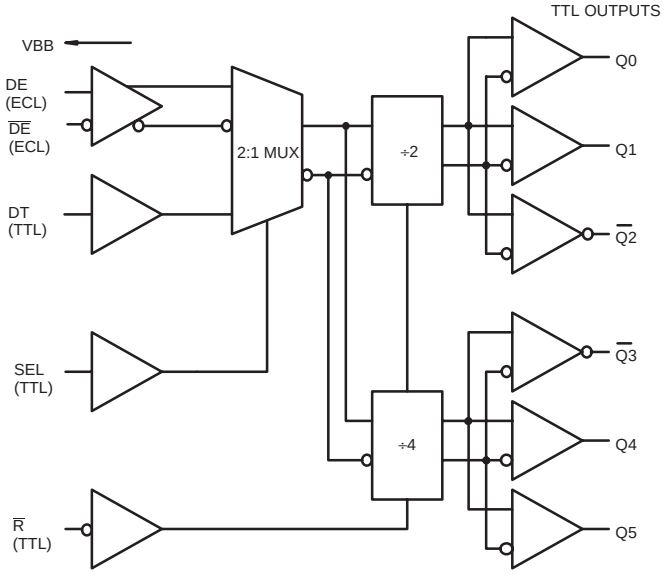
ORDERING INFORMATION

Device	Package	Shipping
MC10H644FN	PLCC–20	37 Units/Rail
MC100H644FN	PLCC–20	37 Units/Rail

Pinout: 20–Lead PLCC (Top View)



LOGIC DIAGRAM



PIN NAMES

PIN	FUNCTION
GT	TTL Ground (0V)
VT	TTL V_{CC} (+5.0V)
VE	ECL V_{CC} (+5.0V)
GE	ECL Ground (0V)
DE, $\overline{DE}$	ECL Signal Input (positive ECL)
V_{BB}	V_{BB} Reference Output
DT	TTL Signal Input
Qn, $\overline{Qn}$	Signal Outputs (TTL)
SEL	Input Select (TTL)
$\overline{R}$	Reset (TTL)

AC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic		0°C		25°C		85°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay ECL D to Output	All Outputs	5.8	6.8	5.7	6.7	6.1	7.1	ns	CL = 50pF
t_{PLH}	Propagation Delay TTL D to Output		5.7	6.7	5.7	6.7	6.0	7.0	ns	CL = 50pF
t_{skwd}*	Within–Device Skew	Q0, 1, 4, 5	–	0.5	–	0.5	–	0.5	ns	CL = 50pF
t_{skwd}*	Within–Device Skew	$\overline{Q2}$, $\overline{Q3}$	–	0.5	–	0.5	–	0.5	ns	CL = 50pF
t_{skwd}*	Within–Device Skew	All Outputs	–	1.5	–	1.5	–	1.5	ns	CL = 50pF
$t_{skp–p}$*	Part–to–Part Skew	Q0, 1, 4, 5	–	1.0	–	1.0	–	1.0	ns	CL = 50pF
t_{PD}	Propagation Delay R to Output	All Outputs	4.3	7.3	4.3	7.3	4.5	7.5	ns	CL = 50pF
t_R t_F	Output Rise/Fall Time 0.8V – 2.0V	All Outputs	–	1.6	–	1.6	–	1.6	ns	CL = 50pF
f_{max}	Maximum Input Frequency		135	–	135	–	135	–	MHz	CL = 50pF
TW	Minimum Pulse Width Reset		1.5	–	1.5	–	1.5	–	ns	
t_{rr}	Reset Recovery Time		1.25	–	1.25	–	1.25	–	ns	
T_{PW}	Pulse Width Out High or Low @ f_{in} = 100 MHz and CL = 50 pf	Q0, 1	9.5	10.5	9.5	10.5	9.5	10.5	ns	CL = 50pf Relative 1.5V
TS	Setup Time SEL to DE, DT		2.0	–	2.0	–	2.0	–	ns	
TH	Hold Time SEL to DE, DT		2.0	–	2.0	–	2.0	–	ns	

* Skews are specified for Identical Edges

DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic		0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
I_{EE}	Power Supply Current	ECL		65		65		65	mA	VE Pin
I_{CC}		TTL		85		85		85	mA	Total all V_T pins

TTL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0	 0.8	2.0	 0.8	2.0	 0.8	V	
I_{IH}	Input HIGH Current		20 100		20 100		20 100	μA	V_{IN} = 2.7 V V_{IN} = 7.0 V
I_{IL}	Input LOW Current		–0.6		–0.6		–0.6	mA	V_{IN} = 0.5 V
V_{OH}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = –3.0 mA I_{OH} = –24 mA
V_{OL}	Output LOW Voltage		0.5		0.5		0.5	V	I_{OL} = 24 mA
V_{IK}	Input Clamp Voltage		–1.2		–1.2		–1.2	V	I_{IN} = –18 mA
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0 V

10H PECL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	175	 0.5	175	μA	
V_{IH}* V_{IL}*	Input HIGH Voltage Input LOW Voltage	3.83 3.05	4.16 3.52	3.87 3.05	4.19 3.52	3.94 3.05	4.28 3.55	V	VE = 5.0 V
V_{BB}*	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	VE = 5.0 V

100H PECL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	175	 0.5	175	μA	
V_{IH}* V_{IL}*	Input HIGH Voltage Input LOW Voltage	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	V	VE = 5.0 V
V_{BB}*	Output Reference Voltage	3.62	3.74	3.62	3.74	3.62	3.74	V	VE = 5.0 V

* NOTE: PECL levels are referenced to V_{CC} and will vary 1:1 with the power supply. The values shown are for V_{CC} = 5.0 V.
Only corresponds to ECL Clock Inputs.

MC10H645

1:9 TTL Clock Driver

The MC10H645 is a single supply, low skew, TTL I/O 1:9 Clock Driver. Devices in the Motorola H600 clock driver family utiize the 28–lead PLCC for optimal power and signal pin placement.

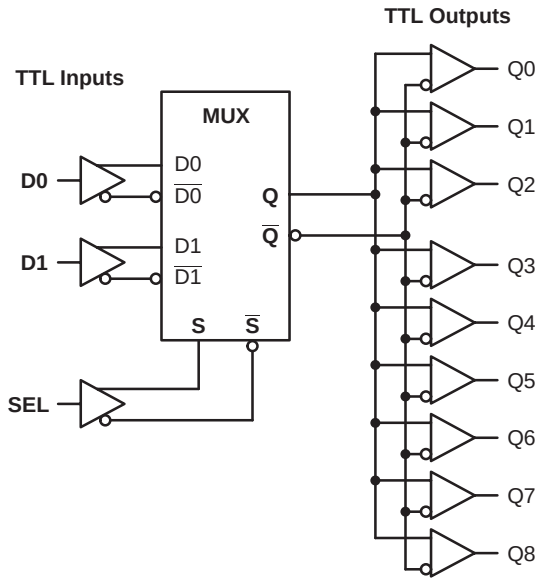
The device features a 24mA TTL ouput stage with AC performance specified into a 50pF load capacitance. A 2:1 input mux is provided on chip to allow for distributing both system and diagnostic clock signals or designing clock redundancy into a system. With the SEL input held LOW the DO input will be selected, while the D1 input is selected when the SEL input is forced HIGH.

- Low Skew Typically 0.65ns Within Device
- Guaranteed Skew Spec 1.25ns Part–to–Part
- Input Clock Muxing
- Differential ECL Internal Design
- Single Supply
- Extra TTL and ECL Power/Ground Pins

PIN NAMES

PIN	FUNCTION
GT	TTL Ground (0V)
VT	TTL V_{CC} (+5.0V)
VE	ECL V_{CC} (+5.0V)
GE	ECL Ground (0V)
Dn	TTL Signal Input
Q0 – Q8	TTL Signal Outputs
SEL	TTL Mux Select

LOGIC DIAGRAM



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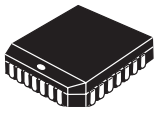
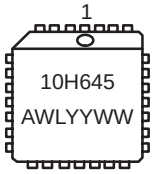


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAM

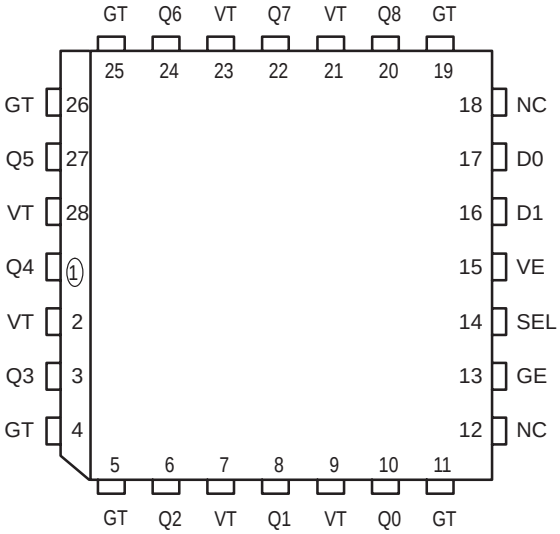


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H645FN	PLCC–28	37 Units/Rail
MC100H645FN	PLCC–28	37 Units/Rail

Pinout: 28–Lead PLCC (Top View)



PIN DESCRIPTIONS

Pin	Symbol	Description	Pin	Symbol	Description
1	Q4	Signal Output (TTL)	15	VE	ECL V_{CC} (+5.0V)
2	VT	TTL V_{CC} (+5.0V)	16	D1	Signal Input (TTL)
3	Q3	Signal Output (TTL)	17	D0	Signal Input (TTL)
4	GT	TTL Ground (0V)	18	NC	No Connection
5	GT	TTL Ground (0V)	19	GT	TTL Ground (0V)
6	Q2	Signal Output (TTL)	20	Q8	Signal Output (TTL)
7	VT	TTL V_{CC} (+5.0V)	21	VT	TTL V_{CC} (+5.0V)
8	Q1	Signal Output (TTL)	22	Q7	Signal Output (TTL)
9	VT	TTL V_{CC} (+5.0V)	23	VT	TTL V_{CC} (+5.0V)
10	Q0	Signal Output (TTL)	24	Q6	Signal Output (TTL)
11	GT	TTL Ground (0V)	25	GT	TTL Ground (0V)
12	NC	No Connection	26	GT	TTL Ground (0V)
13	GE	ECL Ground	27	Q5	Signal Output (TTL)
14	SEL	Select Input (TTL)	28	VT	TTL V_{CC} (+5.0V)

TRUTH TABLE

D0	D1	SEL	Q
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

ABSOLUTE RATINGS (Do not exceed)

Symbol	Characteristic	Value	Unit
VE (ECL)	Power Supply Voltage	–0.5 to +7.0	V
VT (TTL)	Power Supply Voltage	–0.5 to +7.0	V
VI (TTL)	Input Voltage	–0.5 to +7.0	V
V_{out}	Disabled 3–State Output	0.0 to V_T	V
T_{stg}	Storage Temperature	–65 to 150	°C
T_{amb}	Operating Temperature	0.0 to +85	°C

DC CHARACTERISTICS (VT = VE = 5.0V ±5%)

Symbol	Characteristic		0°C		25°C		85°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
I_{EE}	Power Supply Current	ECL		30		30		30	mA	VE Pin
I_{CCH}		TTL		30		30		30	mA	Total all VT pins
I_{CCL}				35		35		35	mA	
V_{OH}	Output HIGH Voltage		2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = –3.0mA I_{OH} = –15mA
V_{OL}	Output LOW Voltage			0.5		0.5		0.5	V	I_{OL} = 24mA
I_{OS}	Output Short Circuit Current		–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0V

TTL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0	 0.8	2.0	 0.8	2.0	 0.8	V	
I_{IH}	Input HIGH Current		20 100		20 100		20 100	μA	V_{IN} = 2.7 V V_{IN} = 7.0 V
I_{IL}	Input LOW Current		–0.6		–0.6		–0.6	mA	V_{IN} = 0.5 V
V_{OH}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = –3.0 mA I_{OH} = –24 mA
V_{OL}	Output LOW Voltage		0.5		0.5		0.5	V	I_{OL} = 24 mA
V_{IK}	Input Clamp Voltage		–1.2		–1.2		–1.2	V	I_{IN} = –18 mA
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0 V

AC CHARACTERISTICS (VT = VE = 5.0V ±5%)

Symbol	Characteristic		0°C		25°C		85°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_0 to Output Only	Q0–Q8	4.8	5.8	4.8	5.8	5.2	6.2	ns	CL = 50pF
t_{PLH}	Propagation Delay D_1 to Output		4.8	5.8	4.8	5.8	5.2	6.2	ns	
t_{PHL}	Propagation Delay D_0 to Output D_1 to Output		 4.8 4.8	 5.8 5.8	 4.8 4.8	 5.8 5.8	 5.2 5.2	 6.2 6.2	ns	
t_{skpp}	Part–to–Part Skew D_0 to Output Only			1.0		1.0		1.0	ns	
t_{skwd}*	Within–Device Skew D_0 to Output Only			0.65		0.65		0.65	ns	
t_{PLH}	Propagation Delay SEL to Q	Q0–Q8	4.5	6.5	5.0	7.0	5.2	7.2	ns	CL = 50pF
t_r t_f	Output Rise/Fall Time 0.8V to 2.0V	Q0–Q8	0.5 0.5	2.5 2.5	0.5 0.5	2.5 2.5	0.5 0.5	2.5 2.5	ns	CL = 50pF
t_S	Setup Time SEL to D		 1.0		 1.0		 1.0		ns	

* Within–Device Skew defined as identical transitions on similar paths through a device.

DUTY CYCLE SPECIFICATIONS (0°C ≤ TA ≤ 85°C; Duty Cycle Measured Relative to 1.5V)

Symbol	Characteristic		Min	Nom	Max	Unit	Condition
PW	Range of V_{CC} and CL to Meet Min Pulse Width (HIGH or LOW) at f_{out} ≤50MHz	V_{CC} CL PW	4.875 10.0 9.0	5.0	5.125 50.0 11.0	V pF ns	All Outputs

MC10H646, MC10H646

PECL/TTL–TTL 1:8 Clock Distribution Chip

The MC10H/100H646 is a single supply, low skew translating 1:8 clock driver. Devices in the Motorola H600 translator series utilize the 28–lead PLCC for optimal power pinning, signal flow through and electrical performance. The single supply H646 is similar to the H643, which is a dual supply 1:8 version of the same function.

The H646 was designed specifically to drive series terminated transmission lines. Special techniques were used to match the HIGH and LOW output impedances to about 7ohms. This simplifies the choice of the termination resistor for series terminated applications. To match the HIGH and LOW output impedances, it was necessary to remove the standard I_{OS} limiting resistor. As a result, the user should take care in preventing an output short to ground as the part will be permanently damaged.

The H646 device meets all of the requirements for driving the 60 and 66MHz Pentium Microprocessor. The device has no PLL components, which greatly simplifies its implementation into a digital design. The eight copies of the clock allows for point–to–point clock distribution to simplify board layout and optimize signal integrity.

The H646 provides differential PECL inputs for picking up LOW skew PECL clocks from the backplane and distributing it to TTL loads on a daughter board. When used in conjunction with the MC10/100E111, very low skew, very wide clock trees can be designed. In addition, a TTL level clock input is provided for flexibility. Note that only one of the inputs can be used on a single chip. For correct operation, the unused input pins should be left open.

The Output Enable pin forces the outputs into a high impedance state when a logic 0 is applied.

The output buffers of the H646 can drive two series terminated, 50Ω transmission lines each. This capability allows the H646 to drive up to 16 different point–to–point clock loads. Refer to the Applications section for a more detailed discussion in this area.

The 10H version is compatible with MECL 10H™ ECL logic levels. The 100H version is compatible with 100K levels.

- PECL/TTL–TTL Version of Popular ECLinPS™ E111
- Low Skew
- Guaranteed Skew Spec
- Tri–State Enable
- Differential Internal Design
- V_{BB} Output
- Single Supply
- Extra TTL and ECL Power/Ground Pins
- Matched High and Low Output Impedance
- Meets Specifications Required to Drive the Pentium™ Microprocessor

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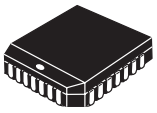
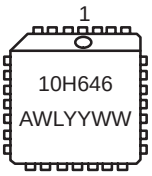


PLCC–28
FN SUFFIX
CASE 776

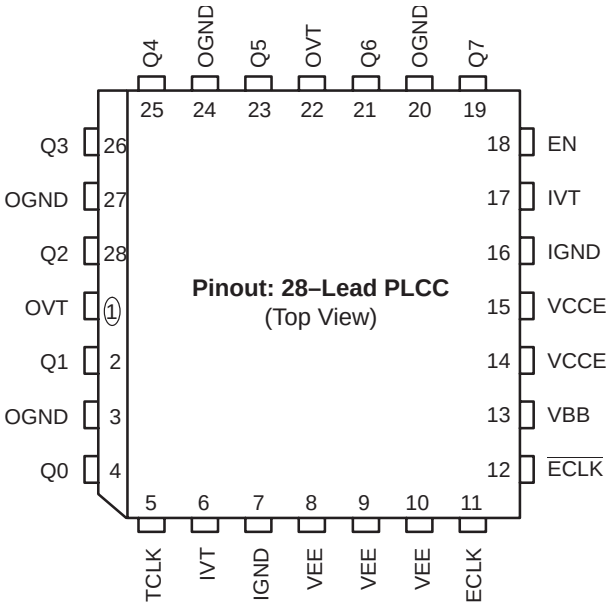
MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H646FN	PLCC–28	37 Units/Rail
MC100H646FN	PLCC–28	37 Units/Rail



PIN NAMES

PIN	FUNCTION
OGND	TTL Output Ground (0V)
OVT	TTL Output V_{CC} (+5.0V)
IGND	Internal TTL GND (0V)
IVT	Internal TTL V_{CC} (+5.0V)
V_{EE}	ECL V_{EE} (0V)
V_{CCE}	ECL Ground (5.0V)
ECLK, $\overline{ECLK}$	Differential Signal Input (PECL)
V_{BB}	V_{BB} Reference Output
Q0–Q7	Signal Outputs (TTL)
EN	Tri–State Enable Input (TTL)

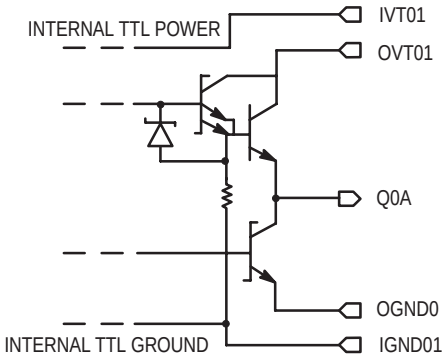
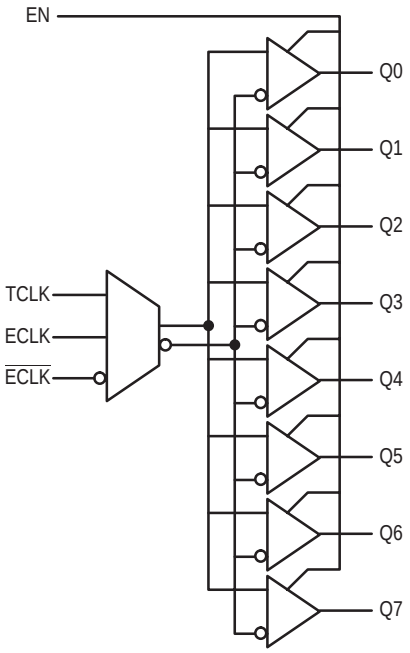


Figure 1. Output Structure

LOGIC DIAGRAM



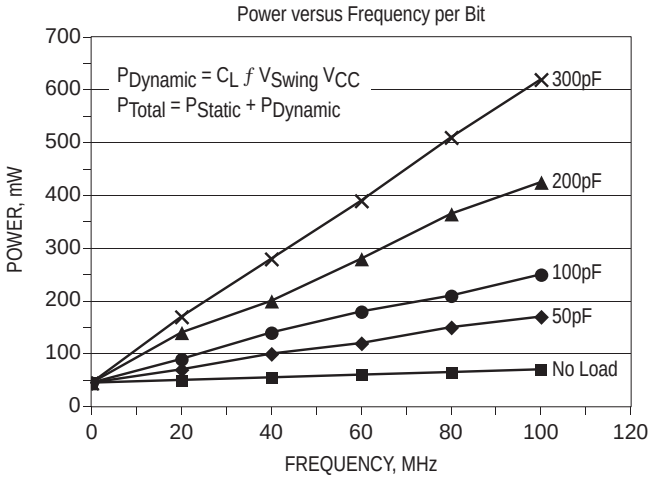


Figure 2. Power versus Frequency (Typical)

TRUTH TABLE

TCLK	ECLK	$\overline{ECLK}$	EN	Q
GND	L	H	H	L
GND	H	L	H	H
H	GND	GND	H	H
L	GND	GND	H	L
X	X	X	L	Z

L = Low Voltage Level; H = High Voltage Level; Z = Tristate

DC CHARACTERISTICS (IVT = OVT = VCCE = 5.0V ±5%)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage	2.6	– –	2.6	– –	2.6	– –	V	I_{OH} = 24mA
V_{OL}	Output LOW Voltage	–	0.5	–	0.5	–	0.5	V	I_{OL} = 48mA
IOS	Output Short Circuit Current	–	–	–	–	–	–	mA	See Note **1**

1. The outputs must not be shorted to ground, as this will result in permanent damage to the device. The high drive outputs of this device do not include a limiting IOS resistor.

TTL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0	 0.8	2.0	 0.8	2.0	 0.8	V	
I_{IH}	Input HIGH Current		20 100		20 100		20 100	μA	V_{IN} = 2.7 V V_{IN} = 7.0 V
I_{IL}	Input LOW Current		–0.6		–0.6		–0.6	mA	V_{IN} = 0.5 V
V_{OH}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = –3.0 mA I_{OH} = –24 mA
V_{OL}	Output LOW Voltage		0.5		0.5		0.5	V	I_{OL} = 24 mA
V_{IK}	Input Clamp Voltage		–1.2		–1.2		–1.2	V	I_{IN} = –18 mA

10H PECL DC CHARACTERISTICS (IVT = OVT = VCCE = 5.0V ±5%)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Notes
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current			225			175			175	μA	
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA	
V_{IH}	Input HIGH Voltage	3.83		4.16	3.87		4.19	3.94		4.28	V	IVT = IVO = VCCE = 5.0V (**1**)
V_{IL}	Input LOW Voltage	3.05		3.52	3.05		3.52	3.05		3.555	V	IVT = IVO = VCCE = 5.0V (**1**)
V_{BB}	Output Reference Voltage	3.62		3.73	3.65		3.75	3.69		3.81	V	IVT = IVO = VCCE = 5.0V (**1**)

100H PECL DC CHARACTERISTICS (IVT = OVT = VCCE = 5.0V ±5%)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Notes
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current			225			175			175	μA	
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA	
V_{IH}	Input HIGH Voltage	3.835		4.12	3.835		4.12	3.835		3.835	V	IVT = IVO = VCCE = 5.0V (**1**)
V_{IL}	Input LOW Voltage	3.19		3.525	3.19		3.525	3.19		3.525	V	IVT = IVO = VCCE = 5.0V (**1**)
V_{BB}	Output Reference Voltage	3.62		3.74	3.62		3.74	3.62		3.74	V	IVT = IVO = VCCE = 5.0V (**1**)

1. ECL V_{IH}, V_{IL} and V_{BB} are referenced to VCCE and will vary 1:1 with the power supply. The levels shown are for IVT = IVO = VCCE = 5.0V

DC CHARACTERISTICS (IVT = OVT = VCCE = 5.0V ±5%)

Symbol	Characteristic	0°C		25°C			85°C		Unit	Condition
		Min	Max	Min	Typ	Max	Min	Max		
I_{CCL}	Power Supply Current		185		166	185		185	mA	Total all OVT, IVT, and VCCE pins
I_{CCH}			175		154	175		175	mA	
I_{CCZ}			210			210		210		

AC CHARACTERISTICS (IVT = OVT = VCCE = 5.0V ±5%)

Symbol	Characteristic		0°C		25°C		85°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	ECLK to Q TCLK to Q	4.8 5.1	5.8 6.4	5.0 5.3	6.0 6.4	5.6 5.7	6.6 7.0	ns	
t_{PHL}	Propagation Delay	ECLK to Q TCLK to Q	4.4 4.7	5.4 6.0	4.4 4.8	5.4 5.9	4.8 5.2	5.8 6.5	ns	
$t_{SK(O)}$	Output Skew	Q0, Q3, Q4, Q7 Q1, Q2, Q5 Q0–Q7		350 350 500		350 350 500		350 350 500	ps	Note 1, 6
$t_{SK(PR)}$	Process Skew	ECLK to Q TCLK to Q		1.0 1.3		1.0 1.1		1.0 1.3	ns	Note 2, 6
$t_{SK(P)}$	Pulse Skew	$\Delta t_{PLH} - t_{PHL}$		1.0		1.0		1.0	ns	
t_r, t_f	Rise/Fall Time		0.3	1.5	0.3	1.5	0.3	1.5	ns	
t_{PW}	Output Pulse Width	66MHz @ 2.0V 66MHz @ 0.8V 60MHz @ 2.0V 60MHz @ 0.8V	5.5 5.5 6.0 6.0		5.5 5.5 6.0 6.0		5.5 5.5 6.0 6.0		ns	Note 3, 6
$t_{Stability}$	Clock Stability			±75		±75		±75	ps	Note 4, 6
F_{MAX}	Maximum Input Frequency			80		80		80	MHz	Note 5, 6

1. Output skew defined for identical output transitions.
2. Process skew is valid for V_{CC} = 5.0V ±5%.
3. Parameters guaranteed by $t_{SK(P)}$ and t_r, t_f specification limits.
4. Clock stability is the period variation between two successive rising edges.
5. For series terminated lines. See Applications section for F_{MAX} enhancement techniques.
6. All AC specifications tested driving 50Ω series terminated transmission lines at 80MHz.

MC10H680, MC10H680

4-Bit Differential ECL Bus to TTL Bus Transceiver

The MC10H/100H680 is a dual supply 4–bit differential ECL bus to TTL bus transceiver. It is designed to allow the system designer to no longer be limited in bus speed associated with standard TTL busses. Using a differential ECL Bus will increase the frequency of operation and increase noise immunity.

Both the TTL and the ECL ports are capable of driving a bus. The ECL outputs have the ability to drive 25 Ω, allowing both ends of the bus line to be terminated in the characteristic impedance of 50 Ω. The TTL outputs are specified to source 15 mA and sink 48 mA, allowing the ability to drive highly capacitive loads.

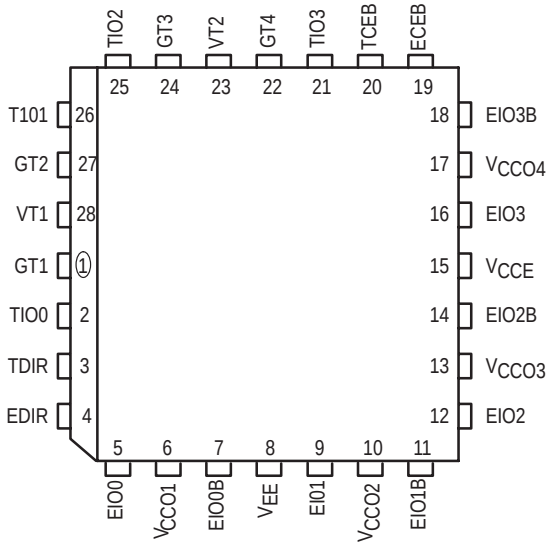
The ECL output levels are V_{OH} approximately equal to –1.0 V and V_{OL} cutoff equal to –2.0 V (VTT). When the ECL ports are disabled both EIOx and EIOxB go to the V_{OL} cutoff level. The ECL input receivers have special circuitry which detects this disabled condition, prevents oscillation, and forces the TTL output to the low state. The noise margin in this disabled state is greater than 600 mV. Multiple ECL V_{CCO} pins are utilized to minimize switching noise.

The TTL ports have standard levels. The TTL input receivers have PNP input devices to significantly reduce loading. Multiple TTL power and ground pins are utilized to minimize switching noise.

The control pins (EDIR and ECEB) of the 10H version is compatible with MECL 10H ECL logic levels. The control pins of the 100H version are compatible with 100K levels.

- Differential ECL Bus (25 Ω) I/O Ports
- High Drive TTL Bus I/O Ports
- Extra TTL and ECL Power/Ground Pins to Minimize Switching Noise
- Dual Supply
- Direction and Chip Enable Control Pins

Pinout: 28–Lead PLCC (Top View)



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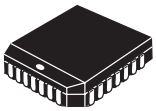
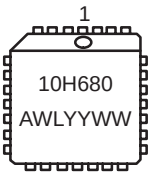


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H680FN	PLCC–28	37 Units/Rail
MC100H680FN	PLCC–28	37 Units/Rail

PIN DESCRIPTIONS

Pin	Symbol	Function
1	GT1	TTL Ground 1
2	TIO0	TTL I/O Bit 0
3	TDIR	TTL Direction Control
4	EDIR	ECL Direction Control
5	EIO0	ECL I/O Bit 0
6	VCCO1	ECL VCC 1 (0V) – Outputs
7	EIO0B	ECL I/O Bit 0 Bar
8	VEE	ECL Supply (–5.2/–4.5V)
9	EIO1	ECL I/O Bit 1
10	VCCO2	ECL VCC 2 (0V) – Outputs
11	EIO1B	ECL I/O Bit 1 Bar
12	EIO2	ECL I/O Bit 2
13	VCCO3	ECL VCC 3 (0V) – Outputs
14	EIO2B	ECL I/O Bit 2 Bar
15	VCCE	ECL VCC (0V)
16	EIO3	ECL I/O Bit 3
17	VCCO4	ECL VCC 4 (0V) – Outputs
18	EIO3B	ECL I/O Bit 3 Bar
19	ECEB	ECL Chip Enable Bar Control
20	TCEB	TTL Chip Enable Bar Control
21	TIO3	TTL I/O Bit 3
22	GT4	TTL Ground 4
23	VT2	TTL Supply 2 (5V)
24	GT3	TTL Ground 3
25	TIO2	TTL I/O Bit 2
26	TIO1	TTL I/O Bit 1
27	GT2	TTL Ground 2
28	VT1	TTL Supply 1 (5V)

TRUTH TABLE

TDIR — Direction Control TTL Levels
EDIR — Direction Control ECL Levels
TCEB — Chip Enable Bar Control TTL Levels
ECEB — Chip Enable Bar Control ECL Levels
TIN — TTL Input
TOUT — TTL Output
EIN — ECL Input
EINB — ECL Input Bar
EOUT — ECL Output
EOUTB — ECL Output Bar

H — HIGH
L — LOW
LC — ECL Low Cutoff (VTT = –2.0 V)
X — Don't Care
Z — High Impedance

ECEB	TCEB	EDIR	TDIR	EIN	EINB	EOUT	EOUTB	TIN	TOUT	COMMENTS
H	X	X	X	X	X	LC	LC	X	Z	ECL and TTL Outputs Disabled
X	H	X	X	X	X	LC	LC	X	Z	ECL and TTL Outputs Disabled
L	L	H	X	H	LC			NA	H	ECL to TTL Direction
L	L	H	X	LC	H			NA	L	ECL to TTL Direction
L	L	H	X	LC	LC			NA	L	ECL to TTL Direction (L–L Cond.)
L	L	X	H	H	LC			NA	H	ECL to TTL Direction
L	L	X	H	LC	H			NA	L	ECL to TTL Direction
L	L	X	H	LC	LC			NA	L	ECL to TTL Direction (L–L Cond.)
L	L	L	L	NA	NA	H	LC	H		TTL to ECL Direction
L	L	L	L	NA	NA	LC	H	L		TTL to ECL Direction

ABSOLUTE RATINGS (Do not exceed):

Power Supply Voltage	V_{EE} (ECL)	–8.0 to 0	Vdc
Power Supply Voltage	V_{CCT} (TTL)	–0.5 to +7.0	Vdc
Input Voltage	V_I (ECL) V_I (TTL)	0.0 to V_{EE} –0.5 to +7.0	Vdc
Disabled 3–State Output	V_{out} (TTL)	0.0 to V_{CCT}	Vdc
Output Source Current Continuous	I_{out} (ECL)	100	mAdc
Output Source Current Surge	I_{out} (ECL)	200	mAdc
Storage Temperature	T_{stg}	–65 to 150	°C
Operating Temperature	T_{amb}	0.0 to +75	°C

ECL DC CHARACTERISTICS: V_{CCT} = +5.0 V ±10%, V_{EE} = –5.2 ±5% (10H Version); V_{EE} = –4.2 V to –5.5 V (100H Version)

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{EE}	Supply Current/ECL		–110		–110		–110	mA	
I_{INH}	Input HIGH Current		225		145		145	µA	
I_{INL}	Input LOW Current	0.5		0.5		0.3		µA	
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	–1100 –2.1	–840 –2.03	–1100 –2.1	–810 –2.03	–1100 –2.1	–735 –2.03	mV V	25 Ω to –2.1 V

CONTROL INPUTS ONLY

10H ECL DC CHARACTERISTICS: V_{CCT} = +5.0 ±10%, V_{EE} = –5.2 ±5%

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1170 –1950	–840 –1480	–1130 –1950	–810 –1480	–1070 –1950	–735 –1450	mV	

CONTROL INPUTS ONLY

100H ECL DC CHARACTERISTICS: V_{CCT} = +5.0 ±10%, V_{EE} = –4.2 V to –5.5 V

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	mV	

TTL DC CHARACTERISTICS: V_{CCT} = +5.0 V ±10%, V_{EE} = –5.2 ±5% (10H Version); V_{EE} = –4.2 V to –5.5 V (100H Version)

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Standard Input Standard Input	2.0	 0.8	2.0	 0.8	2.0	 0.8	Vdc	
V_{IK}	Input Clamp		–1.2		–1.2		–1.2	Vdc	I_{IN} = –18 mA
V_{OH}	Output HIGH Voltage Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = –3.0 mA I_{OH} = –15 mA
V_{OL}	Output LOW Voltage		0.55		0.55		0.55	V	I_{OL} = 48 mA
I_{IH}*	TTL (Input HIGH) TTL (Input HIGH)		20 100		20 100		20 100	µA	V_{in} = 2.7 V V_{in} = 7.0 V
I_{IL}*	TTL (Input LOW)		–0.6		–0.6		–0.6	mA	V_{in} = 0.5 V
I_{CCL}	Supply Current		75		75		75	mA	
I_{CCH}	Supply Current		70		70		70	mA	
I_{CCZ}	Supply Current		70		70		70	mA	
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0 V

* NOTE: TTL Control Inputs only

TTL I/O DC CHARACTERISTICS ONLY

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
$I_{IH/IOZH}$ $I_{IL/IOZL}$	Output Disable Current		70 200		70 200		70 200	µA	V_{OUT} = 2.7 V V_{OUT} = 0.5 V

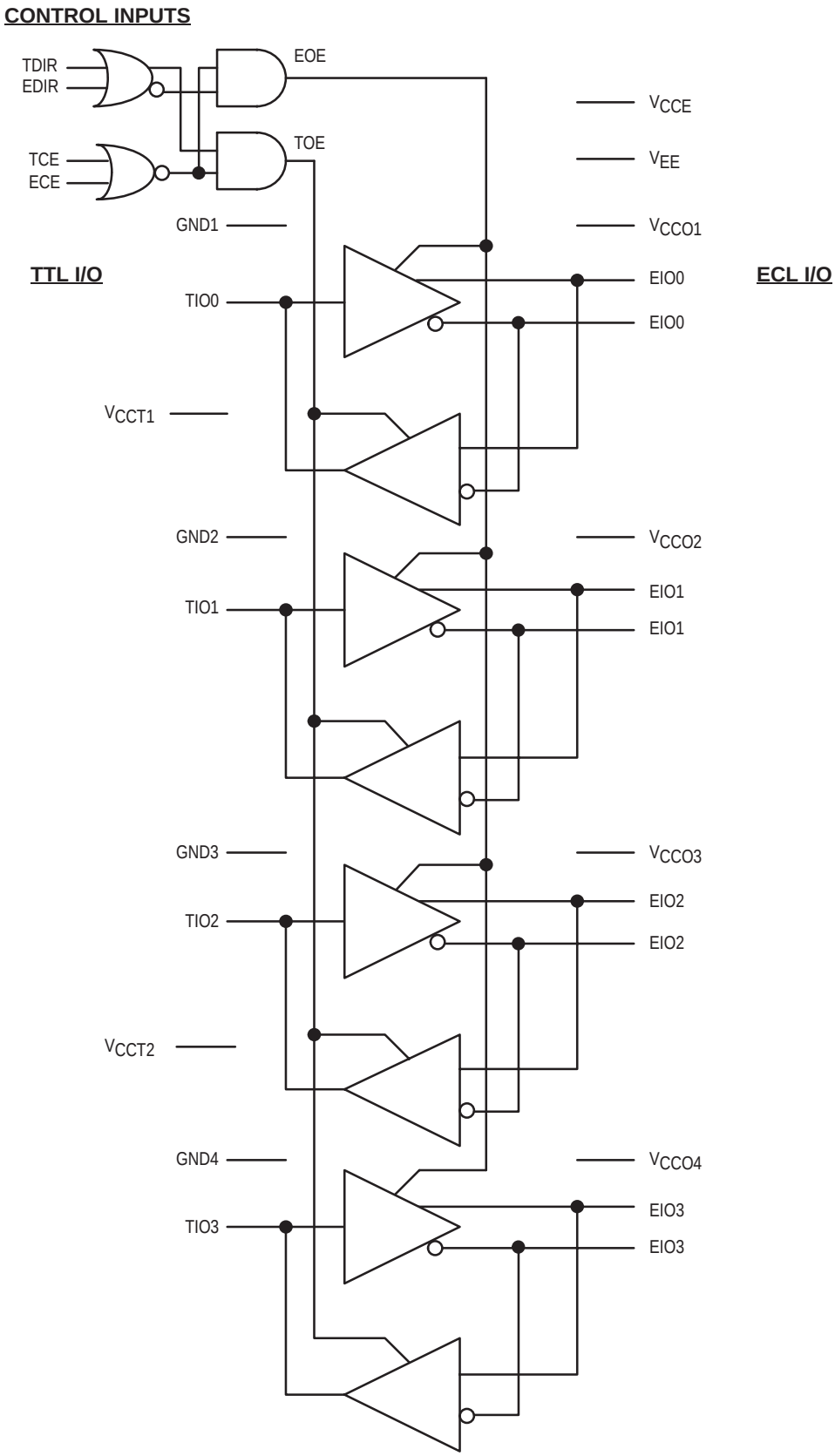
ECL TO TTL DIRECTION / AC TEST

Test Symbol	Parameter	Waveforms	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output	2, 4	2.7	4.8	2.7	4.8	2.7	4.8	ns	C_L = 50 pF
t_{PZH} t_{PZL}	ECEB to Output Enable Time	2, 5, 6	3.5 3.5	6.5 6.0	3.5 3.5	6.5 6.0	3.7 3.7	6.7 6.4	ns	C_L = 50 pF
t_{PHZ} t_{PLZ}	ECEB to Output Disable Time	2, 5, 6	3.5 3.5	8.6 6.5	3.5 3.5	8.6 6.5	3.7 3.7	8.8 7.3	ns	C_L = 50 pF
t_{PZH} t_{PZL}	TCEB to Output Enable Time	2, 5, 6	5.7 5.4	7.7 6.9	5.7 5.4	7.7 6.9	5.9 5.9	7.9 7.4	ns	C_L = 50 pF
t_{PHZ} t_{PLZ}	TCEB to Output Disable Time	2, 5, 6	4.0 4.0	8.5 5.8	4.1 4.2	8.4 6.0	4.2 4.7	8.3 6.5	ns	C_L = 50 pF
t_r/t_f	1.0 to 2.0 Vdc	3	0.4	1.5	0.4	1.5	0.4	1.5	ns	C_L = 50 pF

TTL TO ECL DIRECTION / AC TEST

Test Symbol	Parameter	Waveforms	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output	1, 4	1.8	4.6	1.8	4.6	2.0	4.9	ns	25 Ω to –2.0 V
t_{PLH} t_{PHL}	ECEB to Output	1, 4	2.9	5.1	3.0	5.2	3.4	5.7	ns	25 Ω to –2.0 V
t_{PLH} t_{PHL}	TCEB to Output	1, 4	3.4	6.3	3.5	6.6	3.8	7.4	ns	25 Ω to –2.0 V
t_r/t_f	Output Rise/Fall Time 20%–80%	1, 3	1.0	3.4	1.0	3.4	1.0	3.4	ns	25 Ω to –2.0 V

BLOCK DIAGRAM



SWITCHING CIRCUIT AND WAVEFORMS

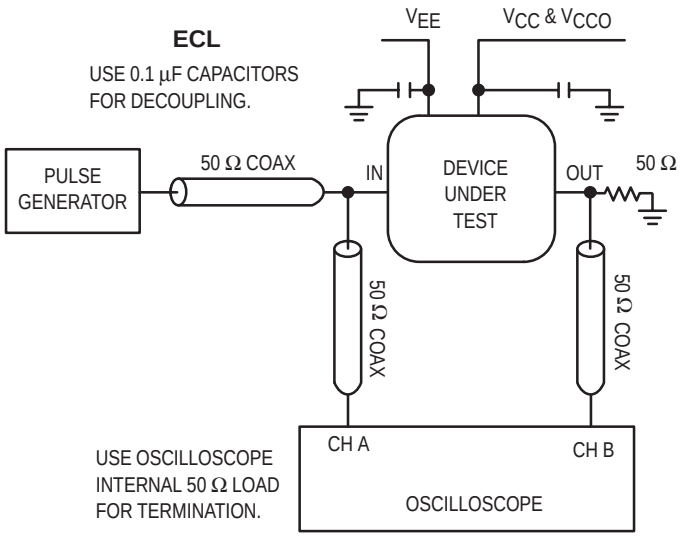


Figure 1. Switching Circuit ECL

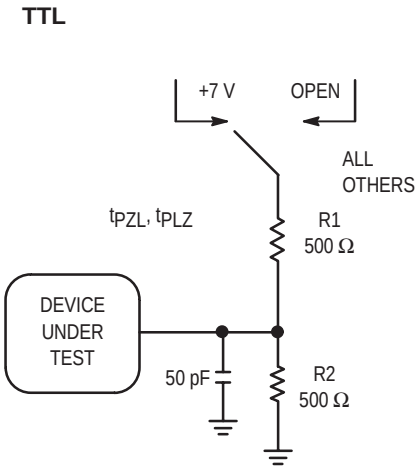


Figure 2.

ECL/TTL

Figure 3. WAVEFORMS: Rise and Fall Times

ECL/TTL

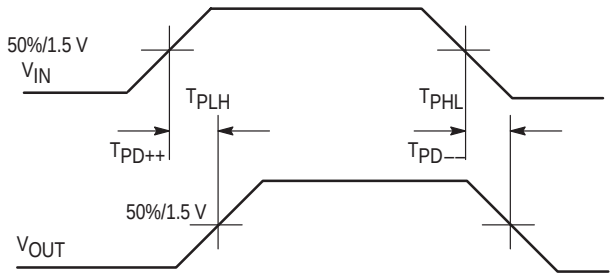


Figure 4. Propagation Delay — Single Ended

TTL

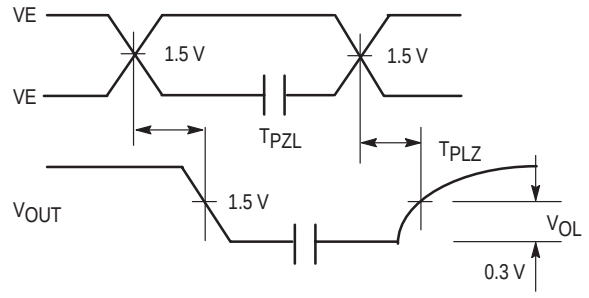


Figure 5. 3–State Output Low Enable and Disable Times

TTL

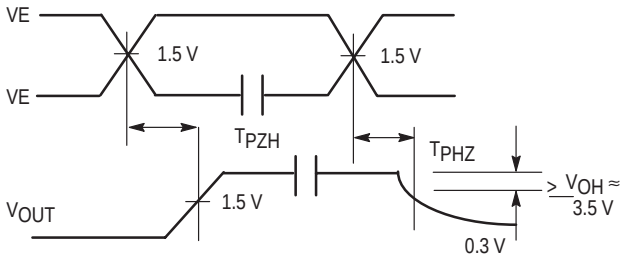


Figure 6. 3–State Output High Enable and Disable Times

MC10H681, MC10H681

Hex ECL to TTL Transceiver with Latches

The MC10/100H681 is a dual supply Hex ECL/TTL transceiver with latches in both directions. ECL controlled Direction and Chip Enable Bar pins. There are two Latch Enable pins, one for each direction.

The ECL outputs are single ended and drive 50 Ω. The TTL outputs are specified to source 15 mA and sink 48 mA, allowing the ability to drive highly capacitive loads. The high driving ability of the TTL outputs make the device ideal for bussing applications.

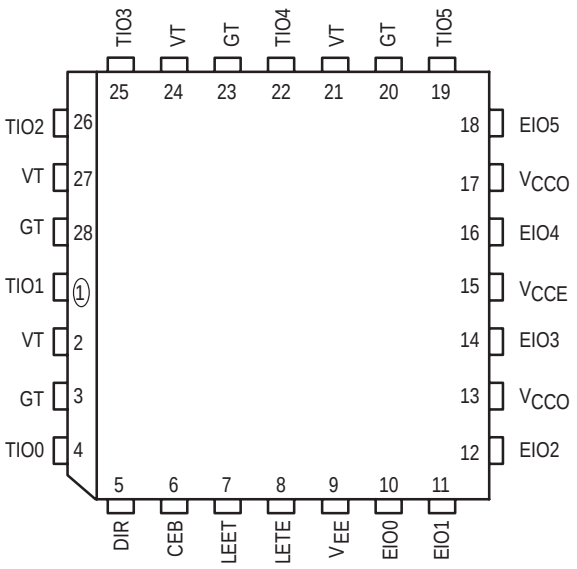
The ECL output levels are standard V_{OH} and V_{OL} cutoff equal to –2.0 V (V_{TT}). When the ECL ports are disabled the outputs go to the V_{OL} cutoff level. Multiple ECL V_{CCO} pins are utilized to minimize switching noise.

The TTL ports have standard levels. The TTL input receivers have PNP input devices to significantly reduce loading. Multiple TTL power and ground pins are utilized to minimize switching noise.

The 10H version is compatible with MECL 10H ECL logic levels. The 100H version is compatible with 100K levels.

- Separate Latch Enable Controls for each Direction
- ECL Single Ended 50 Ω I/O Port
- High Drive TTL I/O Ports
- Extra TTL and ECL Power/Ground Pins to Minimize Switching Noise
- Dual Supply
- Direction and Chip Enable Control Pins

Pinout: 28–Lead PLCC (Top View)



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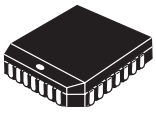
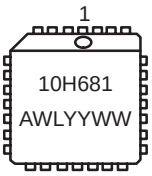


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAM

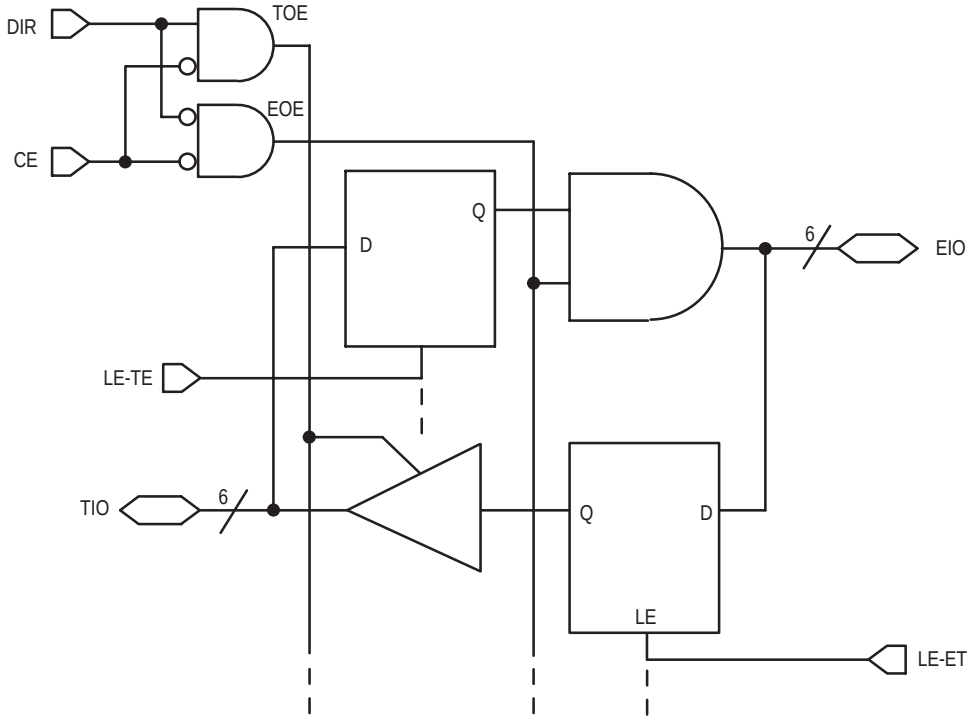


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H681FN	PLCC–28	37 Units/Rail
MC100H681FN	PLCC–28	37 Units/Rail

Pin	Symbol	Description
1	TI01	TTL I/O BIT 1
2	VT	TTL V_{CC} (5.0 V)
3	GT	TTL GND (0 V)
4	TI00	TTL I/O Bit 0
5	DIR	Direction Control (ECL)
6	CEB	Chip Enable Bar Control (ECL)
7	LEET	Latch Enable ECL-TTL Control (ECL)
8	LETE	Latch Enable TTL-ECL Control (ECL)
9	V_{EE}	ECL Supply (−5.2/−4.5 V)
10	EI00	ECL I/O BIT 0
11	EI01	ECL I/O BIT 1
12	EI02	ECL I/O BIT 2
13	V_{CCO}	ECL V_{CC} (0 V) — Outputs
14	EIO3	TTL I/O BIT 3
15	V_{CCE}	ECL V_{CC} (0 V)
16	EIO4	ECL I/O BIT 4
17	V_{CCO}	ECL V_{CC} (0 V) — Outputs
18	EIO5	ECL I/O BIT 5
19	TI05	TTL I/O BIT 5
20	GT	TTL GND (0 V)
21	VT	TTL V_{CC} (5.0 V)
22	TI04	TTL I/O BIT 4
23	GT	TTL GND (0 V)
24	VT	TTL V_{CC} (5.0 V)
25	TIO3	TTL I/O BIT 3
26	TIO2	TTL I/O BIT 2
27	VT	TTL V_{CC} (5.0 V)
28	GT	TTL V_{CC} (0 V)



TRUTH TABLE

CEB	DIR	LEET	LETE	EOUT	TOUT
H	X	X	X	Z	Z
L	H	L	L	Z	EIN
L	H	H	L	Z	Qo
L	L	L	L	TIN	Z
L	L	L	H	Qo	Z

- Hex
- Bi-Directional
- ECL/TTL Translation
- Dual Supply
- ECL Outputs, 50 Ohm S.E., V_{OH}/Cutoff
- TTL Outputs, 48 mA Sink, 15 mA Source
- Multi Power and Ground Pins
- Separate LE Controls

ECL DC CHARACTERISTICS: V_{CCT} = +5.0 V ±10%, V_{EE} = –5.2 ±5% (10H Version); V_{EE} = –4.2 V to –5.5 V (100H Version)

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{EE}	Supply Current/ECL	—	–113	—	–113	—	–113	mA	
I_{INH}	Input HIGH Current	—	225	—	145	—	145	µA	
I_{INL}	Input LOW Current	0.5	—	0.5	—	0.3	—	µA	
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	–1020 –2.1	–840 –2.03	–980 –2.1	–810 –2.03	–920 –2.1	–735 –2.03	mV V	50 Ω to –2.1 V

10H ECL DC CHARACTERISTICS: V_{CCT} = +5.0 ±10%, V_{EE} = –5.2 ±5%

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1170 –1950	–840 –1480	–1130 –1950	–810 –1480	–1070 –1950	–735 –1450	mV	

100H ECL DC CHARACTERISTICS: V_{CCT} = +5.0 ±10%, V_{EE} = –4.2 V to –5.5 V

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	mV	

ABSOLUTE RATINGS (Do not exceed):

Power Supply Voltage	V_{EE} (ECL)	–8.0 to 0	Vdc
Power Supply Voltage	V_{CCT} (TTL)	–0.5 to +7.0	Vdc
Input Voltage	V_I (ECL) V_I (TTL)	0.0 to V_{EE} –0.5 to +7.0	Vdc
Disabled 3-State Output	V_{out} (TTL)	0.0 to V_{CCT}	Vdc
Output Source Current Continuous	I_{out} (ECL)	100	mAdc
Output Source Current Surge	I_{out} (ECL)	200	mAdc
Storage Temperature	T_{stg}	–65 to 150	°C
Operating Temperature	T_{amb}	0.0 to +75	°C

TTL DC CHARACTERISTICS: V_{CCT} = +5.0 V ±10%, V_{EE} = –5.2 ±5% (10H Version); V_{EE} = –4.2 V to –5.5 V (100H Version)

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Standard Input Standard Input	2.0 —	— 0.8	2.0 —	— 0.8	2.0 —	— 0.8	Vdc	
V_{IK}	Input Clamp	—	–1.2	—	–1.2	—	–1.2	Vdc	I_{IN} = –18 mA
V_{OH}	Output HIGH Voltage Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	I_{OH} = –3.0 mA I_{OH} = –15 mA
V_{OL}	Output LOW Voltage	—	0.55	—	0.55	—	0.55	V	I_{OL} = 48 mA
I_{IH}/I_{OZH} I_{IL}/I_{OZL}	Output Disable Current	— —	70 200	— —	70 200	— —	70 200	µA	V_{OUT} = 2.7 V V_{OUT} = 0.5 V
I_{CCL}	Supply Current	—	63	—	63	—	63	mA	
I_{CCH}	Supply Current	—	63	—	63	—	63	mA	
I_{CCZ}	Supply Current	—	63	—	63	—	63	mA	
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0 V

ECL TO TTL DIRECTION AC CHARACTERISTICS

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output	4.0	7.8	4.0	7.8	4.2	8.0	ns	C_L = 50 pF
t_{PLH} t_{PHL}	LEET to Output	5.5 5.5	8.3 7.6	5.5 5.5	8.3 7.6	5.7 5.8	8.5 8.0	ns	C_L = 50 pF
t_{PZH} t_{PZL}	CEB to Output Enable Time	5.5 5.3	8.3 8.3	5.5 5.3	8.3 8.3	4.7 5.4	8.5 8.4	ns	C_L = 50 pF
t_{PHZ} t_{PLZ}	CEB to Output Disable Time	3.5 3.5	7.2 5.3	3.5 3.5	7.2 5.3	3.7 4.1	7.3 5.8	ns	C_L = 50 pF
t_r/t_f	1.0 Vdc to 2.0 Vdc	0.4	2.2	0.4	2.2	0.4	2.2	ns	C_L = 50 pF

TTL TO ECL DIRECTION AC CHARACTERISTICS

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output	1.9	3.9	1.9	3.9	2.2	4.4	ns	50 Ω to –2.0 V
t_{PHL} t_{PLH}	CEB to Output	2.2 2.3	4.0 4.6	2.2 2.3	4.0 4.6	2.5 2.7	4.3 5.0	ns	50 Ω to –2.0 V
t_{PHL} t_{PLH}	LETE to Output	2.4	3.9	2.4	3.9	2.7	4.3	ns	50 Ω to –2.0 V
t_r/t_f	Output Rise/Fall Time 20%–80%	0.4	2.2	0.4	2.2	0.4	2.2	ns	50 Ω to –2.0 V

TEST CIRCUITS AND WAVEFORMS

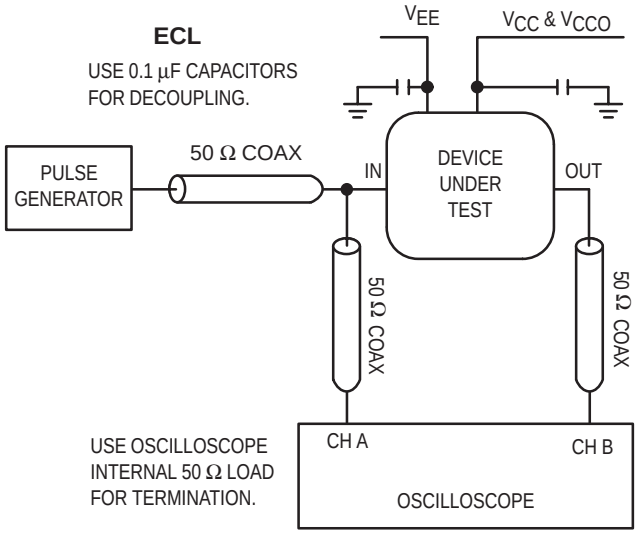


Figure 1. Test Circuit ECL

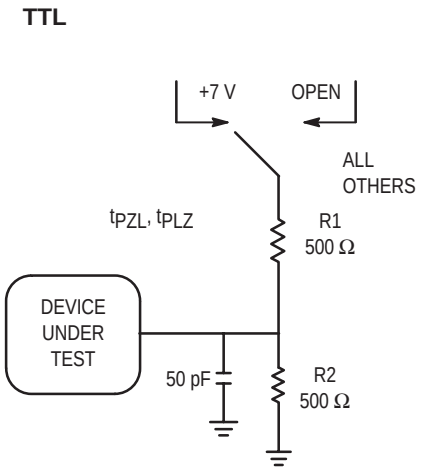


Figure 2. Test Circuit TTL

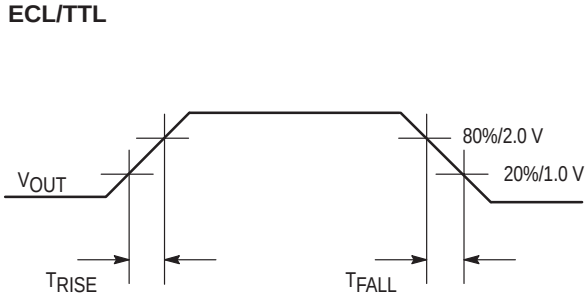


Figure 3. Rise and Fall Times

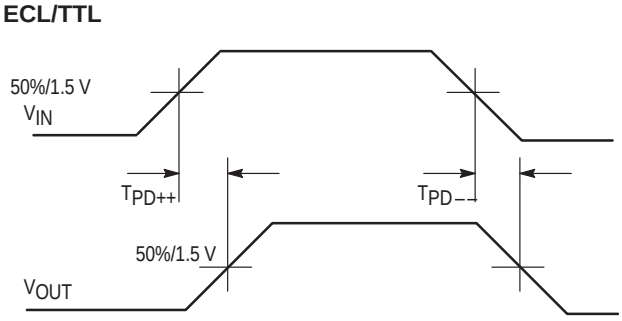


Figure 4. Propagation Delay — Single Ended

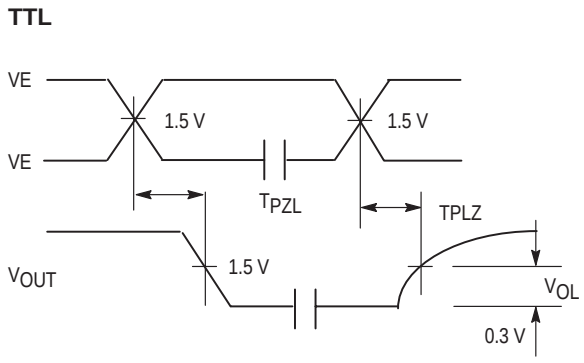


Figure 5. 3-State Output Low Enable and Disable Times

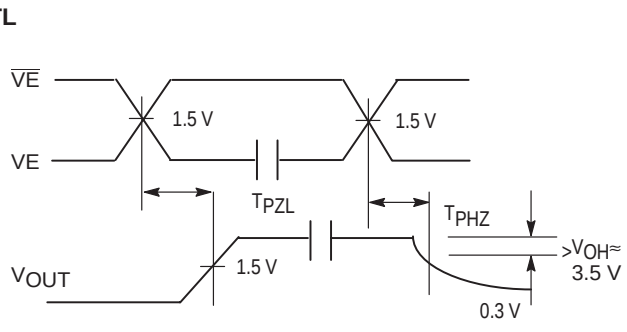


Figure 6. 3-State Output High Enable and Disable Times

CHAPTER 3
MECL 10K Data Sheets

MECL 10K
INTEGRATED CIRCUITS

MC10,100/10,200 Series

–30 to 85°C

Function Selection — (–30° to +85°C)

Function	Device	Case
NOR Gates		
Quad 2-Input Gate	MC10102	620, 648, 775
Triple 4-3-3 Input Gate	MC10106	620, 648, 775
Dual 3-Input 3-Output Gate	MC10111	620, 648
Dual 3-Input 3-Output Gate	MC10211	620, 648, 775
OR Gates		
Quad 2-Input Gate	MC10103	620, 648, 775
Dual 3-Input 3-Output Gate	MC10110	620, 648
Dual 3-Input 3-Output Gate	MC10210	620, 648, 775
AND Gates		
Quad 2-Input Gate	MC10104	620, 648, 775
Hex Gate	MC10197	620, 648, 775
Complex Gates		
Quad OR/NOR Gate	MC10101	620, 648, 775
Triple 2-3-2 Input OR/NOR Gate	MC10105	620, 648, 775
Dual 4-5 Input OR/NOR Gate	MC10109	620, 648, 775
Dual 3-Input 3-Output OR/NOR Gate	MC10212	648, 775
Triple 2-Input Exclusive OR/NOR Gate	MC10107	620, 648, 775
Quad 2-Input Exclusive OR/NOR Gate	MC10113	620, 648, 775
Dual 2-Wide 2-3 Input OR-AND/OR-AND INVERT	MC10117	620, 648, 775
4-Wide 3-Input OR-AND/OR-AND INVERT	MC10121	620, 648, 775
Buffers/Inverters		
Hex Buffer/Enable	MC10188	620, 648, 775
Hex Inverter/Enable	MC10189	620, 648, 775
Hex Inverter/Buffer	MC10195	620, 648, 775
Line Drivers/Line Receivers		
Triple Line Receiver	MC10114	620, 648, 775
Quad Line Receiver	MC10115	620, 648, 775
Triple Line Receiver	MC10116	620, 648, 775
Triple Bus Driver	MC10123	620, 648, 775
Quad Bus Receiver	MC10129	620
Quad Bus Driver	MC10192	620, 648, 775
Triple Line Receiver	MC10216	620, 648, 775
Translators		
Quad TTL-MECL	MC10124	620, 648, 775
Quad MECL-TTL	MC10125	620, 648, 775

Function	Device	Case
Flip-Flop/Latches		
Dual D Master Slave Flip-Flop	MC10131	620, 648, 775
Dual J-K Master Slave Flip-Flop	MC10135	620, 648, 775
Quad Latch	MC10153	620, 648, 775
Hex D Master Slave Flip-Flop	MC10176	620, 648, 775
Hex D Common Reset Flip-Flop	MC10186	620, 648, 775
Dual D Master Slave Flip-Flop	MC10231	620, 648, 775
Quad Latch	MC10133	620, 648
Quint Latch	MC10175	620, 648, 775
Quad/Common Clock Latch	MC10168	648
Encoders		
8-Input Encoder	MC10165	620, 648
Decoders		
Binary to 1-8 (Low)	MC10161	620, 648, 775
Binary to 1-8 (High)	MC10162	620, 648, 775
Dual Binary to 1-4 (Low)	MC10171	620, 648, 775
Dual Binary to 1-4 (High)	MC10172	620, 648, 775
Parity Generator/Checkers		
12-Bit Parity Generator-Checker	MC10160	620, 648
9 + 2 Bit Parity	MC10170	620, 648
Counters		
Hexadecimal	MC10136	620, 648, 775
Decade	MC10137	620, 648
Biquinary	MC10138	620, 648, 775
Binary Down Counter	MC10154	620, 648
Binary	MC10178	620, 648, 775
Arithmetic Functions		
5-Bit Magnitude Comparator	MC10166	620, 648, 775
4-Bit Arithmetic Function Gen.	MC10181	623
Shift Register		
4-Bit Universal	MC10141	620, 648, 775
Multivibrators		
Monostable Multivibrators	MC10198	620, 648, 775
Multiplexer		
Dual with Latch	MC10134	620, 648, 775
Quad 2-Input/Noninverting	MC10158	620, 648, 775
Quad 2-Input/Inverting	MC10159	620, 648, 775
8-Line	MC10164	620, 648, 775
Quad 2-Input/Latch	MC10173	620, 648, 775
Dual 4-1	MC10174	620, 648, 775

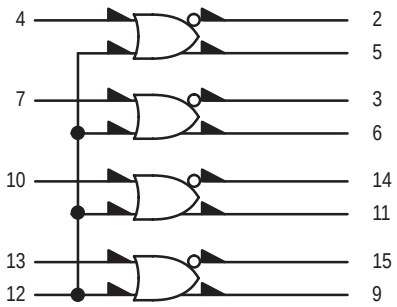
MC10101

Quad OR/NOR Gate

The MC10101 is a quad 2–input OR/NOR gate with one input from each gate common to pin 12.

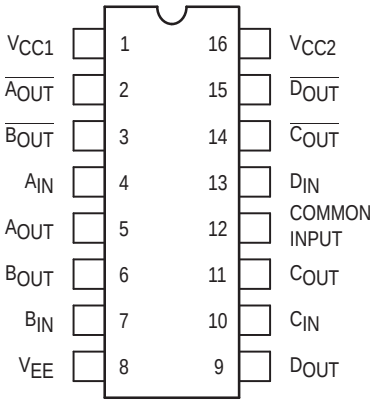
- P_D = 25 mW typ/gate (No Load)
- t_{pd} = 2.0 ns typ
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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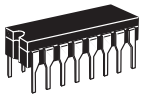
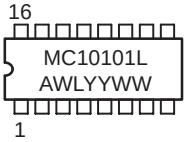
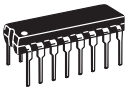
MARKING DIAGRAMS

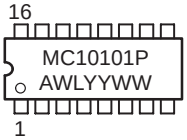


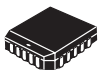
CDIP–16
L SUFFIX
CASE 620



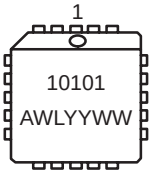


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10101L	CDIP–16	25 Units / Rail
MC10101P	PDIP–16	25 Units / Rail
MC10101FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		29		20	26		29	mAdc
Input Current	I_{inH}	4 12		425 850			265 535		265 535	μAdc
	I_{inL}	4 12	0.5 0.5		0.5 0.5			0.3 0.3		μAdc
Output Voltage Logic 1	V_{OH}	5 5 2 2	–1.060 –1.060 –1.060 –1.060	–0.890 –0.890 –0.890 –0.890	–0.960 –0.960 –0.960 –0.960		–0.810 –0.810 –0.810 –0.810	–0.890 –0.890 –0.890 –0.890	–0.700 –0.700 –0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	5 5 2 2	–1.890 –1.890 –1.890 –1.890	–1.675 –1.675 –1.675 –1.675	–1.850 –1.850 –1.850 –1.850		–1.650 –1.650 –1.650 –1.650	–1.825 –1.825 –1.825 –1.825	–1.615 –1.615 –1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	5 5 2 2	–1.080 –1.080 –1.080 –1.080		–0.980 –0.980 –0.980 –0.980			–0.910 –0.910 –0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	5 5 2 2		–1.655 –1.655 –1.655 –1.655			–1.630 –1.630 –1.630 –1.630		–1.595 –1.595 –1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{4+2-} t_{4-2+} t_{4+5+} t_{4-5-}	2 2 5 5	1.0 1.0 1.0 1.0	3.1 3.1 3.1 3.1	1.0 1.0 1.0 1.0	2.0 2.0 2.0 2.0	2.9 2.9 2.9 2.9	1.0 1.0 1.0 1.0	3.3 3.3 3.3 3.3	
Rise Time (20 to 80%)	t_{2+} t_{5+}	2 5	1.1 1.1	3.6 3.6	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.7 3.7	
Fall Time (20 to 80%)	t_{2-} t_{5-}	2 5	1.1 1.1	3.6 3.6	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.7 3.7	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8					8	1, 16
Input Current	I_{inH}	4	4				8	1, 16
		12	12				8	1, 16
	I_{inL}	4		4			8	1, 16
		12		12			8	1, 16
Output Voltage Logic 1	V_{OH}	5	12				8	1, 16
		5	4				8	1, 16
		2					8	1, 16
		2					8	1, 16
Output Voltage Logic 0	V_{OL}	5					8	1, 16
		5					8	1, 16
		2	12				8	1, 16
		2	4				8	1, 16
Threshold Voltage Logic 1	V_{OHA}	5			12		8	1, 16
		5			4		8	1, 16
		2				12	8	1, 16
		2				4	8	1, 16
Threshold Voltage Logic 0	V_{OLA}	5				12	8	1, 16
		5				4	8	1, 16
		2			12		8	1, 16
		2			4		8	1, 16
Switching Times (50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	t_{4+2-}	2			4	2	8	1, 16
	t_{4-2+}	2			4	2	8	1, 16
	t_{4+5+}	5			4	5	8	1, 16
	t_{4-5-}	5			4	5	8	1, 16
Rise Time (20 to 80%)	t_{2+}	2			4	2	8	1, 16
	t_{5+}	5			4	5	8	1, 16
Fall Time (20 to 80%)	t_{2-}	2			4	2	8	1, 16
	t_{5-}	5			4	5	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

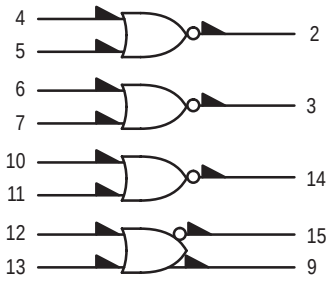
MC10102

Quad 2-Input NOR Gate

The MC10102 is a quad 2–input NOR gate. The MC10102 provides one gate with OR/NOR outputs.

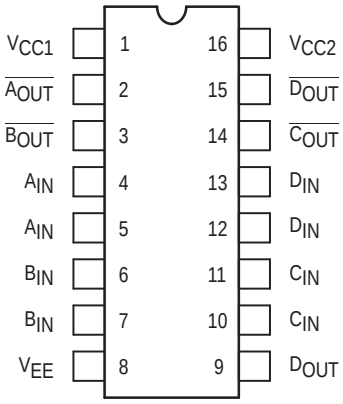
- P_D = 25 mW typ/gate (No Load)
- t_{pd} = 2.0 ns typ
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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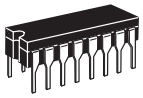
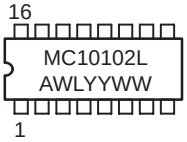
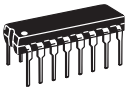
MARKING DIAGRAMS

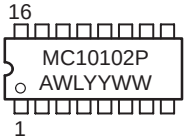


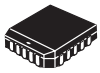
CDIP–16
L SUFFIX
CASE 620



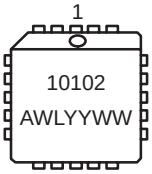


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10102L	CDIP–16	25 Units / Rail
MC10102P	PDIP–16	25 Units / Rail
MC10102FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		29		20	26		29	mAdc
Input Current	I_{inH}	12		425			265		265	μAdc
	I_{inL}	12	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	9 9 15 15	–1.060 –1.060 –1.060 –1.060	–0.890 –0.890 –0.890 –0.890	–0.960 –0.960 –0.960 –0.960		–0.810 –0.810 –0.810 –0.810	–0.890 –0.890 –0.890 –0.890	–0.700 –0.700 –0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	9 9 15 15	–1.890 –1.890 –1.890 –1.890	–1.675 –1.675 –1.675 –1.675	–1.850 –1.850 –1.850 –1.850		–1.650 –1.650 –1.650 –1.650	–1.825 –1.825 –1.825 –1.825	–1.615 –1.615 –1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	9 9 15 15	–1.080 –1.080 –1.080 –1.080		–0.980 –0.980 –0.980 –0.980			–0.910 –0.910 –0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	9 9 15 15		–1.655 –1.655 –1.655 –1.655			–1.630 –1.630 –1.630 –1.630		–1.595 –1.595 –1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{12+15-} t_{12-15+} t_{12+9+} t_{12-9-}	15 15 9 9	1.0 1.0 1.0 1.0	3.1 3.1 3.1 3.1	1.0 1.0 1.0 1.0	2.0 2.0 2.0 2.0	2.9 2.9 2.9 2.9	1.0 1.0 1.0 1.0	3.3 3.3 3.3 3.3	
Rise Time (20 to 80%)	t_{15+} t_{9+}	15 9	1.1 1.1	3.6 3.6	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.7 3.7	
Fall Time (20 to 80%)	t_{15-} t_{9-}	15 9	1.1 1.1	3.6 3.6	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.7 3.7	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
	TEST VOLTAGE VALUES (Volts)				
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	12	12				8	1, 16
		I_{inL}	12		12			8	1, 16
Output Voltage	Logic 1	V_{OH}	9	12				8	1, 16
			9	13				8	1, 16
			15					8	1, 16
			15					8	1, 16
Output Voltage	Logic 0	V_{OL}	9					8	1, 16
			9					8	1, 16
			15	12				8	1, 16
			15	13				8	1, 16
Threshold Voltage	Logic 1	V_{OHA}	9			12		8	1, 16
			9			13		8	1, 16
			15				12	8	1, 16
			15				13	8	1, 16
Threshold Voltage	Logic 0	V_{OLA}	9				12	8	1, 16
			9				13	8	1, 16
			15			12		8	1, 16
			15			13		8	1, 16
Switching Times	(50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay		t_{12+15-}	15			12	15	8	1, 16
		t_{12-15+}	15			12	15	8	1, 16
		t_{12+9+}	9			12	9	8	1, 16
		t_{12-9-}	9			12	9	8	1, 16
Rise Time	(20 to 80%)	t_{15+}	15			12	15	8	1, 16
		t_{9+}	9			12	9	8	1, 16
Fall Time	(20 to 80%)	t_{15-}	15			12	15	8	1, 16
		t_{9-}	9			12	9	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

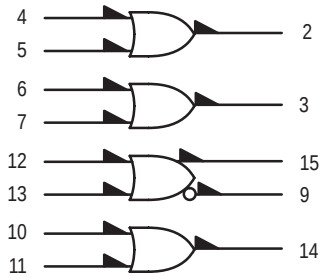
MC10103

Quad 2-Input OR Gate

The MC10103 is a quad 2–input OR gate. The MC10103 provides one gate with OR/NOR outputs.

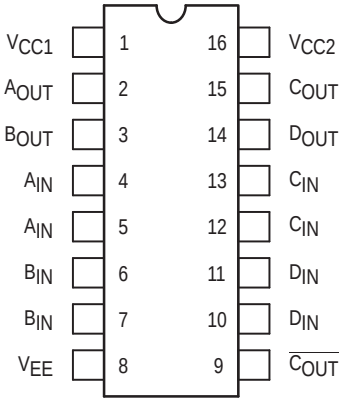
- P_D = 25 mW typ/gate (No Load)
- t_{pd} = 2.0 ns typ
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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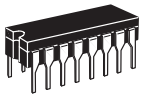
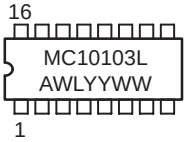
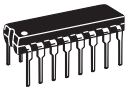
MARKING DIAGRAMS

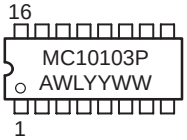


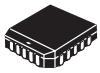
CDIP–16
L SUFFIX
CASE 620



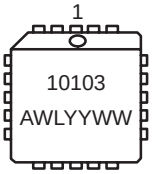


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10103L	CDIP–16	25 Units / Rail
MC10103P	PDIP–16	25 Units / Rail
MC10103FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		29		21	26		29	mAdc
Input Current	I_{inH}	4*		390			245		245	μAdc
	I_{inL}	4*	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	2 9	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 9	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 9	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 9		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{4+2+} t_{12+9-}	2 9	1.0 1.0	3.1 3.1	1.0 1.0	2.0 2.0	2.9 2.9	1.0 1.0	3.3 3.3	
Rise Time (20 to 80%)	t_{2+}	2	1.1	3.6	1.1	2.0	3.3	1.1	3.7	
Fall Time (20 to 80%)	t_{2-}	2	1.1	3.6	1.1	2.0	3.3	1.1	3.7	

* Individually test each input applying V_{IH} or V_{IL} to input under test.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C			–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C			–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C			–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					**(V_{CC}) Gnd**
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	4*	4*				8	1, 16
		I_{inL}	4*		4*			8	1, 16
Output Voltage	Logic 1	V_{OH}	2 9	4.5				8 8	1, 16 1, 16
Output Voltage	Logic 0	V_{OL}	2 9	 12, 13				8 8	1, 16 1, 16
Threshold Voltage	Logic 1	V_{OHA}	2 9			4, 5	 12, 13	8 8	1, 16 1, 16
Threshold Voltage	Logic 0	V_{OLA}	2 9			 12, 13	4, 5	8 8	1, 16 1, 16
Switching Times	(50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay		t_{4+2+} t_{12+9-}	2 9			4 12	2 9	8 8	1, 16 1, 16
Rise Time	(20 to 80%)	t_{2+}	2			4	2	8	1, 16
Fall Time	(20 to 80%)	t_{2-}	2			4	2	8	1, 16

* Individually test each input applying V_{IH} or V_{IL} to input under test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

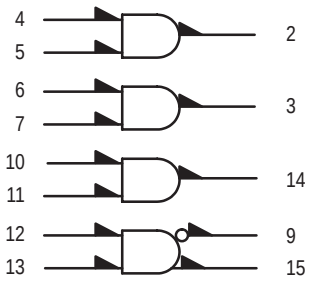
MC10104

Quad 2-Input AND Gate

The MC10104 is a quad 2–input AND gate. One of the gates has both AND/NAND outputs available.

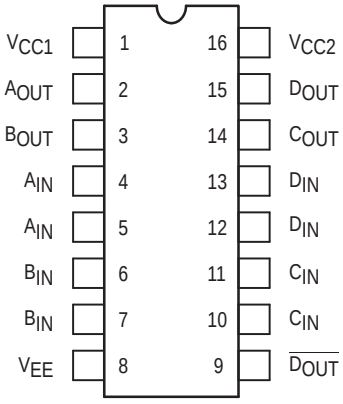
- P_D = 35 mW typ/gate (No Load)
- t_{pd} = 2.7 ns typ
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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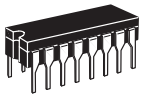
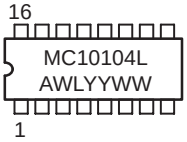
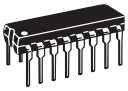
MARKING DIAGRAMS

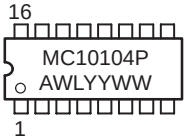


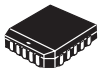
CDIP–16
L SUFFIX
CASE 620



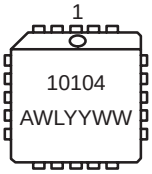


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10104L	CDIP–16	25 Units / Rail
MC10104P	PDIP–16	25 Units / Rail
MC10104FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		39			35		39	mAdc
Input Current	I_{inH}*	12 13		425 350			265 220		265 220	μAdc
	I_{inL}	12	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	15 9	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	15 9	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	9 9 15 15	–1.090 –1.090 –1.090 –1.090		–0.980 –0.980 –0.980 –0.980			–0.910 –0.910 –0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	9 9 15 15		–1.655 –1.655 –1.655 –1.655			–1.630 –1.630 –1.630 –1.630		–1.595 –1.595 –1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{12+15+} t_{12-15-} t_{12+9-} t_{12-9+}	15 15 9 9	1.0 1.0 1.0 1.0	4.3 4.3 4.3 4.3	1.0 1.0 1.0 1.0	2.2 2.2 2.2 2.2	4.0 4.0 4.0 4.0	1.0 1.0 1.0 1.0	4.2 4.2 4.2 4.2	
	t_{13+15+} t_{13+9-}	15 9	1.0 1.0	4.3 4.3	1.0 1.0	2.7 2.7	4.0 4.0	1.0 1.0	4.2 4.2	
Rise Time (20 to 80%)	t_{15+} t_{9+}	15 9	1.5 1.5	3.7 3.7	1.5 1.5	2.0 2.0	3.5 3.5	1.5 1.5	3.6 3.6	
Fall Time (20 to 80%)	t_{15-} t_{9-}	15 9	1.5 1.5	3.7 3.7	1.5 1.5	2.0 2.0	3.5 3.5	1.5 1.5	3.6 3.6	

* Inputs 4, 7, 10 and 13 will behave similarly for ac and I_{inH} values.
Inputs 5, 6, 11 and 12 will behave similarly for ac and I_{inH} values.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

TEST VOLTAGE VALUES (Volts)

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8					8	1, 16
Input Current	I_{inH}*	12 13	12, 13 13				8 8	1, 16 1, 16
	I_{inL}	12		12			8	1, 16
Output Voltage Logic 1	V_{OH}	15 9	12, 13				8 8	1, 16 1, 16
Output Voltage Logic 0	V_{OL}	15 9	 12, 13				8 8	1, 16 1, 16
Threshold Voltage Logic 1	V_{OHA}	9 9 15 15	 12 13		 13 12	12 13 	8 8 8 8	1, 16 1, 16 1, 16 1, 16
Threshold Voltage Logic 0	V_{OLA}	9 9 15 15	12 13 		13 12 	 12 13	8 8 8 8	1, 16 1, 16 1, 16 1, 16
Switching Times (50Ω Load)			**+1.11V**		**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	t_{12+15+} $t_{12–15–}$ $t_{12+9–}$ $t_{12–9+}$	15 15 9 9	13 13 13 13		12 12 12 12	15 15 9 9	8 8 8 8	1, 16 1, 16 1, 16 1, 16
	t_{13+15+} $t_{13+9–}$	15 9	12 12		13 13	15 9	8 8	1, 16 1, 16
Rise Time (20 to 80%)	t_{15+} t_{9+}	15 9	12 12		13 13	15 9	8 8	1, 16 1, 16
Fall Time (20 to 80%)	$t_{15–}$ $t_{9–}$	15 9	12 12		13 13	15 9	8 8	1, 16 1, 16

* Inputs 4, 7, 10 and 13 will behave similarly for ac and I_{inH} values.
Inputs 5, 6, 11 and 12 will behave similarly for ac and I_{inH} values.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

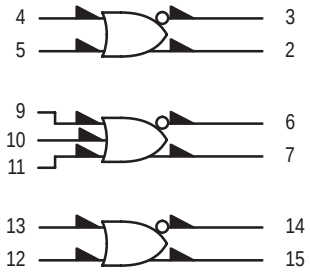
MC10105

Triple 2-3-2-Input OR/NOR Gate

The MC10105 is a triple 2–3–2 input OR/NOR gate.

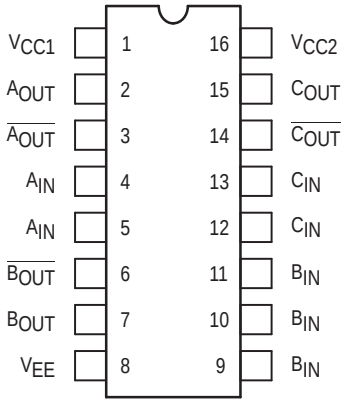
- P_D = 30 mW typ/gate (No Load)
- t_{pd} = 2.0 ns typ
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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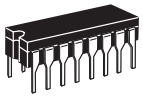
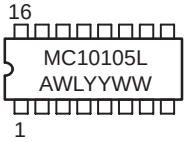
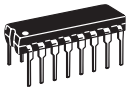
MARKING DIAGRAMS

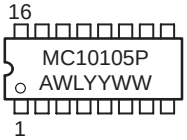


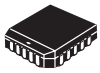
CDIP–16
L SUFFIX
CASE 620



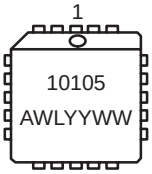


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10105L	CDIP–16	25 Units / Rail
MC10105P	PDIP–16	25 Units / Rail
MC10105FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		23		17	21		23	mAdc
Input Current	I_{inH}	4		425			265		265	μAdc
	I_{inL}	4	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	3 2	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	3 2	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	3 2	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	3 2		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{4+3-} t_{4-3+} t_{4+2+} t_{4-2-}	3 3 2 2	1.0 1.0 1.0 1.0	3.1 3.1 3.1 3.1	1.0 1.0 1.0 1.0	2.0 2.0 2.0 2.0	2.9 2.9 2.9 2.9	1.0 1.0 1.0 1.0	3.3 3.3 3.3 3.3	
Rise Time (20 to 80%)	t_{3+} t_{2+}	3 2	1.1 1.1	3.6 3.6	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.7 3.7	
Fall Time (20 to 80%)	t_{3-} t_{2-}	3 2	1.1 1.1	3.6 3.6	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.7 3.7	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C			–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C			–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C			–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					**(V_{CC}) Gnd**
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	4	4				8	1, 16
		I_{inL}	4		4			8	1, 16
Output Voltage	Logic 1	V_{OH}	3 2	 4				8 8	1, 16 1, 16
Output Voltage	Logic 0	V_{OL}	3 2	4				8 8	1, 16 1, 16
Threshold Voltage	Logic 1	V_{OHA}	3 2			 4	4	8 8	1, 16 1, 16
Threshold Voltage	Logic 0	V_{OLA}	3 2			4	 4	8 8	1, 16 1, 16
Switching Times	(50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay		t_{4+3-}	3			4	3	8	1, 16
		t_{4-3+}	3			4	3	8	1, 16
		t_{4+2+}	2			4	2	8	1, 16
		t_{4-2-}	2			4	2	8	1, 16
Rise Time	(20 to 80%)	t_{3+}	3			4	3	8	1, 16
		t_{2+}	2			4	2	8	1, 16
Fall Time	(20 to 80%)	t_{3-}	3			4	3	8	1, 16
		t_{2-}	2			4	2	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

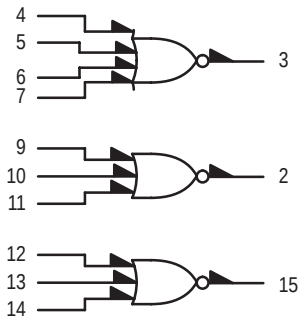
MC10106

Triple 4-3-3-Input NOR Gate

The MC10106 is a triple 4–3–3 input NOR gate.

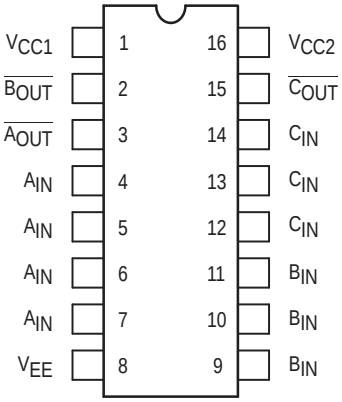
- P_D = 30 mW typ/gate (No Load)
- t_{pd} = 2.0 ns typ
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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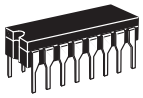
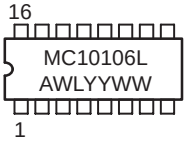
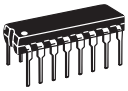
MARKING DIAGRAMS

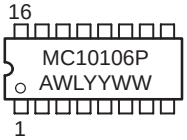


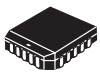
CDIP–16
L SUFFIX
CASE 620



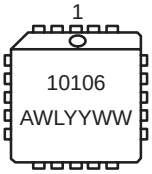


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10106L	CDIP–16	25 Units / Rail
MC10106P	PDIP–16	25 Units / Rail
MC10106FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		23		17	21		23	mAdc
Input Current	I_{inH}	4		425			265		265	μAdc
	I_{inL}	4	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	3 2	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	3 2	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	3 2	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	3 2		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{4+3-} t_{4-3+}	3 3	1.0 1.0	3.1 3.1	1.0 1.0	2.0 2.0	2.9 2.9	1.0 1.0	3.3 3.3	
Rise Time (20 to 80%)	t_{3+}	3	1.1	3.6	1.1	2.0	3.3	1.1	3.7	
Fall Time (20 to 80%)	t_{3-}	3	1.1	3.6	1.1	2.0	3.3	1.1	3.7	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts)					
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8					8	1, 16
Input Current	I_{inH}	4	4				8	1, 16
	I_{inL}	4		4			8	1, 16
Output Voltage Logic 1	V_{OH}	3 2					8 8	1, 16 1, 16
Output Voltage Logic 0	V_{OL}	3 2	4 9				8 8	1, 16 1, 16
Threshold Voltage Logic 1	V_{OHA}	3 2				4 9	8 8	1, 16 1, 16
Threshold Voltage Logic 0	V_{OLA}	3 2			4 9		8 8	1, 16 1, 16
Switching Times (50Ω Load)					Pulse In	Pulse Out	–3.2 V	+2.0 V
Propagation Delay	t_{4+3-} t_{4-3+}	3 3			4 4	3 3	8 8	1, 16 1, 16
Rise Time (20 to 80%)	t_{3+}	3			4	3	8	1, 16
Fall Time (20 to 80%)	t_{3-}	3			4	3	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

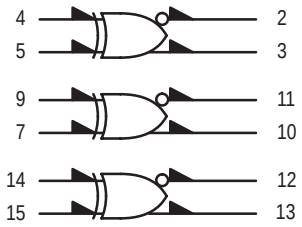
MC10107

Triple 2-Input Exclusive OR/ Exclusive NOR Gate

The MC10107 is a triple–2 input exclusive OR/NOR gate.

- P_D = 40 mW typ/gate (No Load)
- t_{pd} = 2.8 ns typ
- t_r, t_f = 2.5 ns typ (20%–80%)

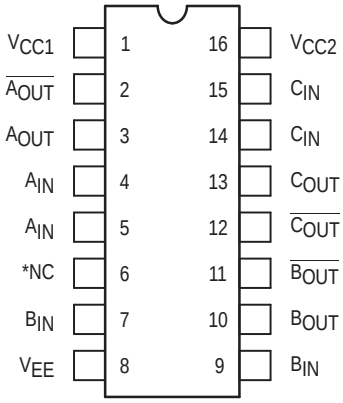
LOGIC DIAGRAM



$3 = (4 \bullet \overline{5}) + (\overline{4} \bullet 5)$
$2 = (\overline{4} \bullet \overline{5}) + (4 \bullet 5)$

V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



***NC = No Connection**

Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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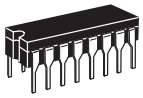
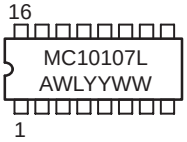
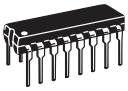
MARKING DIAGRAMS

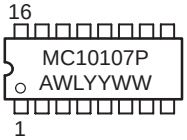


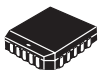
CDIP–16
L SUFFIX
CASE 620



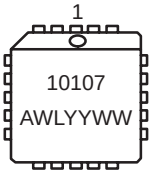


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10107L	CDIP–16	25 Units / Rail
MC10107P	PDIP–16	25 Units / Rail
MC10107FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		31			28		31	mAdc
Input Current	I_{inH}	4, 9, 14 5, 7, 15		425 350			265 220		265 220	µAdc
	I_{inL}	*	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	2 2 3 3	–1.060 –1.060 –1.060 –1.060	–0.890 –0.890 –0.890 –0.890	–0.960 –0.960 –0.960 –0.960		–0.810 –0.810 –0.810 –0.810	–0.890 –0.890 –0.890 –0.890	–0.700 –0.700 –0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 2 3 3	–1.890 –1.890 –1.890 –1.890	–1.675 –1.675 –1.675 –1.675	–1.850 –1.850 –1.850 –1.850		–1.650 –1.650 –1.650 –1.650	–1.825 –1.825 –1.825 –1.825	–1.615 –1.615 –1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 2 3 3	–1.080 –1.080 –1.080 –1.080		–0.980 –0.980 –0.980 –0.980			–0.910 –0.910 –0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 2 3 3		–1.655 –1.655 –1.655 –1.655			–1.630 –1.630 –1.630 –1.630		–1.595 –1.595 –1.595 –1.595	Vdc
Switching Times (50Ω Load)					Min	Typ	Max			ns
Propagation Delay	t++ t+ – t–+ t– –	Inputs 4,9 or 14 to either Output	–1.1 1.1 1.1 1.1	3.8 3.8 3.8 3.8	1.1 1.1 1.1 1.1	2.0 2.0 2.0 2.0	3.7 3.7 3.7 3.7	1.1 1.1 1.1 1.1	4.0 4.0 4.0 4.0	
	t++ t+ – t–+ t– –	Inputs 5,7 or 15 to either Output	1.1 1.1 1.1 1.1	3.8 3.8 3.8 3.8	1.1 1.1 1.1 1.1	2.8 2.8 2.8 2.8	3.7 3.7 3.7 3.7	1.1 1.1 1.1 1.1	4.0 4.0 4.0 4.0	
Rise Time (20 to 80%)	t+	**	1.1	3.5	1.1	2.5	3.5	1.1	3.8	
Fall Time (20 to 80%)	t–	**	1.1	3.5	1.1	2.5	3.5	1.1	3.8	

* Individually test each input applying V_{IH} or V_{IL} to input under test.

** Any Output.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
	TEST VOLTAGE VALUES (Volts)				
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8	5, 7, 15				8	1, 16
Input Current	I_{inH}	4, 9, 14	*				8	1, 16
		5, 7, 15	*				8	1, 16
	I_{inL}	*		*			8	1, 16
Output Voltage Logic 1	V_{OH}	2	4, 5				8	1, 16
		2					8	1, 16
		3	4				8	1, 16
		3	5				8	1, 16
Output Voltage Logic 0	V_{OL}	2	4				8	1, 16
		2	5				8	1, 16
		3	4, 5				8	1, 16
		3					8	1, 16
Threshold Voltage Logic 1	V_{OHA}	2	5		4		8	1, 16
		2				4	8	1, 16
		3			4		8	1, 16
		3			5		8	1, 16
Threshold Voltage Logic 0	V_{OLA}	2			4		8	1, 16
		2			5		8	1, 16
		3	5		4		8	1, 16
		3				4	8	1, 16
Switching Times (50Ω Load)			**+1.1V**		**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	t++	Inputs	5, 7, 15		Input 4, 9 or 14	Corresponding XOR/XNOR Outputs	8	1, 16
	t+ –	4,9 or 14	5, 7, 15				8	1, 16
	t–+	to either	5, 7, 15				8	1, 16
	t– –	Output	5, 7, 15				8	1, 16
	t++	Inputs	4, 9, 14		Input 5, 7 or 15	Corresponding XOR/XNOR Outputs	8	1, 16
	t+ –	5,7 or 15	4, 9, 14				8	1, 16
	t–+	to either	4, 9, 14				8	1, 16
	t– –	Output	4, 9, 14				8	1, 16
Rise Time (20 to 80%)	t+	**	4, 9, 14		Any Input	Corresponding XOR/XNOR Outputs	8	1, 16
Fall Time (20 to 80%)	t–	**	4, 9, 14		Any Input		8	1, 16

* Individually test each input applying V_{IH} or V_{IL} to input under test.

** Any Output.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

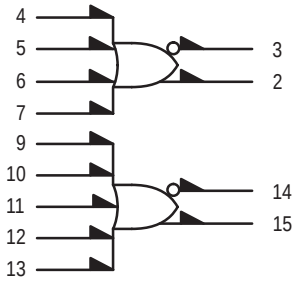
MC10109

Dual 4-5-Input OR/NOR Gate

The MC10109 is a dual 4–5 input OR/NOR gate.

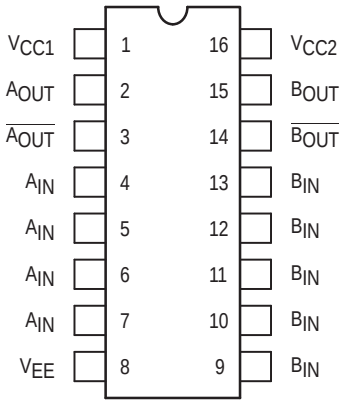
- P_D = 30 mW typ/gate (No Load)
- t_{pd} = 2.0 ns typ
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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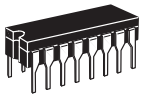
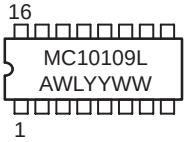
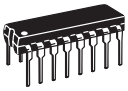
MARKING DIAGRAMS

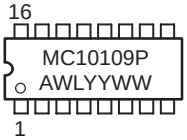


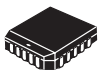
CDIP–16
L SUFFIX
CASE 620



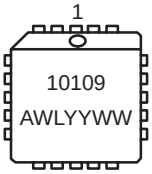


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10109L	CDIP–16	25 Units / Rail
MC10109P	PDIP–16	25 Units / Rail
MC10109FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		15		11	14		15	mAdc
Input Current	I_{inH}	4		425			265		265	μAdc
	I_{inL}	4	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	2 3	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{4+2+} t_{4-2-} t_{4+3-} t_{4-3+}	2 2 3 3	1.0 1.0 1.0 1.0	3.7 3.7 3.7 3.7	1.0 1.0 1.0 1.0	2.0 2.0 2.0 2.0	2.9 2.9 2.9 2.9	1.0 1.0 1.0 1.0	3.7 3.7 3.7 3.7	
Rise Time (20 to 80%)	t_{2+} t_{3+}	2 3	1.1 1.1	4.0 4.0	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	4.0 4.0	
Fall Time (20 to 80%)	t_{2-} t_{3-}	2 3	1.1 1.1	4.0 4.0	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	4.0 4.0	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C			–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C			–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C			–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					**(V_{CC}) Gnd**
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	4	4				8	1, 16
		I_{inL}	4		4			8	1, 16
Output Voltage	Logic 1	V_{OH}	2 3	4				8 8	1, 16 1, 16
Output Voltage	Logic 0	V_{OL}	2 3	 4				8 8	1, 16 1, 16
Threshold Voltage	Logic 1	V_{OHA}	2 3			4	 4	8 8	1, 16 1, 16
Threshold Voltage	Logic 0	V_{OLA}	2 3			 4	4 	8 8	1, 16 1, 16
Switching Times	(50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay		t_{4+2+} t_{4-2-} t_{4+3-} t_{4-3+}	2 2 3 3			4 4 4 4	2 2 3 3	8 8 8 8	1, 16 1, 16 1, 16 1, 16
Rise Time	(20 to 80%)	t_{2+} t_{3+}	2 3			4 4	2 3	8 8	1, 16 1, 16
Fall Time	(20 to 80%)	t_{2-} t_{3-}	2 3			4 4	2 3	8 8	1, 16 1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

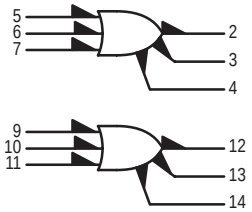
MC10110

Dual 3-Input/3-Ouput OR Gate

The ability to control three parallel lines from a single point makes the MC10110 particularly useful in clock distribution applications where minimum clock skew is desired. Three V_{CC} pins are provided and each one should be used.

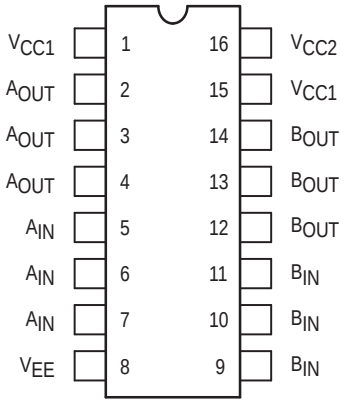
- P_D = 80 mW typ/pkg (No Load)
- t_{pd} = 2.4 ns typ (All Outputs Loaded)
- t_r, t_f = 2.2 ns typ (20%–80%)

LOGIC DIAGRAM



V_{CC1} = PIN 1, 15
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP
PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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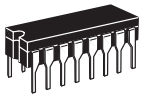
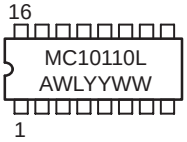
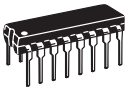
MARKING DIAGRAMS

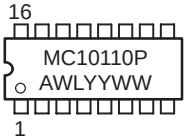


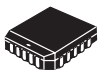
CDIP–16
L SUFFIX
CASE 620



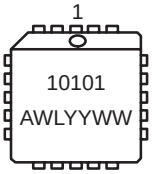


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10110L	CDIP–16	25 Units / Rail
MC10110P	PDIP–16	25 Units / Rail
MC10110FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		42		30	38		42	mAdc
Input Current	I_{inH}	5, 6, 7		680			425		425	μAdc
	I_{inL}	5, 6, 7	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	2 3 4	–1.060 –1.060 –1.060	–0.890 –0.890 –0.890	–0.960 –0.960 –0.960		–0.810 –0.810 –0.810	–0.890 –0.890 –0.890	–0.700 –0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3 4	–1.890 –1.890 –1.890	–1.675 –1.675 –1.675	–1.850 –1.850 –1.850		–1.650 –1.650 –1.650	–1.825 –1.825 –1.825	–1.615 –1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3 4	–1.080 –1.080 –1.080		–0.980 –0.980 –0.980			–0.910 –0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3 4		–1.655 –1.655 –1.655			–1.630 –1.630 –1.630		–1.595 –1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{5+2+} t_{5-2-} t_{5+3+} t_{5-3-} t_{5+4+} t_{5-4-}	2 2 3 3 4 4	1.4 1.4 1.4 1.4 1.4 1.4	3.5 3.5 3.5 3.5 3.5 3.5	1.4 1.4 1.4 1.4 1.4 1.4	2.4 2.4 2.4 2.4 2.4 2.4	3.5 3.5 3.5 3.5 3.5 3.5	1.5 1.5 1.5 1.5 1.5 1.5	3.8 3.8 3.8 3.8 3.8 3.8	
Rise Time (20 to 80%)	t_{2+} t_{3+} t_{4+}	2 3 4	1.0 1.0 1.0	3.5 3.5 3.5	1.1 1.1 1.1	2.2 2.2 2.2	3.5 3.5 3.5	1.2 1.2 1.2	3.8 3.8 3.8	
Fall Time (20 to 80%)	t_{2-} t_{3-} t_{4-}	2 3 4	1.0 1.0 1.0	3.5 3.5 3.5	1.1 1.1 1.1	2.2 2.2 2.2	3.5 3.5 3.5	1.2 1.2 1.2	3.8 3.8 3.8	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

TEST VOLTAGE VALUES (Volts)

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8					8	1, 15, 16
Input Current	I_{inH}	5, 6, 7	*				8	1, 15, 16
	I_{inL}	5, 6, 7		*			8	1, 15, 16
Output Voltage Logic 1	V_{OH}	2 3 4	5 6 7				8 8 8	1, 15, 16 1, 15, 16 1, 15, 16
Output Voltage Logic 0	V_{OL}	2 3 4					8 8 8	1, 15, 16 1, 15, 16 1, 15, 16
Threshold Voltage Logic 1	V_{OHA}	2 3 4			5 6 7		8 8 8	1, 15, 16 1, 15, 16 1, 15, 16
Threshold Voltage Logic 0	V_{OLA}	2 3 4				5 6 7	8 8 8	1, 15, 16 1, 15, 16 1, 15, 16
Switching Times (50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	t_{5+2+} t_{5-2-} t_{5+3+} t_{5-3-} t_{5+4+} t_{5-4-}	2 2 3 3 4 4			5 5 5 5 5 5	2 2 3 3 4 4	8 8 8 8 8 8	1, 15, 16 1, 15, 16 1, 15, 16 1, 15, 16 1, 15, 16 1, 15, 16
Rise Time (20 to 80%)	t_{2+} t_{3+} t_{4+}	2 3 4			5 5 5	2 3 4	8 8 8	1, 15, 16 1, 15, 16 1, 15, 16
Fall Time (20 to 80%)	t_{2-} t_{3-} t_{4-}	2 3 4			5 5 5	2 3 4	8 8 8	1, 15, 16 1, 15, 16 1, 15, 16

* Individually test each input using the pin connections shown.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10111

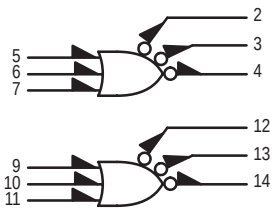
Dual 3-Input/3-Ouput NOR Gate

The MC10111 is designed to drive up to three transmission lines simul– taneously. The multiple outputs of this device also allow the wire "OR"–ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines from a single point makes the MC10111 particularly useful in clock distribution applications where minimum clock skew is desired. Three V_{CC} pins are provided and each one should be used.

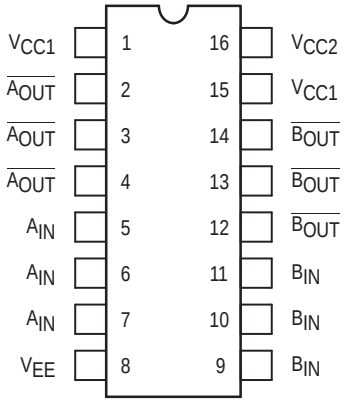
- P_D = 80 mW typ/gate (No Load)
- t_{pd} = 2.4 ns typ (All Outputs Loaded)
- t_r, t_f = 2.2 ns typ (20%–80%)

LOGIC DIAGRAM



V_{CC1} = PIN 1,15
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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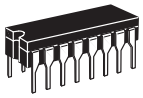
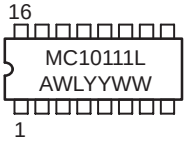
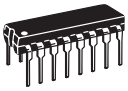
MARKING DIAGRAMS

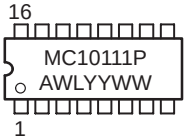


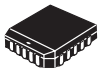
CDIP–16
L SUFFIX
CASE 620



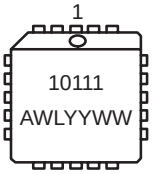


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10111L	CDIP–16	25 Units / Rail
MC10111P	PDIP–16	25 Units / Rail
MC10111FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		42		30	38		42	mAdc
Input Current	I_{inH}	5, 6, 7		680			425		425	μAdc
	I_{inL}	5, 6, 7	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	2 3 4	–1.060 –1.060 –1.060	–0.890 –0.890 –0.890	–0.960 –0.960 –0.960		–0.810 –0.810 –0.810	–0.890 –0.890 –0.890	–0.700 –0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3 4	–1.890 –1.890 –1.890	–1.675 –1.675 –1.675	–1.850 –1.850 –1.850		–1.650 –1.650 –1.650	–1.825 –1.825 –1.825	–1.615 –1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3 4	–1.080 –1.080 –1.080		–0.980 –0.980 –0.980			–0.910 –0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3 4		–1.655 –1.655 –1.655			–1.630 –1.630 –1.630		–1.595 –1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{5+2-} t_{5-2+} t_{5+3-} t_{5-3+} t_{5+4-} t_{5-4+}	2 2 3 3 4 4	1.4 1.4 1.4 1.4 1.4 1.4	3.5 3.5 3.5 3.5 3.5 3.5	1.4 1.4 1.4 1.4 1.4 1.4	2.4 2.4 2.4 2.4 2.4 2.4	3.5 3.5 3.5 3.5 3.5 3.5	1.5 1.5 1.5 1.5 1.5 1.5	3.8 3.8 3.8 3.8 3.8 3.8	
Rise Time (20 to 80%)	t_{2+} t_{3+} t_{4+}	2 3 4	1.0 1.0 1.0	3.5 3.5 3.5	1.1 1.1 1.1	2.2 2.2 2.2	3.5 3.5 3.5	1.2 1.2 1.2	3.8 3.8 3.8	
Fall Time (20 to 80%)	t_{2-} t_{3-} t_{4-}	2 3 4	1.0 1.0 1.0	3.5 3.5 3.5	1.1 1.1 1.1	2.2 2.2 2.2	3.5 3.5 3.5	1.2 1.2 1.2	3.8 3.8 3.8	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

TEST VOLTAGE VALUES (Volts)

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8					8	1, 15, 16
Input Current	I_{inH}	5, 6, 7	*				8	1, 15, 16
	I_{inL}	5, 6, 7		*			8	1, 15, 16
Output Voltage Logic 1	V_{OH}	2					8	1, 15, 16
		3					8	1, 15, 16
		4					8	1, 15, 16
Output Voltage Logic 0	V_{OL}	2	5				8	1, 15, 16
		3	6				8	1, 15, 16
		4	7				8	1, 15, 16
Threshold Voltage Logic 1	V_{OHA}	2				5	8	1, 15, 16
		3				6	8	1, 15, 16
		4				7	8	1, 15, 16
Threshold Voltage Logic 0	V_{OLA}	2			5		8	1, 15, 16
		3			6		8	1, 15, 16
		4			7		8	1, 15, 16
Switching Times (50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	t_{5+2-}	2			5	2	8	1, 15, 16
	t_{5-2+}	2			5	2	8	1, 15, 16
	t_{5+3-}	3			5	3	8	1, 15, 16
	t_{5-3+}	3			5	3	8	1, 15, 16
	t_{5+4-}	4			5	4	8	1, 15, 16
	t_{5-4+}	4			5	4	8	1, 15, 16
Rise Time (20 to 80%)	t_{2+}	2			5	2	8	1, 15, 16
	t_{3+}	3			5	3	8	1, 15, 16
	t_{4+}	4			5	4	8	1, 15, 16
Fall Time (20 to 80%)	t_{2-}	2			5	2	8	1, 15, 16
	t_{3-}	3			5	3	8	1, 15, 16
	t_{4-}	4			5	4	8	1, 15, 16

* Individually test each input using the pin connections shown.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

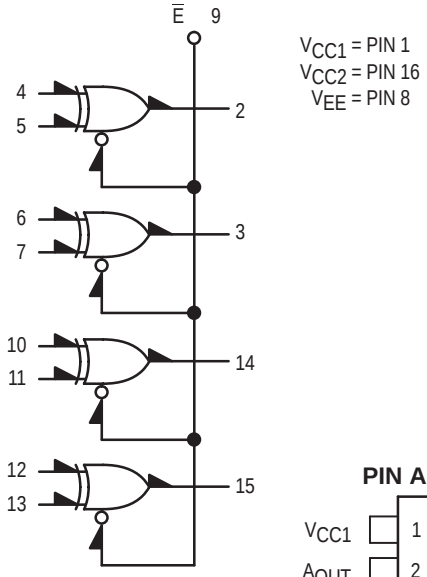
MC10113

Quad Exclusive OR Gate

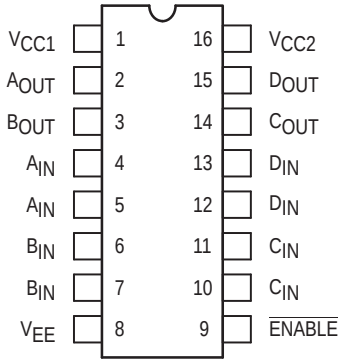
The MC10113 is a quad Exclusive OR gate, with an enable common to all four gates. The outputs may be wire–ORed together to perform a 4–bit comparison function (A = B). The enable is active low.

- P_D = 175 mW typ/pkg (No Load)
- t_{pd} = 2.5 ns typ
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

TRUTH TABLE

IN		$\overline{E}$	OUTPUT
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
X	X	H	L

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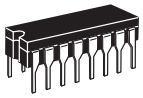
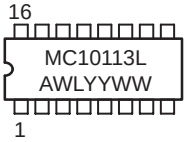
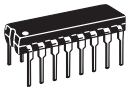
MARKING DIAGRAMS

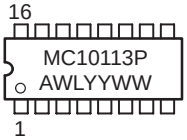


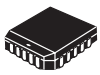
CDIP–16
L SUFFIX
CASE 620



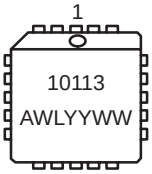


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10113L	CDIP–16	25 Units / Rail
MC10113P	PDIP–16	25 Units / Rail
MC10113FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		46			42		46	mAdc
Input Current	I_{inH}	4,7,10,13 5,6,11,12 9		425 350 870			265 220 545		265 220 545	µAdc
	I_{inL}	*	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	2 3 14 15	–1.060 –1.060 –1.060 –1.060	–0.890 –0.890 –0.890 –0.890	–0.960 –0.960 –0.960 –0.960		–0.810 –0.810 –0.810 –0.810	–0.890 –0.890 –0.890 –0.890	–0.700 –0.700 –0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3 14 15	–1.890 –1.890 –1.890 –1.890	–1.675 –1.675 –1.675 –1.675	–1.850 –1.850 –1.850 –1.850		–1.650 –1.650 –1.650 –1.650	–1.825 –1.825 –1.825 –1.825	–1.615 –1.615 –1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3 14 15	–1.080 –1.080 –1.080 –1.080		–0.980 –0.980 –0.980 –0.980			–0.910 –0.910 –0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3 14 15		–1.655 –1.655 –1.655 –1.655			–1.630 –1.630 –1.630 –1.630		–1.595 –1.595 –1.595 –1.595	Vdc
Switching Times (50Ω Load)					**Min**	**Typ**	**Max**			ns
Propagation Delay	t_{4+2+} t_{4-2-} t_{9+2-} t_{9-2+}	2 2 2 2	1.1 1.1 1.3 1.3	4.7 4.7 5.2 5.2	1.3 1.3 1.5 1.5	2.6 2.6 3.4 3.4	4.5 4.5 5.0 5.0	1.3 1.3 1.5 1.5	5.0 5.0 5.5 5.5	
Rise Time (20 to 80%)	t_{2+}	2	1.1	4.2	1.1	2.5	3.9	1.1	4.4	
Fall Time (20 to 80%)	t_{2-}	2	1.1	4.2	1.1	2.5	3.9	1.1	4.4	

* Individually test each input applying V_{IH} or V_{IL} to input under test.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C			–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C			–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C			–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8					8	1, 16
Input Current	I_{inH}	4,7,10,13	*				8	1, 16
		5,6,11,12	*				8	1, 16
		9	9				8	1, 16
	I_{inL}	*		*			8	1, 16
Output Voltage Logic 1	V_{OH}	2	4				8	1, 16
		3	7				8	1, 16
		14	11				8	1, 16
		15	13				8	1, 16
Output Voltage Logic 0	V_{OL}	2		4			8	1, 16
		3		7			8	1, 16
		14		11			8	1, 16
		15		13			8	1, 16
Threshold Voltage Logic 1	V_{OHA}	2			4		8	1, 16
		3			6		8	1, 16
		14			10		8	1, 16
		15			12		8	1, 16
Threshold Voltage Logic 0	V_{OLA}	2				5	8	1, 16
		3				7	8	1, 16
		14				11	8	1, 16
		15				13	8	1, 16
Switching Times (50Ω Load)			+1.11V		Pulse In	Pulse Out	–3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2			4	2	8	1, 16
	t_{4-2-}	2			4	2	8	1, 16
	t_{9+2-}	2	4		9	2	8	1, 16
	t_{9-2+}	2	4		9	2	8	1, 16
Rise Time (20 to 80%)	t_{2+}	2			4	2	8	1, 16
Fall Time (20 to 80%)	t_{2-}	2			4	2	8	1, 16

* Individually test each input applying V_{IH} or V_{IL} to input under test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10114

Triple Line Receiver

The MC10114 is a triple line receiver designed for use in sensing differential signals over long lines. An active current source and translated emitter follower inputs provide the line receiver with a common mode noise rejection limit of one volt in either the positive or the negative direction. This allows a large amount of common mode noise immunity for extra long lines.

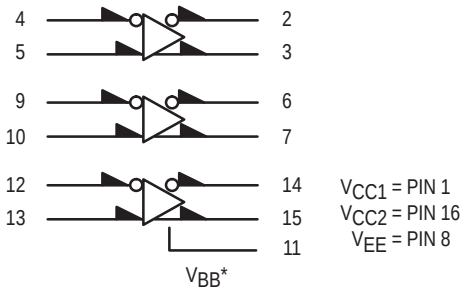
Another feature of the MC10114 is that the OR outputs go to a logic low level whenever the inputs are left floating. The outputs are each capable of driving 50 ohm transmission lines.

This device is useful in high speed central processors, minicomputers, peripheral controllers, digital communication systems, testing and instrumen– tation systems. The MC10114 can also be used for MOS to MECL interfacing and it is ideal as a sense amplifier for MOS RAM's.

A V_{BB} reference is provided which is useful in making the MC10114 a Schmit trigger, allowing single–ended driving of the inputs, or other applications where a stable reference voltage is necessary. See MECL Design Handbook (HB205) pages 226 and 228.

- P_D = 145 mW typ/pkg
- t_{pd} = 2.4 ns typ (Single Ended Input)
- t_{pd} = 2.0 ns typ (Differential Input)
- t_r, t_f = 2.1 ns typ (20%–80%)

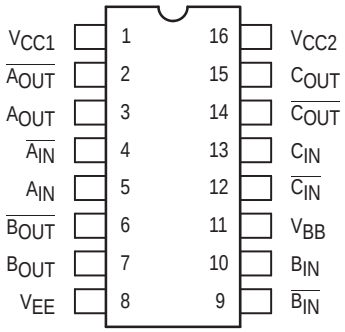
LOGIC DIAGRAM



*V_{BB} to be used to supply bias to the MC10114 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor to ground (0 V). V_{BB} can source < 1.0 mA.

When the input pin with the bubble goes positive, its respective output pin with bubble goes positive.

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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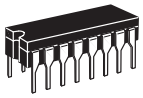
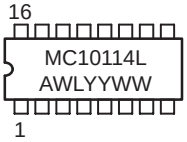
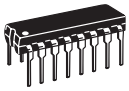
MARKING DIAGRAMS

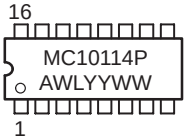


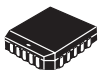
CDIP–16
L SUFFIX
CASE 620





PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10114L	CDIP–16	25 Units / Rail
MC10114P	PDIP–16	25 Units / Rail
MC10114FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		39		28	35		39	mAdc
Input Current	I_{inH}	4		70			45		45	μAdc
	I_{CBO}	4		1.5			1.0		1.0	μAdc
Output Voltage Logic 1	V_{OH}	2 3	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Reference Voltage	V_{BB}	11	–1.420	–1.280	–1.350		–1.230	–1.295	–1.150	Vdc
Common Mode Rejection Test	V_{OH}	2 3	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
	V_{OL}	2 3	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Switching Times (50Ω Load)			**Min**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Max**	ns
Propagation Delay	t_{4+2+} t_{4-2-} t_{4+3-} t_{4-3+}	2 2 3 3	1.0 1.0 1.0 1.0	4.4 4.4 4.4 4.4	1.0 1.0 1.0 1.0	2.4 2.4 2.4 2.4	4.0 4.0 4.0 4.0	0.9 0.9 0.9 0.9	4.3 4.3 4.3 4.3	
Rise Time (20 to 80%)	t_{2+} t_{3+}	2 3	1.5 1.5	3.8 3.8	1.5 1.5	2.1 2.1	3.5 3.5	1.5 1.5	3.7 3.7	
Fall Time (20 to 80%)	t_{2-} t_{3-}	2 3	1.5 1.5	3.8 3.8	1.5 1.5	2.1 2.1	3.5 3.5	1.5 1.5	3.7 3.7	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{BB}
	TEST VOLTAGE VALUES (Volts)				
–30°C	–0.890	–1.890	–1.205	–1.500	From Pin 11
+25°C	–0.810	–1.850	–1.105	–1.475	
+85°C	–0.700	–1.825	–1.035	–1.440	

Characteristic	Symbol	Pin Under Test	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{BB}	Unit
			TEST VOLTAGE APPLIED TO PINS LISTED BELOW					
Power Supply Drain Current	I_E	8		4, 9, 12			5, 10, 13	mAdc
Input Current	I_{inH}	4	4	9, 12			5, 10, 13	µAdc
	I_{inL}	4		9, 12			5, 10, 13	µAdc
Output Voltage Logic 1	V_{OH}	2 3	4 9, 12	9, 12 4			5, 10, 13 5, 10, 13	Vdc
Output Voltage Logic 0	V_{OL}	2 3	9, 12 4	4 9, 12			5, 10, 13 5, 10, 13	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3	 9, 12	9, 12	4	 4	5, 10, 13 5, 10, 13	Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3	9, 12	 9, 12	 4	4	5, 10, 13 5, 10, 13	Vdc
Reference Voltage	V_{BB}	11					5, 10, 13	Vdc
Common Mode Rejection Test	V_{OH}	2 3						Vdc
	V_{OL}	2 3						Vdc
Switching Times (50Ω Load)					**Pulse In**	**Pulse Out**		
Propagation Delay	t_{4+2+} t_{4-2-} t_{4+3-} t_{4-3+}	2 2 3 3			4 4 4 4	2 2 3 3	5, 10, 13 5, 10, 13 5, 10, 13 5, 10, 13	ns
Rise Time (20 to 80%)	t_{2+} t_{3+}	2 3			4 4	2 3	5, 10, 13 5, 10, 13	
Fall Time (20 to 80%)	t_{2-} t_{3-}	2 3			4 4	2 3	5, 10, 13 5, 10, 13	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{EE}
–30°C	+0.110	–0.890	–1.890	–2.890	–5.2
+25°C	+0.190	–0.850	–1.810	–2.850	–5.2
+85°C	+0.300	–0.825	–1.700	–2.825	–5.2

TEST VOLTAGE VALUES (Volts)

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{EE}	
Power Supply Drain Current	I_E	8					8	1, 16
Input Current	I_{inH}	4					8	1, 16
	I_{inL}	4					8, 4	1, 16
Output Voltage Logic 1	V_{OH}	2 3					8 8	1, 16 1, 16
Output Voltage Logic 0	V_{OL}	2 3					8 8	1, 16 1, 16
Threshold Voltage Logic 1	V_{OHA}	2 3					8 8	1, 16 1, 16
Threshold Voltage Logic 0	V_{OLA}	2 3					8 8	1, 16 1, 16
Reference Voltage	V_{BB}	11					8	1, 16
Common Mode Rejection Test	V_{OH}	2 3	4	5	 5	 4	8 8	1, 16 1, 16
	V_{OL}	2 3	 4	 5	5	4	8 8	1, 16 1, 16
Switching Times (50Ω Load)							**–3.2 V**	**+2.0 V**
Propagation Delay	t_{4+2+} t_{4-2-} t_{4+3-} t_{4-3+}	2 2 3 3					8 8 8 8	1, 16 1, 16 1, 16 1, 16
Rise Time (20 to 80%)	t_{2+} t_{3+}	2 3					8 8	1, 16 1, 16
Fall Time (20 to 80%)	t_{2-} t_{3-}	2 3					8 8	1, 16 1, 16

* V_{IHH} = Input Logic 1 level shifted positive one volt for common mode rejection tests
V_{ILH} = Input Logic 0 level shifted positive one volt for common mode rejection tests
V_{IHL} = Input Logic 1 level shifted negative one volt for common mode rejection tests
V_{ILL} = Input Logic 0 level shifted negative one volt for common mode rejection tests

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10115

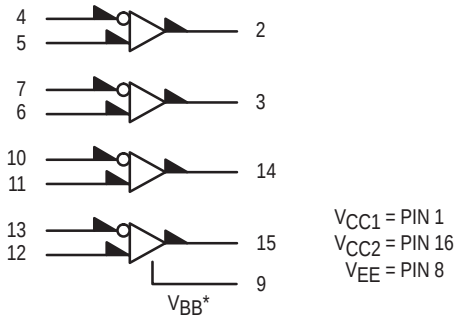
Quad Line Receiver

The MC10115 is a quad differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10115 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 9) to prevent upsetting the current source bias network.

- P_D = 110 mW typ/pkg (No Load)
- t_{pd} = 2.0 ns typ
- t_r, t_f = 2.0 ns typ (20%–80%)

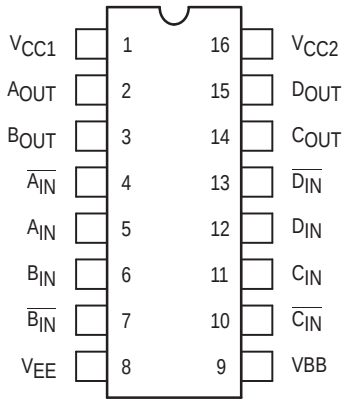
LOGIC DIAGRAM



*V_{BB} to be used to supply bias to the MC10115 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor to ground (0 V). V_{BB} can source < 1.0 mA.

When the input pin with the bubble goes positive, the output goes negative.

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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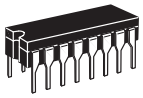
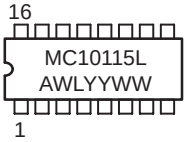
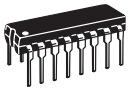
MARKING DIAGRAMS

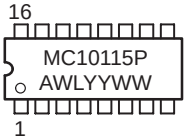


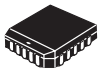
CDIP–16
L SUFFIX
CASE 620



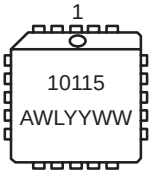


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10115L	CDIP–16	25 Units / Rail
MC10115P	PDIP–16	25 Units / Rail
MC10115FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		29			26		29	mAdc
Input Current	I_{inH}	4		150			95		95	μAdc
	I_{CBO}	4		1.5			1.0		1.0	μAdc
Output Voltage Logic 1	V_{OH}	2	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	Vdc
Output Voltage Logic 0	V_{OL}	2	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2	–1.080		–0.980			–0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2		–1.655			–1.630		–1.595	Vdc
Reference Voltage	V_{BB}	9	1.420	1.280	–1.350		–1.230	1.295	–1.150	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	$t_{4–2+}$	2	1.0	3.1	1.0		2.9	1.0	3.3	
	$t_{4+2–}$	2	1.0	3.1	1.0		2.9	1.0	3.3	
Rise Time (20 to 80%)	t_{2+}	2	1.1	3.6	1.1		3.3	1.1	3.7	
Fall Time (20 to 80%)	$t_{2–}$	2	1.1	3.6	1.1		3.3	1.1	3.7	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{BB}	V_{EE}
–30°C	–0.890	–1.890	–1.205	–1.500	From Pin 9	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475		–5.2
+85°C	–0.700	–1.825	–1.035	–1.440		–5.2

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{BB}	V_{EE}	
Power Supply Drain Current	I_E	8		4,7,10,13			5,6,11,12	8	1, 16
Input Current	I_{inH}	4	4	7,10,13			5,6,11,12	8	1, 16
	I_{CBO}	4		7,10,13			5,6,11,12	8,4	1, 16
Output Voltage Logic 1	V_{OH}	2	7,10,13	4			5,6,11,12	8	1, 16
Output Voltage Logic 0	V_{OL}	2	4	7,10,13			5,6,11,12	8	1, 16
Threshold Voltage Logic 1	V_{OHA}	2		7,10,13		4	5,6,11,12	8	1, 16
Threshold Voltage Logic 0	V_{OLA}	2		7,10,13	4		5,6,11,12	8	1, 16
Reference Voltage	V_{BB}	9					5,6,11,12	8	1, 16
Switching Times (50Ω Load)			Pulse In		Pulse Out			–3.2 V	+2.0 V
Propagation Delay	$t_{4–2+}$	2	4		2		5,6,11,12	8	1, 16
	$t_{4+2–}$	2	4		2		5,6,11,12	8	1, 16
Rise Time (20 to 80%)	t_{2+}	2	4		2		5,6,11,12	8	1, 16
Fall Time (20 to 80%)	$t_{2–}$	2	4		2		5,6,11,12	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10116

Triple Line Receiver

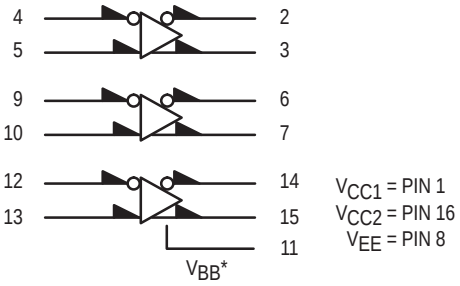
The MC10116 is a triple differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 11 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10116 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 11) to prevent upsetting the current source bias network.

Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to provide complement outputs of the input logic function.

- P_D = 85 mW typ/pkg (No Load)
- t_{pd} = 2.0 ns typ
- t_r, t_f = 2.0 ns typ (20%–80%)

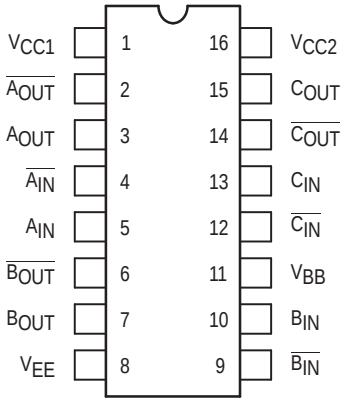
LOGIC DIAGRAM



*V_{BB} to be used to supply bias to the MC10116 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor to ground (0 V). V_{BB} can source < 1.0 mA.

When the input pin with the bubble goes positive, the output pin with the bubble goes positive.

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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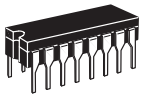
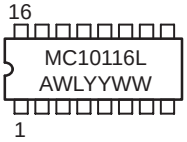
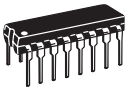
MARKING DIAGRAMS

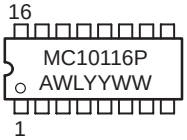


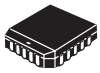
CDIP–16
L SUFFIX
CASE 620



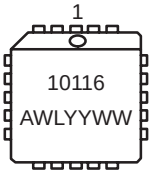


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10116L	CDIP–16	25 Units / Rail
MC10116P	PDIP–16	25 Units / Rail
MC10116FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		23		17	21		23	mAdc
Input Current	I_{inH}	4		150			95		95	μAdc
	I_{CBO}	4		1.5			1.0		1.0	μAdc
Output Voltage Logic 1	V_{OH}	2 3	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Reference Voltage	V_{BB}	11	–1.420	–1.280	–1.350		–1.230	–1.295	–1.150	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{4+2+} t_{4-2-} t_{4+3-} t_{4-3+}	2 2 3 3	1.0 1.0 1.0 1.0	3.1 3.1 3.1 3.1	1.0 1.0 1.0 1.0	2.0 2.0 2.0 2.0	2.9 2.9 2.9 2.9	1.0 1.0 1.0 1.0	3.3 3.3 3.3 3.3	
Rise Time (20 to 80%)	t_{2+} t_{3+}	2 3	1.1 1.1	3.6 3.6	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.7 3.7	
Fall Time (20 to 80%)	t_{2-} t_{3-}	2 3	1.1 1.1	3.6 3.6	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.7 3.7	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{BB}	V_{EE}
–30°C	–0.890	–1.890	–1.205	–1.500	From Pin 11	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475		–5.2
+85°C	–0.700	–1.825	–1.035	–1.440		–5.2

TEST VOLTAGE VALUES (Volts)

Characteristic	Symbol	Pin Under Test	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{BB}	V_{EE}	(V_{CC}) Gnd
			TEST VOLTAGE APPLIED TO PINS LISTED BELOW						
Power Supply Drain Current	I_E	8		4, 9, 12			5, 10, 13	8	1, 16
Input Current	I_{inH}	4	4	9, 12			5, 10, 13	8	1, 16
	I_{CBO}	4		9, 12			5, 10, 13	8,4	1, 16
Output Voltage Logic 1	V_{OH}	2 3	4 9, 12	9, 12 4			5, 10, 13 5, 10, 13	8 8	1, 16 1, 16
Output Voltage Logic 0	V_{OL}	2 3	9, 12 4	4 9, 12			5, 10, 13 5, 10, 13	8 8	1, 16 1, 16
Threshold Voltage Logic 1	V_{OHA}	2 3	 9, 12	9, 12	4	 4	5, 10, 13 5, 10, 13	8 8	1, 16 1, 16
Threshold Voltage Logic 0	V_{OLA}	2 3	 9, 12	9, 12	 4	4 	5, 10, 13 5, 10, 13	8 8	1, 16 1, 16
Reference Voltage	V_{BB}	11					5, 10, 13	8	1, 16
Switching Times (50Ω Load)					**Pulse In**	**Pulse Out**		**–3.2 V**	**+2.0 V**
Propagation Delay	t_{4+2+}	2			4	2	5, 10, 13	8	1, 16
	t_{4-2-}	2			4	2	5, 10, 13	8	1, 16
	t_{4+3-}	3			4	3	5, 10, 13	8	1, 16
	t_{4-3+}	3			4	3	5, 10, 13	8	1, 16
Rise Time (20 to 80%)	t_{2+}	2			4	2	5, 10, 13	8	1, 16
	t_{3+}	3			4	3	5, 10, 13	8	1, 16
Fall Time (20 to 80%)	t_{2-}	2			4	2	5, 10, 13	8	1, 16
	t_{3-}	3			4	3	5, 10, 13	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

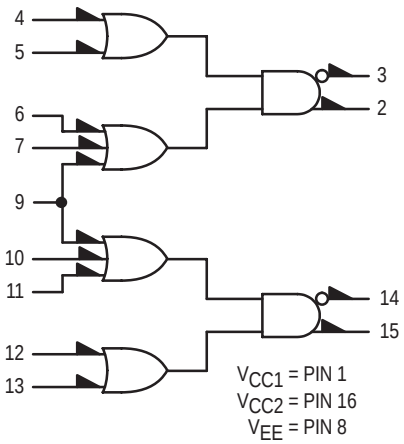
MC10117

Dual 2-Wide 2-3-Input OR-AND/OR-AND Gate

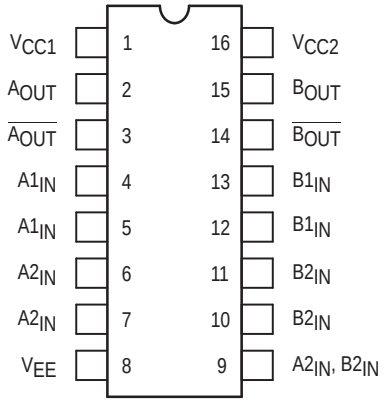
The MC10117 is a dual 2–wide 2–3–input OR–AND/OR–AND–Invert gate. This general purpose logic element is designed for use in data control, such as digital multiplexing or data distribution. Pin 9 is common to both gates.

- P_D = 100 mW typ/pkg (No Load)
- t_{pd} = 2.3 ns typ
- t_r, t_f = 2.2 ns typ (20%–80%)

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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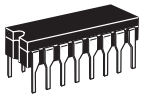
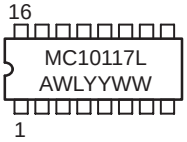
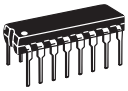
MARKING DIAGRAMS

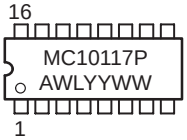


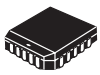
CDIP–16
L SUFFIX
CASE 620



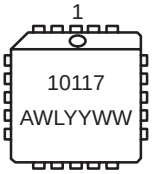


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10117L	CDIP–16	25 Units / Rail
MC10117P	PDIP–16	25 Units / Rail
MC10117FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		29		20	26		29	mAdc
Input Current	I_{inH}*	6 9 4		425 560 390			265 350 245		265 350 245	µAdc
	I_{inL}	4	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	2 3	–1.060 –1.060	–0.890 –0.780	–0.960 –0.960		–0.810 –0.700	–0.890 –0.890	–0.700 –0.590	Vdc
Output Voltage Logic 0	V_{OL}	2 3	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{4+2+} t_{4-2-} t_{4+3-} t_{4-3+}	2 2 3 3	1.4 1.4 1.4 1.4	3.9 3.9 3.9 3.9	1.4 1.4 1.4 1.4	2.3 2.3 2.3 2.3	3.4 3.4 3.4 3.4	1.4 1.4 1.4 1.4	3.8 3.8 3.8 3.8	
Rise Time (20 to 80%)	t_{2+} t_{3+}	2 3	0.9 0.9	4.1 4.1	1.1 1.1	2.2 2.2	4.0 4.0	1.1 1.1	4.6 4.6	
Fall Time (20 to 80%)	t_{2-} t_{3-}	2 3	0.9 0.9	4.1 4.1	1.1 1.1	2.2 2.2	4.0 4.0	1.1 1.1	4.6 4.6	

* Inputs 4, 5, 12 and 13 have same I_{inH} limit.
Inputs 6, 7, 10 and 11 have same I_{inH} limit.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C			–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C			–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C			–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					**(V_{CC}) Gnd**
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}*	6	4				8	1, 16
			9	9				8	1, 16
			4		4			8	1, 16
		I_{inL}	4		9			8	1, 16
Output Voltage	Logic 1	V_{OH}	2	4, 9				8	1, 16
			3					8	1, 16
Output Voltage	Logic 0	V_{OL}	2					8	1, 16
			3	4, 9				8	1, 16
Threshold Voltage	Logic 1	V_{OHA}	2	9		4		8	1, 16
			3				4	8	1, 16
Threshold Voltage	Logic 0	V_{OLA}	2				4	8	1, 16
			3	9		4		8	1, 16
Switching Times	(50Ω Load)			**+1.11V**		**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay		t_{4+2+}	2	9		4	2	8	1, 16
		$t_{4–2–}$	2	9		4	2	8	1, 16
		$t_{4+3–}$	3	9		4	3	8	1, 16
		$t_{4–3+}$	3	9		4	3	8	1, 16
Rise Time	(20 to 80%)	t_{2+}	2	9		4	2	8	1, 16
		t_{3+}	3	9		4	3	8	1, 16
Fall Time	(20 to 80%)	$t_{2–}$	2	9		4	2	8	1, 16
		$t_{3–}$	3	9		4	3	8	1, 16

* Inputs 4, 5, 12 and 13 have same I_{inH} limit.
Inputs 6, 7, 10 and 11 have same I_{inH} limit.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

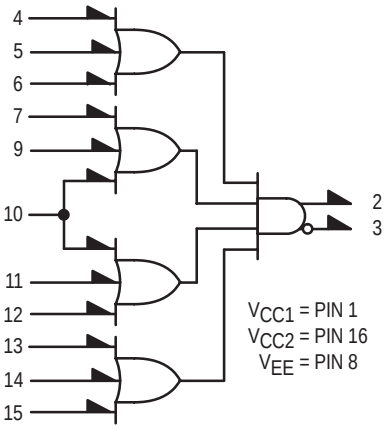
MC10121

4-Wide OR-AND/$\overline{\text{OR-AND}}$ Gate

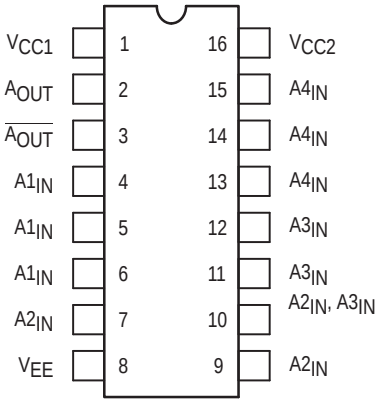
The MC10121 is a basic logic building block providing the simultaneous OR–AND/OR–AND–Invert function, useful in data control and digital multiplexing applications.

- P_D = 100 mW typ/pkg (No Load)
- t_{pd} = 2.3 ns typ
- t_r, t_f = 2.5 ns typ (20%–80%)

LOGIC DIAGRAM



DIP
PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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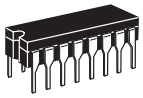
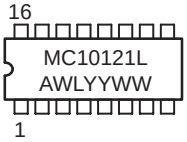
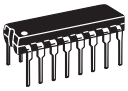
MARKING DIAGRAMS

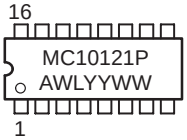


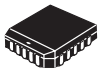
CDIP–16
L SUFFIX
CASE 620



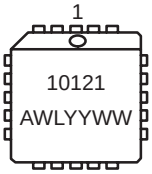


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10121L	CDIP–16	25 Units / Rail
MC10121P	PDIP–16	25 Units / Rail
MC10121FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		29		20	26		29	mAdc
Input Current	I_{inH}	7 9 10		390 390 495			245 245 310		245 245 310	μAdc
	I_{inL}	7 9 10	0.5 0.5 0.5		0.5 0.5 0.5			0.3 0.3 0.3		μAdc
Output Voltage Logic 1	V_{OH}	3 2	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	3 2	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	3 2	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	3 2		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{4+3-} t_{4-3+} t_{4+2+} t_{4-2-}	3 3 2 2	1.4 1.4 1.4 1.4	3.6 3.6 3.6 3.6	1.4 1.4 1.4 1.4	2.3 2.3 2.3 2.3	3.4 3.4 3.4 3.4	1.4 1.4 1.4 1.4	3.5 3.5 3.5 3.5	
Rise Time (20 to 80%)	t_{3+} t_{2+}	3 2	0.9 0.9	4.1 4.1	1.1 1.1	2.5 2.5	4.0 4.0	1.1 1.1	4.6 4.6	
Fall Time (20 to 80%)	t_{3-} t_{2-}	3 2	0.9 0.9	4.1 4.1	1.1 1.1	2.5 2.5	4.0 4.0	1.1 1.1	4.6 4.6	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C			–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C			–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C			–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	7 9 10	7 9 10				8 8 8	1, 16 1, 16 1, 16
		I_{inL}	7 9 10		7 9 10			8 8 8	1, 16 1, 16 1, 16
Output Voltage	Logic 1	V_{OH}	3 2	 4, 10, 13				8 8	1, 16 1, 16
Output Voltage	Logic 0	V_{OL}	3 2	4, 10, 13				8 8	1, 16 1, 16
Threshold Voltage	Logic 1	V_{OHA}	3 2	 10, 13		 4	4	8 8	1, 16 1, 16
Threshold Voltage	Logic 0	V_{OLA}	3 2	 10, 13		4	 4	8 8	1, 16 1, 16
Switching Times	(50Ω Load)			**+1.11V**		**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay		t_{4+3-}	3	10, 13		4	3	8	1, 16
		t_{4-3+}	3	10, 13		4	3	8	1, 16
		t_{4+2+}	2	10, 13		4	2	8	1, 16
		t_{4-2-}	2	10, 13		4	2	8	1, 16
Rise Time	(20 to 80%)	t_{3+}	3	10, 13		4	3	8	1, 16
		t_{2+}	2	10, 13		4	2	8	1, 16
Fall Time	(20 to 80%)	t_{3-}	3	10, 13		4	3	8	1, 16
		t_{2-}	2	10, 13		4	2	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10123

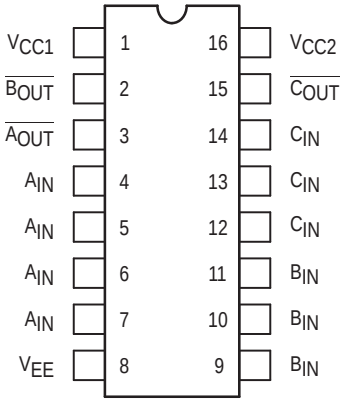
Triple 4-3-3-Input Bus Driver

The MC10123 consists of three NOR gates designed for bus driving applications on card or between cards. Output low logic levels are specified with V_{OL} = –2.1 Vdc so that the bus may be terminated to –2.0 Vdc. The gate output, when low, appears as a high impedance to the bus, because the output emitter– followers of the MC10123 are "turned–off." This eliminates discontinuities in the characteristic impedance of the bus.

The V_{OH} level is specified when driving a 25–ohm load terminated to –2.0 Vdc, the equivalent of a 50–ohm bus terminated at both ends. Although 25 ohms is the lowest characteristic impedance that can be driven by the MC10123, higher impedance values may be used with this part. A typical 50–ohm bus is shown in Figure 1.

- P_D = 310 mW typ/pkg (No Load)
- t_{pd} = 3.0 ns typ
- t_r, t_f = 2.5 ns typ (20%–80%)

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

LOGIC DIAGRAM

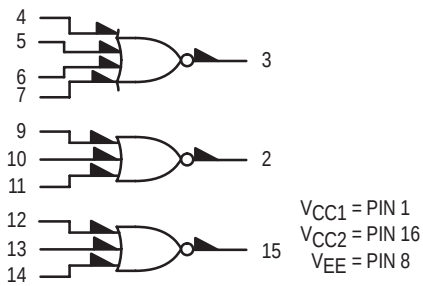
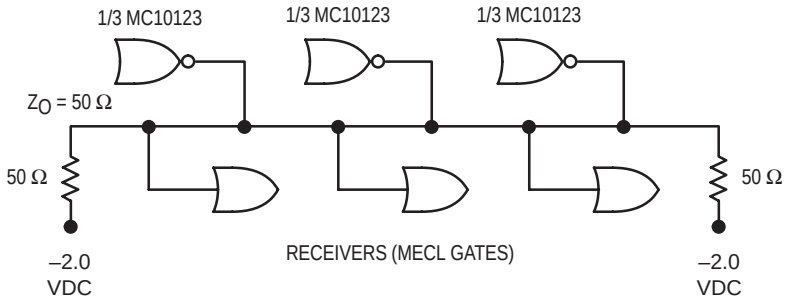


FIGURE 1 — 50–OHM BUS DRIVER (TYPICAL APPLICATION)



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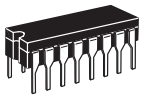
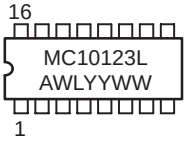
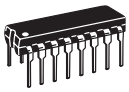
MARKING DIAGRAMS

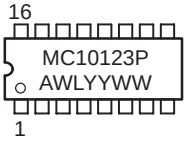


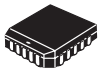
CDIP–16
L SUFFIX
CASE 620



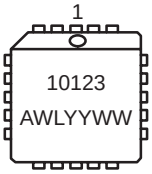


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10123L	CDIP–16	25 Units / Rail
MC10123P	PDIP–16	25 Units / Rail
MC10123FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		82		71	75		82	mAdc
Input Current	I_{inH}	4		350			220		220	µAdc
	I_{inL}	4			0.5					µAdc
Output Voltage Logic 1	V_{OH}	3	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	Vdc
Output Voltage Logic 0	V_{OL}	3	–2.100	–2.030	–2.100		–2.030	–2.100	–2.030	Vdc
Threshold Voltage Logic 1	V_{OHA}	3	–1.080		–0.980			–0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	3		–2.100			–2.100		–2.100	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{4+3-} t_{4-3+}	3 3	1.2 1.2	4.6 4.6	1.2 1.2	3.0 3.0	4.4 4.4	1.2 1.2	4.8 4.8	
Rise Time (20 to 80%)	t_{3+}	3	1.0	3.7	1.0	2.5	3.5	1.0	3.9	
Fall Time (20 to 80%)	t_{3-}	3	1.0	3.7	1.0	2.5	3.5	1.0	3.9	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts)					
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8	4,5,6,7,9 10,11,12 13,14				8	1, 16
Input Current	I_{inH}	4	4				8	1, 16
	I_{inL}	4		4			8	1, 16
Output Voltage Logic 1	V_{OH}	3					8	1, 16
Output Voltage Logic 0	V_{OL}	3	4,5,6,7 9,12				8	1, 16
Threshold Voltage Logic 1	V_{OHA}	3				4,5,6,7	8	1, 16
Threshold Voltage Logic 0	V_{OLA}	3	9,12		4,5,6,7		8	1, 16
Switching Times (50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	t_{4+3-} t_{4-3+}	3 3			4 4	3 3	8 8	1, 16 1, 16
Rise Time (20 to 80%)	t_{3+}	3			4	3	8	1, 16
Fall Time (20 to 80%)	t_{3-}	3			4	3	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10124

Quad TTL to MECL Translator

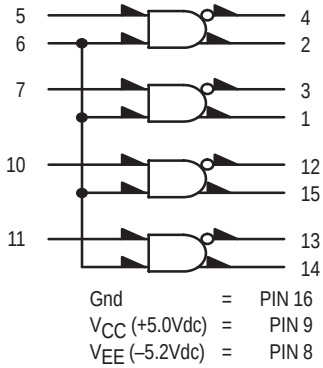
The MC10124 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The MC10124 has TTL compatible inputs, and MECL complementary open–emitter outputs that allow use as an inverting/ non–inverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to a MECL low logic state and all inverting outputs to a MECL high logic state.

Power supply requirements are ground, +5.0 Volts, and –5.2 Volts. Propagation delay of the MC10124 is typically 3.5 ns. The dc levels are standard or Schottky TTL in, MECL 10,000 out.

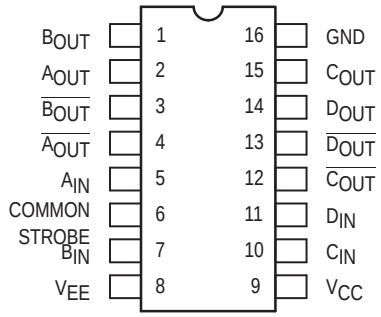
An advantage of this device is that TTL level information can be transmitted differentially, via balanced twisted pair lines, to the MECL equipment, where the signal can be received by the MC10115 or MC10116 differential line receivers. The MC10124 is useful in computers, instrumentation, peripheral controllers, test equipment, and digital communications systems.

- P_D = 380 mW typ/pkg (No Load)
- t_{pd} = 3.5 ns typ (+ 1.5 Vdc in to 50% out)
- t_r, t_f = 2.5 ns typ (20%–80%)

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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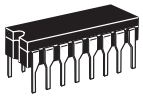
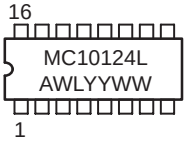
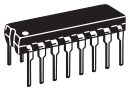
MARKING DIAGRAMS

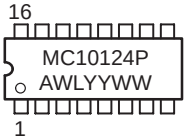


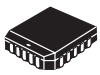
CDIP–16
L SUFFIX
CASE 620



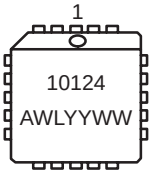


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10124L	CDIP–16	25 Units / Rail
MC10124P	PDIP–16	25 Units / Rail
MC10124FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Negative Power Supply Drain Current	I_E	8		72			66		72	mAdc
Positive Power Supply Drain Current	I_{CCH}	9		16			16		18	mAdc
	I_{CCL}	9		25			25		25	mAdc
Reverse Current	I_R	6 7		200 50			200 50		200 50	µAdc
Forward Current	I_F	6 7		–12.8 –3.2			–12.8 –3.2		–12.8 –3.2	mAdc
Input Breakdown Voltage	BV_{in}	6 7	5.5 5.5		5.5 5.5			5.5 5.5		Vdc
Clamp Input Voltage	V_I	6 7		–1.5 –1.5			–1.5 –1.5		–1.5 –1.5	Vdc
High Output Voltage	V_{OH}	1 3	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Low Output Voltage	V_{OL}	1 3	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
High Threshold Voltage	V_{OHA}	1 3	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Low Threshold Voltage	V_{OLA}	1 3		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay (+3.5Vdc to 50%)[1]	t_{6+1+} t_{6-1-} t_{7+1+} t_{7-1-} t_{7+3-} t_{7-3+}	1 1 1 1 3 3	1.5 1.0 1.5 1.0 1.5 1.0	6.8 6.0 6.8 6.0 6.8 6.0	1.0 1.0 1.0 1.0 1.0 1.0	3.5 3.5 3.5 3.5 3.5 3.5	6.0 6.0 6.0 6.0 6.0 6.0	1.0 1.5 1.0 1.5 1.0 1.5	6.0 6.8 6.0 6.8 6.0 6.8	
Rise Time (20 to 80%)	t_{1+}	1	1.0	4.2	1.1	2.5	3.9	1.1	4.3	
Fall Time (20 to 80%)	t_{1-}	1	1.0	4.2	1.1	2.5	3.9	1.1	4.3	

1. See switching time test circuit. Propagation delay for this circuit is specified from +1.5Vdc in to the 50% point on the output waveform. The +3.5Vdc is shown here because all logic and supply levels are shifted 2 volts positive.

ELECTRICAL CHARACTERISTICS (continued)

			TEST VOLTAGE VALUES (Volts)					
		@ Test Temperature	V_{IH}	V_{ILmax}	$V_{IHA'}$	$V_{ILA'}$	V_F	
		–30°C	+4.0	+0.40	+2.00	+1.10	+0.40	
		+25°C	+4.0	+0.40	+1.80	+1.10	+0.40	
		+85°C	+4.0	+0.40	+1.80	+0.90	+0.40	
Characteristic	**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					
			V_{IH}	V_{ILmax}	$V_{IHA'}$	$V_{ILA'}$	V_F	**Gnd**
Negative Power Supply Drain Current	I_E	8						16
Positive Power Supply Drain Current	I_{CCH}	9	5,6,7,10,11					16
	I_{CCL}	9						5,6,7,10,11,16
Reverse Current	I_R	6 7					5,7,10,11 6	16 16
Forward Current	I_F	6 7	5,7,10,11 6				6 7	16 16
Input Breakdown Voltage	BV_{in}	6 7						5,7,10,11,16 6,16
Clamp Input Voltage	V_I	6 7						16 16
High Output Voltage	V_{OH}	1 3	6,7	6,7				16 16
Low Output Voltage	V_{OL}	1 3	6,7	6,7				16 16
High Threshold Voltage	V_{OHA}	1 3	6 6		7	7		16 16
Low Threshold Voltage	V_{OLA}	1 3	6 6		7	7		16 16
Switching Times (50Ω Load)			**+6.0 V**	**Pulse In**	**Pulse Out**			**+2.0 V**
Propagation Delay (+3.5Vdc to 50%)[1]	t_{6+1+}	1	7	6	1			16
	t_{6-1-}	1	7	6	1			16
	t_{7+1+}	1	6	7	1			16
	t_{7-1-}	1	6	7	1			16
	t_{7+3-}	3	6	7	3			16
	t_{7-3+}	3	6	7	3			16
Rise Time (20 to 80%)	t_{1+}	1	6	7	1			16
Fall Time (20 to 80%)	t_{1-}	1	6	7	1			16

1. See switching time test circuit. Propagation delay for this circuit is specified from +1.5Vdc in to the 50% point on the output waveform. The +3.5Vdc is shown here because all logic and supply levels are shifted 2 volts positive.

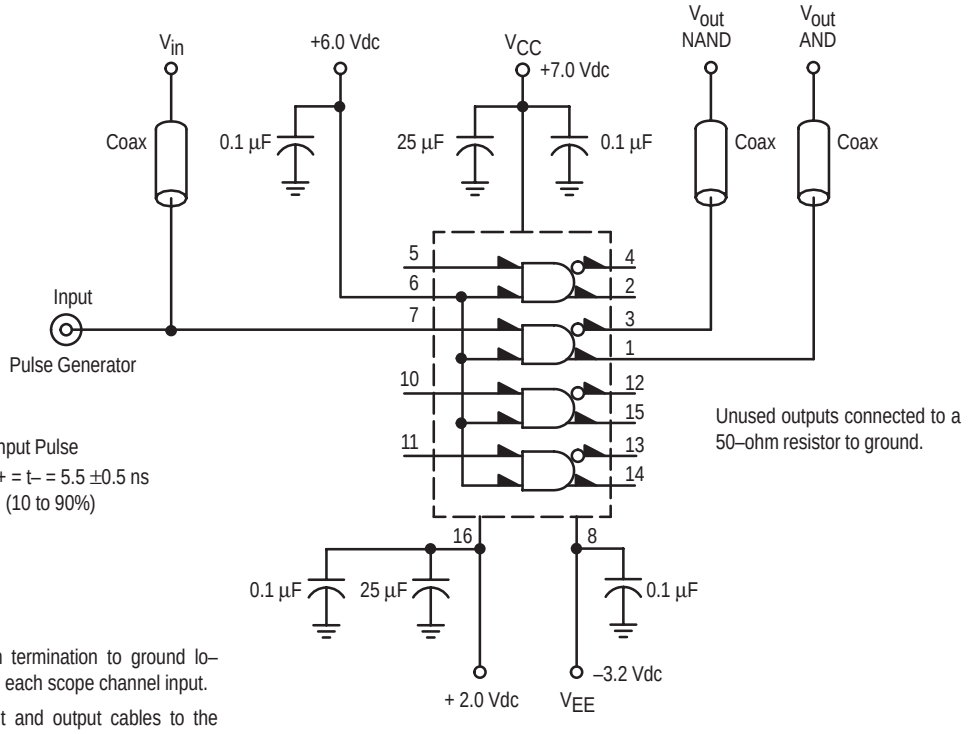
ELECTRICAL CHARACTERISTICS (continued)

			TEST VOLTAGE VALUES (Volts)			(mA)		
		@ Test Temperature	V_R	V_{CC}	V_{EE}	I_I	I_{in}	
		–30°C	+2.40	+5.00	–5.2	–10	+1.0	
		+25°C	+2.40	+5.00	–5.2	–10	+1.0	
		+85°C	+2.40	+5.00	–5.2	–10	+1.0	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					Gnd
			V_R	V_{CC}	V_{EE}	I_I	I_{in}	
Negative Power Supply Drain Current	I_E	8		9	8			16
Positive Power Supply Drain Current	I_{CCH}	9		9	8			16
	I_{CCL}	9		9	8			5,6,7,10,11,16
Reverse Current	I_R	6 7	6 7	9 9	8 8			16 16
Forward Current	I_F	6 7		9 9	8 8			16 16
Input Breakdown Voltage	BV_{in}	6 7		9 9	8 8		6 7	5,7,10,11,16 6,16
Clamp Input Voltage	V_I	6 7		9 9	8 8	6 7		16 16
High Output Voltage	V_{OH}	1 3		9 9	8 8			16 16
Low Output Voltage	V_{OL}	1 3		9 9	8 8			16 16
High Threshold Voltage	V_{OHA}	1 3		9 9	8 8			16 16
Low Threshold Voltage	V_{OLA}	1 3		9 9	8 8			16 16
Switching Times (50Ω Load)				**+7.0 V**	**–3.2 V**			**+2.0 V**
Propagation Delay (+3.5Vdc to 50%)[1]	t_{6+1+} t_{6-1-} t_{7+1+} t_{7-1-} t_{7+3-} t_{7-3+}	1 1 1 1 3 3		9 9 9 9 9 9	8 8 8 8 8 8			16 16 16 16 16 16
Rise Time (20 to 80%)	t_{1+}	1		9	8			16
Fall Time (20 to 80%)	t_{1-}	1		9	8			16

1. See switching time test circuit. Propagation delay for this circuit is specified from +1.5Vdc in to the 50% point on the output waveform. The +3.5Vdc is shown here because all logic and supply levels are shifted 2 volts positive.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

SWITCHING TIME TEST CIRCUIT



Input Pulse
t+ = t– = 5.5 ±0.5 ns
(10 to 90%)

Unused outputs connected to a 50–ohm resistor to ground.

50–ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50–ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

NOTE: All power supply and logic levels are shown shifted 2 volts positive.

MC10125

Quad MECL to TTL Translator

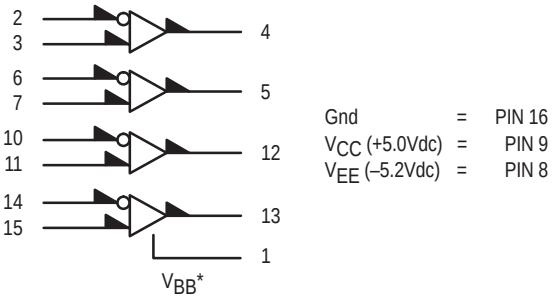
The MC10125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic sections of digital systems. The MC10125 incorporates differential inputs and Schottky TTL "totem pole" outputs. Differential inputs allow for use as an inverting/ non–inverting translator or as a differential line receiver. The V_{BB} reference voltage is available on pin 1 for use in single–ended input biasing. The outputs of the MC10125 go to a low logic level whenever the inputs are left floating.

Power supply requirements are ground, +5.0 Volts and –5.2 Volts. Propagation delay of the MC10125 is typically 4.5 ns. The MC10125 has fanout of 10 TTL loads. The dc levels are MECL 10,000 in and Schottky TTL, or TTL out. This device has an input common mode noise rejection of ± 1.0 Volt.

An advantage of this device is that MECL level information can be received, via balanced twisted pair lines, in the TTL equipment. This isolates the MECL logic from the noisy TTL environment. This device is useful in computers, instrumentation, peripheral controllers, test equipment and digital communications systems.

- P_D = 380 mW typ/pkg (No Load)
- t_{pd} = 4.5 ns typ (50% to + 1.5 Vdc out)
- t_r, t_f = 2.5 ns typ (1.0 V to 2.0 V)

LOGIC DIAGRAM

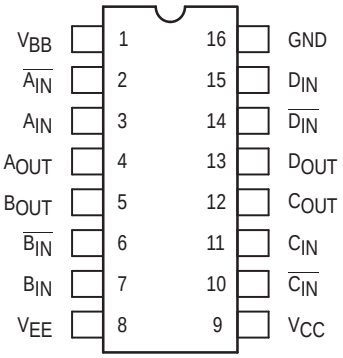


Gnd = PIN 16
V_{CC} (+5.0Vdc) = PIN 9
V_{EE} (–5.2Vdc) = PIN 8

*V_{BB} to be used to supply bias to the MC10125 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor to ground (0 V). V_{BB} can source < 1.0 mA.

When the input pin with the bubble goes positive, the output goes negative.

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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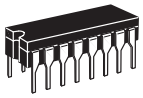
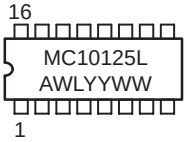
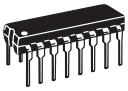
MARKING DIAGRAMS

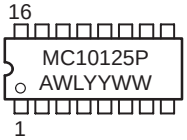


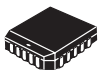
CDIP–16
L SUFFIX
CASE 620



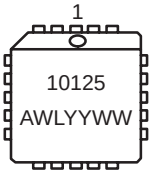


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10125L	CDIP–16	25 Units / Rail
MC10125P	PDIP–16	25 Units / Rail
MC10125FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Negative Power Supply Drain Current	I_E	8		–44			–40		–44	mAdc
Positive Power Supply Drain Current	I_{CCH}	9		52			52		52	mAdc
	I_{CCL}	9		39			39		39	mAdc
Input Current	I_{inH}[1]	2		180			115		115	µAdc
Input Leakage Current	I_{CBO}	2		1.5			1.0		1.0	µAdc
High Output Voltage	V_{OH}	4	2.5		2.5			2.5		Vdc
Low Output Voltage	V_{OL}	4		0.5			0.5		0.5	Vdc
High Threshold Voltage	V_{OHA}	4	2.5		2.5			2.5		Vdc
Low Threshold Voltage	V_{OLA}	4		0.5			0.5		0.5	Vdc
Indeterminate Input Protection Tests	V_{OLS1}	4		0.5			0.5		0.5	Vdc
	V_{OLS2}	4		0.5			0.5		0.5	Vdc
Short Circuit Current	I_{OS}	4	40	100	40		100	40	100	mAdc
Reference Voltage	V_{BB}	1	–1.420	–1.280	–1.350		–1.230	–1.295	–1.150	Vdc
Common Mode Rejection Tests	V_{OH}	4 4	2.5 2.5		2.5 2.5			2.5 2.5		Vdc
	V_{OL}	4 4		0.5 0.5			0.5 0.5		0.5 0.5	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay (50% to +1.5Vdc)	t_{6+5-} t_{6-5+} t_{2+4-} t_{2-4+}	5 5 4 4	1.0 1.0 1.0 1.0	6.0 6.0 6.0 6.0	1.0 1.0 1.0 1.0	4.5 4.5 4.5 4.5	6.0 6.0 6.0 6.0	1.0 1.0 1.0 1.0	6.0 6.0 6.0 6.0	
Rise Time (+1.0V to 2.0V)	t_{4+}	4		3.3			3.3		3.3	
Fall Time (+1.0V to 2.0V)	t_{4-}	4		3.3			3.3		3.3	

1. Individually test each output, apply V_{IHmax} to pin under test.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)							
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHH}	V_{ILH}		
–30°C			–0.890	–1.890	–1.205	–1.500	+0.110	–0.890		
+25°C			–0.810	–1.850	–1.105	–1.475	+0.190	–0.850		
+85°C			–0.700	–1.825	–1.035	–1.440	+0.300	–0.825		
Characteristic	**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**						**Gnd**	**Output Condition**
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHH}	V_{ILH}		
Negative Power Supply Drain Current	I_E	8							16	
Positive Power Supply Drain Current	I_{CCH}	9	2,6,10,14						16	
	I_{CCL}	9		2,6,10,14					16	
Input Current	I_{inH}[1]	2	2,6,10,14						16	
Input Leakage Current	I_{CBO}	2							16	
High Output Voltage	V_{OH}	4		2,6,10,14					16	–2.0mA
Low Output Voltage	V_{OL}	4	2,6,10,14						16	20mA
High Threshold Voltage	V_{OHA}	4		6,10,14		2			16	–2.0mA
Low Threshold Voltage	V_{OLA}	4	6,10,14		2				16	20mA
Indeterminate Input Protection Tests	V_{OLS1}	4							16	20mA
	V_{OLS2}	4							16	20mA
Short Circuit Current	I_{OS}	4		2,6,10,14					4, 16	
Reference Voltage	V_{BB}	1		2,6,10,14						
Common Mode Rejection Tests	V_{OH}	4 4					3	2	16 16	–2.0mA –2.0mA
	V_{OL}	4 4					2	3	16 16	20mA 20mA
Switching Times (50Ω Load)			**Pulse In**	**Pulse Out**	**C_L** (pF)					
Propagation Delay (50% to +1.5Vdc)	t_{6+5-}	5	6	5	25				16	
	t_{6-5+}	5	6	5	25				16	
	t_{2+4-}	4	2	4	25				16	
	t_{2-4+}	4	2	4	25				16	
Rise Time (+1.0V to 2.0V)	t_{4+}	4	2	4	25				16	
Fall Time (+1.0V to 2.0V)	t_{4-}	4	2	4	25				16	

1. Individually test each output, apply V_{IHmax} to pin under test.

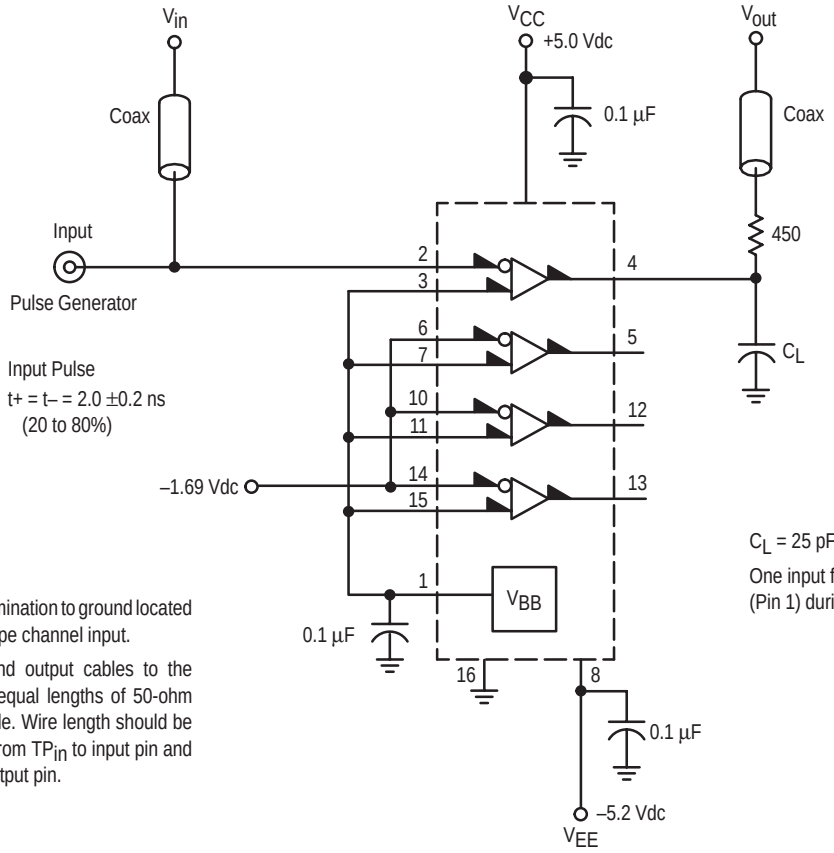
ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)						
			V_{IHH}	V_{ILH}	V_{BB}	V_{CC}	V_{EE}		
–30°C			–1.890	–2.890	From Pin 1	+5.0	–5.2		
+25°C			–1.810	–2.850		+5.0	–5.2		
+85°C			–1.700	–2.825		+5.0	–5.2		
Characteristic	**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					**Gnd**	**Output Condition**
			V_{IHH}	V_{ILH}	V_{BB}	V_{CC}	V_{EE}		
Negative Power Supply Drain Current	I_E	8			3,7,11,15	9	8	16	
Positive Power Supply Drain Current	I_{CCH}	9			3,7,11,15	9	8	16	
	I_{CCL}	9			3,7,11,15	9	8	16	
Input Current	I_{inH}[1]	2			3,7,11,15	9	8	16	
Input Leakage Current	I_{CBO}	2			3,7,11,15	9	2,6,8,10,14	16	
High Output Voltage	V_{OH}	4			3,7,11,15	9	8	16	–2.0mA
Low Output Voltage	V_{OL}	4			3,7,11,15	9	8	16	20mA
High Threshold Voltage	V_{OHA}	4			3,7,11,15	9	8	16	–2.0mA
Low Threshold Voltage	V_{OLA}	4			3,7,11,15	9	8	16	20mA
Indeterminate Input Protection Tests	V_{OLS1}	4				9	2,3,6,7,8, 10,11,14,15	16	20mA
	V_{OLS2}	4				9	8	16	20mA
Short Circuit Current	I_{OS}	4			3,7,11,15	9	8	4, 16	
Reference Voltage	V_{BB}	1			3,7,11,15				
Common Mode Rejection Tests	V_{OH}	4 4	 3	 2		9 9	8 8	16 16	–2.0mA –2.0mA
	V_{OL}	4 4	 2	 3		9 9	8 8	16 16	20mA 20mA
Switching Times (50Ω Load)									
Propagation Delay (50% to +1.5Vdc)	t_{6+5-} t_{6-5+} t_{2+4-} t_{2-4+}	5 5 4 4			3,7,11,15 3,7,11,15 3,7,11,15 3,7,11,15	9 9 9 9	8 8 8 8	16 16 16 16	
Rise Time (+1.0V to 2.0V)	t_{4+}	4			3,7,11,15	9	8	16	
Fall Time (+1.0V to 2.0V)	t_{4-}	4			3,7,11,15	9	8	16	

1. Individually test each output, apply V_{IHmax} to pin under test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

SWITCHING TIME TEST CIRCUIT



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

C_L = 25 pF, including test fixture

One input from each gate must be tied to V_{BB} (Pin 1) during testing.

MC10129

Quad Bus Receiver

The MC10129 data inputs are compatible with, and accept TTL logic levels as well as levels compatible with IBM–type buses. The clock, strobe, and reset inputs accept MECL 10,000 logic levels.

The data inputs accept the bus levels, and storage elements are provided to yield temporary latch storage of the information after receiving it from the bus. The outputs can be strobed to allow accurate synchronization of signals and/or connection to MECL 10,000 level buses. When the clock is low, and the reset input is disabled, the outputs will follow the D inputs. The latches will store the data on the rising edge of the clock. The outputs are enabled when the strobe input is high. Unused D inputs must be tied to V_{CC} or Gnd. The clock, strobe, and reset inputs each have 50 k ohm pulldown resistors to V_{EE}. They may be left floating, if not used.

The MC10129 will operate in either of two modes. The first mode is obtained by tying the hysteresis control input to V_{EE}. In this mode, the input threshold points of the D inputs are fixed. The second mode is obtained by tying the hysteresis control input to ground. In this mode, input hysteresis is achieved as shown in the test table. This hysteresis is desirable where extra noise margin is required on the D inputs. The outer input pins are unaffected by the mode of operation used.

The MC10129 is especially useful in interface applications for central processors, mini–computers, and peripheral equipment.

- P_D = 750 mW typ/pkg (No Load)
- t_{pd} = 10 ns typ
- V_{CC} Max = 7.0 Vdc

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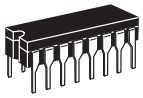
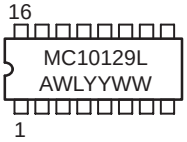
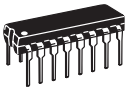
MARKING DIAGRAMS

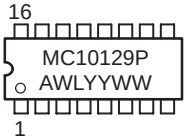


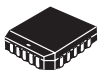
CDIP–16
L SUFFIX
CASE 620



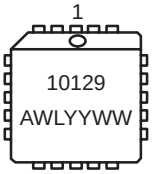


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

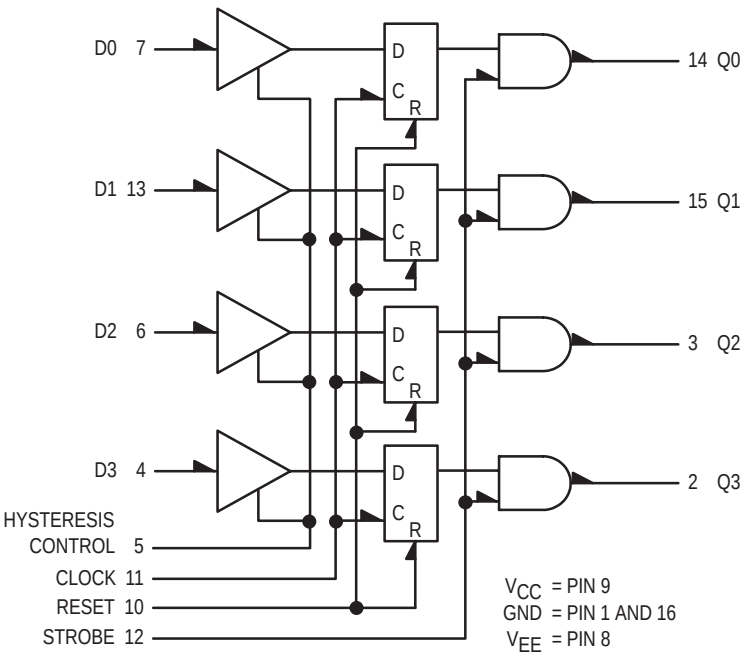


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

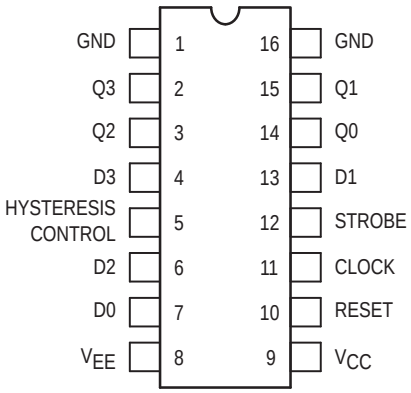
ORDERING INFORMATION

Device	Package	Shipping
MC10129L	CDIP–16	25 Units / Rail
MC10129P	PDIP–16	25 Units / Rail
MC10129FN	PLCC–20	46 Units / Rail

LOGIC DIAGRAM



PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

TRUTH TABLE

D	C	STROBE	RESET	Q_{n+1}
X	X	L	X	L
X	H	X	H	L
L	L	H	X	L
X	H	H	L	Q_n
H	L	H	X	H

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Negative Power Supply Drain Current	I_E	8 8		167 189			152 172		167 189	mAdc
Positive Power Supply Drain Current	I_{CC}	9		8.0			8.0		8.0	mAdc
Input Current	I_{inH}	4 6 7 10 11 12 13		150 150 150 720 390 390 150			95 95 95 450 245 245 95		95 95 95 450 245 245 95	µAdc
	I_{CBO} (1.)	4 6 7 13		1.5 1.5 1.5	 –1.0		–1.0 –1.0 –1.0		1.0 1.0 1.0	µAdc
	I_{inL}	10 11 12	0.5 0.5 0.5		0.5 0.5 0.5			0.3 0.3 0.3		µAdc
Output Voltage Logic 1	V_{OH}	2 3 2 3	–1.060 –1.060 –1.060 –1.060	–0.890 –0.890 –0.890 –0.890	–0.960 –0.960 –0.960 –0.960		–0.810 –0.810 –0.810 –0.810	–0.890 –0.890 –0.890 –0.890	–0.700 –0.700 –0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3 2 3	–1.890 –1.890 –1.890 –1.890	–1.675 –1.675 –1.675 –1.675	–1.850 –1.850 –1.850 –1.850		–1.650 –1.650 –1.650 –1.650	–1.825 –1.825 –1.825 –1.825	–1.615 –1.615 –1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 (2.) 2 2 2 2 (3.) 2 (4.)	–1.080 –1.080 –1.080 –1.080 –1.080 –1.080		–0.980 –0.980 –0.980 –0.980 –0.980 –0.980			–0.910 –0.910 –0.910 –0.910 –0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 (2.) 2 2 (2.) 2 2 (3.) 2 (4.)		–1.655 –1.655 –1.655 –1.655 –1.655 –1.655			–1.630 –1.630 –1.630 –1.630 –1.630 –1.630		–1.595 –1.595 –1.595 –1.595 –1.595 –1.595	Vdc
Switching Times Propagation Delay										ns
Data Input	t_{7+14+} t_{7-14-}	14 14	3.7 3.7	15 15	3.7 3.7	10 10	15 15	3.7 3.7	30 40	
Clock Input	t_{11-14+} t_{11-14-}	14 14	2.7 2.7	11 11	2.7 2.7	5.0 5.0	9.0 9.0	2.7 2.7	11 11	
Strobe Input	t_{12+14+} t_{12-14-}	14 14	1.6 1.6	8.0 8.0	1.6 1.6	4.0 4.0	7.0 7.0	1.6 1.6	8.0 8.0	
Reset Input	t_{10+14-}	14	2.0	8.0	2.0	5.0	6.5	2.0	8.0	
Hysteresis Mode	t_{7+14+} t_{7-14-}	14 14	6.6 3.7	30 17	6.7 3.7	18 10	25 15	6.6 3.7	30 40	
Setup Time	t_{setup}	14	30		2.7	15		30		
Hold Time	t_{hold}	14	0		–2.0	15		–2.0		
Rise Time	t+	14	1.5	5.0	1.5	2.0	4.3	1.5	5.0	
Fall Time	t–	14	1.5	5.0	1.5	2.0	4.3	1.5	5.0	

1. Pin 5 to V_{EE}, V_{IL} to Data input one at a time.
2. Output latched to logic high state prior to test. V_{IHA}', V_{ILA}' are standard logic 1 and logic 0 MTTL threshold voltages. V_{IHA}'', V_{ILA}'', V_{IHA}''' and V_{ILA}''' are logic 1 and logic 0 threshold voltages in the hysteresis mode as shown in Figure 1 on page 301.
3. Input level on data input taken from +0.4V up to voltage level given.
4. Input level on data input taken from +4.0V down to voltage level given.
5. Operation and limits shown also apply for V_{CC} = +6.0V.

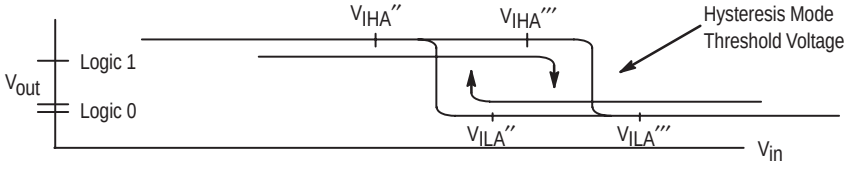


Figure 1. Hysteresis Mode Threshold Voltage

ELECTRICAL CHARACTERISTICS

			TEST VOLTAGE VALUES (Volts)								
			MECL 10,000 INPUT LEVELS				TTL INPUT LEVELS (6.)				
@ Test Temperature			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	$V_{IHA'}$	$V_{ILA'}$	
–30°C			–0.890	–1.890	–1.155	–1.500	3.000	0.400	2.000	0.800	
+25°C			–0.810	–1.850	–1.105	–1.475	3.000	0.400	2.000	0.800	
+85°C			–0.700	–1.825	–1.035	–1.440	3.000	0.400	2.000	0.800	
			TEST VOLTAGE APPLIED TO PINS LISTED BELOW								
Characteristic	Symbol	Pin Under Test	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	$V_{IHA'}$	$V_{ILA'}$	Gnd
Negative Power Supply Drain Current	I_E	8 8	11 11	12 12							1,5,16 1,16
Positive Power Supply Drain Current	I_{CC}	9						4,6,7,13			1,16
Input Current	I_{inH}	4 6 7 10 11 12 13	 10,11 11 12 				4 6 7 13				1,16 1,16 1,16 1,16 1,16 1,16 1,16
	I_{CBO} (1.)	4 6 7 13						4 6 7 13			1,16 1,16 1,16 1,16
	I_{inL}	10 11 12		10 11 12							1,16 1,16 1,16
Output Voltage Logic 1	V_{OH}	2 3 2 3	12 12 12 12	10,11 10,11 10,11 10,11			4 6 4 6				1,16 1,16 1,5,16 1,5,16
Output Voltage Logic 0	V_{OL}	2 3 2 3	12 12 12 12	10,11 10,11 10,11 10,11				4 6 4 6			1,16 1,16 1,5,16 1,5,16
Threshold Voltage Logic 1	V_{OHA}	2 (2.) 2 2 2 2 (3.) 2 (4.)	11,12 10,12 12 12 12	 10,11 10,11 10,11 10,11	 12 	10 11 	4 4 4 	 	 4 	 	1,16 1,16 1,16 1,16 1,5,16 1,5,16
Threshold Voltage Logic 0	V_{OLA}	2 (2.) 2 2 (2.) 2 2 (3.) 2 (4.)	11,12 10,12 12 12 12	 10,11 10,11 10,11 10,11	10 11 	 12 	4 4 4 	 	 	 4 	1,16 1,16 1,16 1,16 1,5,16 1,5,16
Switching Times Propagation Delay			+1.11V	+0.31V	Pulse In	Pulse Out	+5.0V	+2.40V	Figure		+2.0V
Data Input	t_{7+14+} t_{7-14-}	14 14	12 12	10,11 10,11	7 7	14 14			Figure 3 Figure 3		1,16 1,16
Clock Input	t_{11-14+} t_{11-14-}	14 14	12 12	10 10	7,11 7,11	14 14			Figure 6 Figure 6		1,16 1,16
Strobe Input	t_{12+14+} t_{12-14-}	14 14		10,11 10,11	12 12	14 14	7 7		Figure 4 Figure 4		1,16 1,16
Reset Input	t_{10+14-}	14	12		10,11	14	7	7	Figure 5		1,16
Hysteresis Mode	t_{7+14+} t_{7-14-}	14 14	12 12	10,11 10,11	7 7	14 14			Figure 3 Figure 3		1,5,16 1,5,16
Setup Time	t_{setup}	14	12	10	7,11	14			Figure 7		1,16
Hold Time	t_{hold}	14	12	10	7,11	14			Figure 7		1,16
Rise Time	t+	14	12	10,11	7	14			Figure 3		1,16
Fall Time	t–	14	12	10,11	7	14			Figure 3		1,16

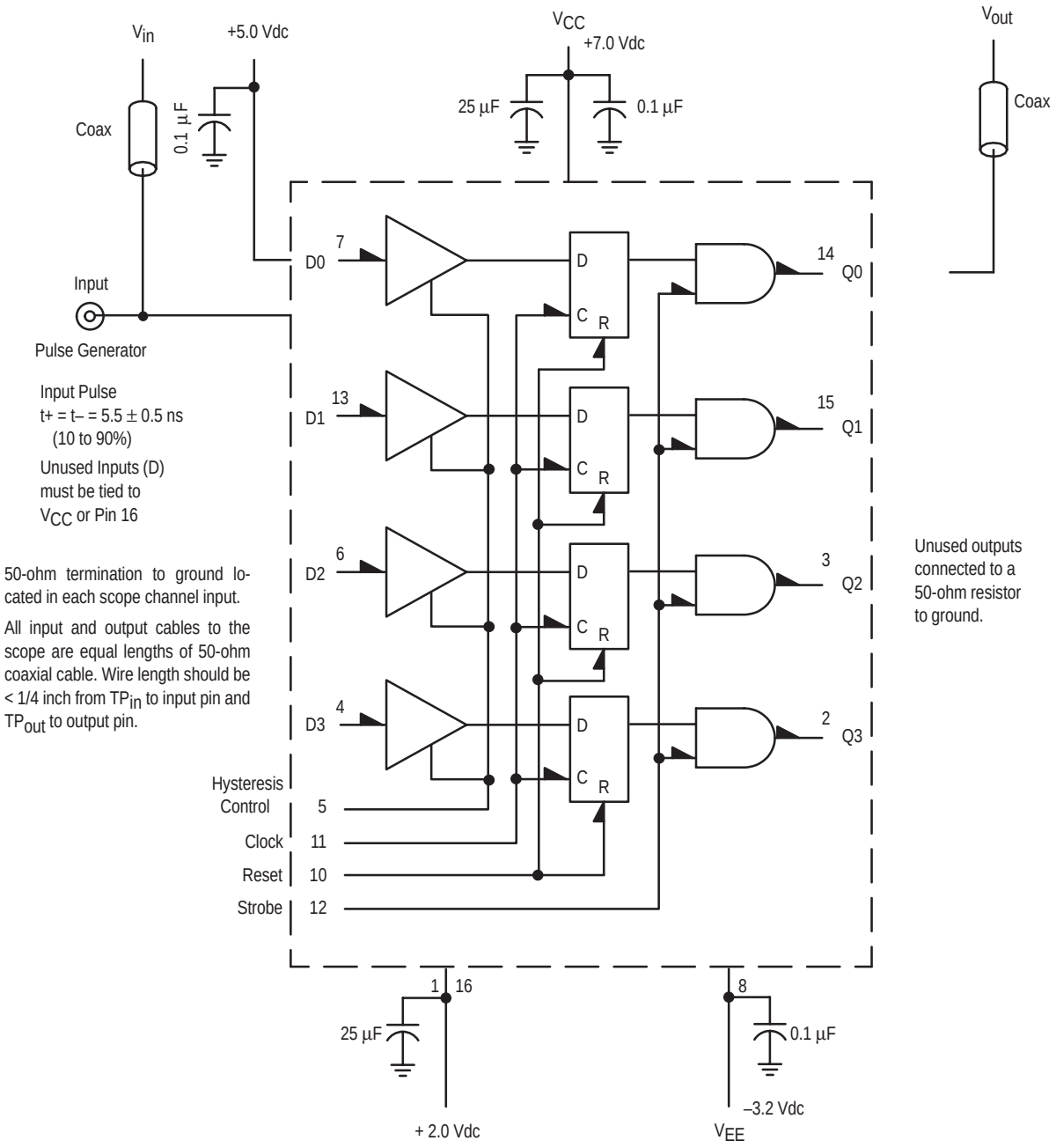
1. Pin 5 to V_{EE}, V_{IL} to Data input one at a time.
2. Output latched to logic high state prior to test. $V_{IHA'}$, $V_{ILA'}$ are standard logic 1 and logic 0 MTTL threshold voltages. $V_{IHA''}$, $V_{ILA''}$, $V_{IHA'''}$ and $V_{ILA'''}$ are logic 1 and logic 0 threshold voltages in the hysteresis mode as shown in Figure 1 on page 301.
3. Input level on data input taken from +0.4V up to voltage level given.
4. Input level on data input taken from +4.0V down to voltage level given.
5. Operation and limits shown also apply for V_{CC} = +6.0V.
6. When testing, choose either TTL or IBM input levels.

ELECTRICAL CHARACTERISTICS

@ Test Temperature			TEST VOLTAGE VALUES (Volts)										
			IBM INPUT LEVELS (6.)				HYSTERESIS MODE						
			V_{IH}	V_{IL}	V_{IHA}'	V_{ILA}'	V_{IHA}''	V_{ILA}''	V_{IHA}'''	V_{ILA}'''	V_{CC} (5.)	V_{EE}	
–30°C			3.11	0.150			2.90	2.00	2.20	1.30	+5.0	–5.2	
+25°C			3.11	0.150	1.700	0.70	2.60	1.70	1.90	1.00	+5.0	–5.2	
+85°C			3.11	0.150			2.30	1.40	1.60	0.70	+5.0	–5.2	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW										Gnd
			V_{IH}	V_{IL}	V_{IHA}'	V_{ILA}'	V_{IHA}''	V_{ILA}''	V_{IHA}'''	V_{ILA}'''	V_{CC} (5.)	V_{EE}	
Negative Power Supply Drain Current	I_E	8 8									9 9	8 5,8	1,5,16 1,16
Positive Power Supply Drain Current	I_{CC}	9		4,6, 7,13							9 9	5,8 5,8	1,16 1,16
Input Current	I_{inH}	4 6 7 10 11 12 13	4 6 7 13								9 9 9 9 9 9 9	8 8 8 8 8 8 8	1,16 1,16 1,16 1,16 1,16 1,16 1,16
	I_{CBO} (1.)	4 6 7 13		4 6 7 13							9 9 9 9	8 8 8 8	1,16 1,16 1,16 1,16
	I_{inL}	10 11 12									9 9 9	8 8 8	1,16 1,16 1,16
Output Voltage Logic 1	V_{OH}	2 3 2 3	4 6 4 6								9 9 9 9	5,8 5,8 8 8	1,16 1,16 1,5,16 1,5,16
Output Voltage Logic 0	V_{OL}	2 3 2 3		4 6 4 6							9 9 9 9	5,8 5,8 8 8	1,16 1,16 1,5,16 1,5,16
Threshold Voltage Logic 1	V_{OHA}	2 (2.) 2 2 2 2 (3.) 2 (4.)	4 4 4		4		4		4		9 9 9 9 9 9	5,8 5,8 5,8 5,8 8 8	1,16 1,16 1,16 1,16 1,5,16 1,5,16
Threshold Voltage Logic 0	V_{OLA}	2 (2.) 2 2 (2.) 2 2 (3.) 2 (4.)	4 4 4			4		4		4	9 9 9 9 9 9	5,8 5,8 5,8 5,8 8 8	1,16 1,16 1,16 1,16 1,5,16 1,5,16
Switching Times Propagation Delay			+5.0V	+2.40V	Figure						+7.0V	–3.2V	+2.0V
Data Input	t_{7+14+} t_{7-14-}	14 14			Figure 3 Figure 3						9 9	5,8 5,8	1,16 1,16
Clock Input	t_{11-14+} t_{11-14-}	14 14			Figure 6 Figure 6						9 9	5,8 5,8	1,16 1,16
Strobe Input	t_{12+14+} t_{12-14-}	14 14	7 7		Figure 4 Figure 4						9 9	5,8 5,8	1,16 1,16
Reset Input	t_{10+14-}	14	7		Figure 5						9	5,8	1,16
Hysteresis Mode	t_{7+14+} t_{7-14-}	14 14			Figure 3 Figure 3						9 9	8 8	1,5,16 1,5,16
Setup Time	t_{setup}	14			Figure 7						9	5,8	1,16
Hold Time	t_{hold}	14			Figure 7						9	5,8	1,16
Rise Time	t+	14			Figure 3						9	5,8	1,16
Fall Time	t–	14			Figure 3						9	5,8	1,16

1. Pin 5 to V_{EE}, V_{IL} to Data input one at a time.
2. Output latched to logic high state prior to test. V_{IHA}', V_{ILA}' are standard logic 1 and logic 0 MTTL threshold voltages. V_{IHA}'', V_{ILA}'', V_{IHA}''' and V_{ILA}''' are logic 1 and logic 0 threshold voltages in the hysteresis mode as shown in Figure 1 on page 301.
3. Input level on data input taken from +0.4V up to voltage level given.
4. Input level on data input taken from +4.0V down to voltage level given.
5. Operation and limits shown also apply for V_{CC} = +6.0V.
6. When testing, choose either TTL or IBM input levels.

Figure 2. SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



NOTE: All power supplies and logic levels are shifted 2 volts positive.

Figure 3 – DATA to OUTPUT
(Clock and Reset are low, Strobe is high)

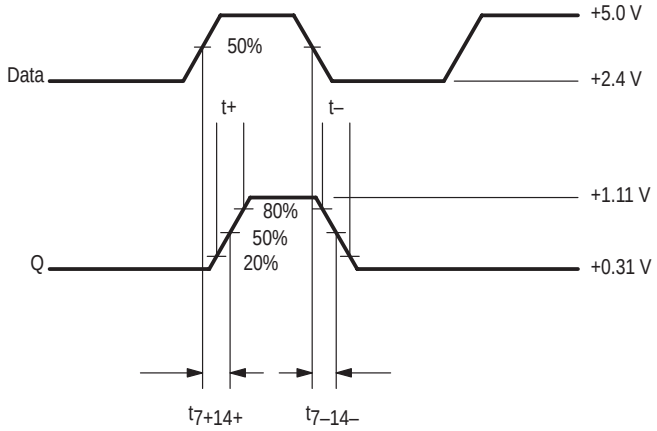


Figure 4 – STROBE to OUTPUT
(Data is high, Clock and Reset are low)

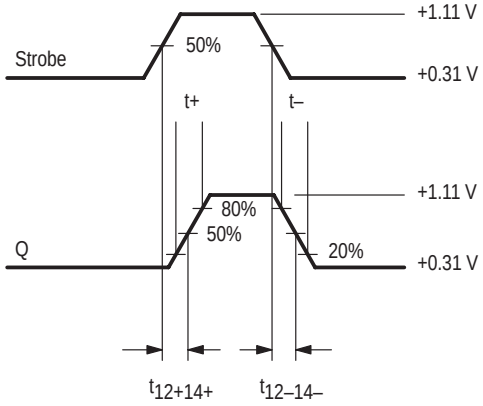


Figure 5 – RESET to OUTPUT
(Data and Strobe are high)

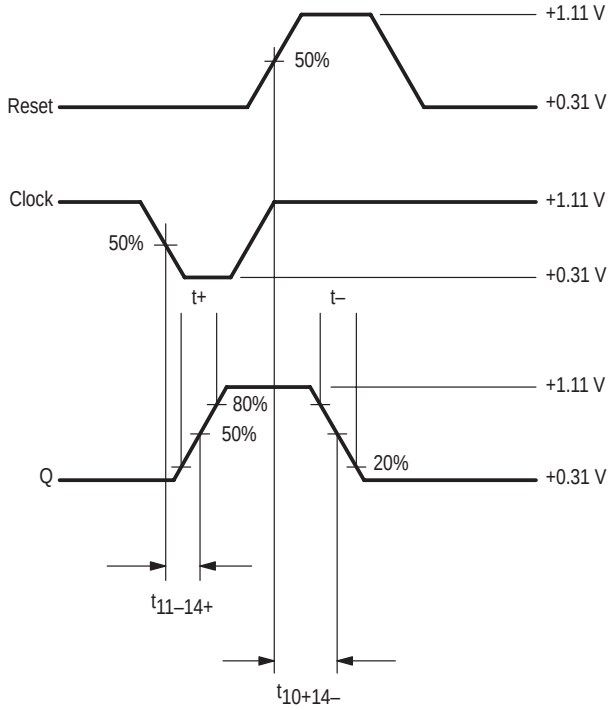


Figure 6 – CLOCK to OUTPUT
(Reset is low, Strobe is high)

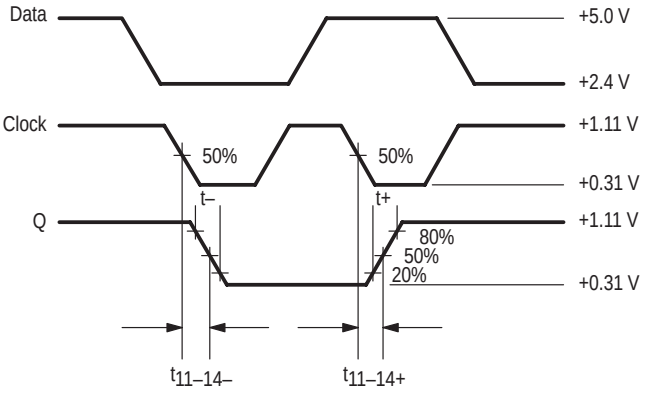
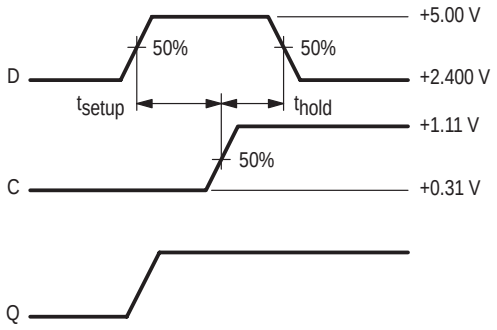


Figure 7 – $T_{SET\ UP}$ AND T_{HOLD} WAVEFORMS



MC10131

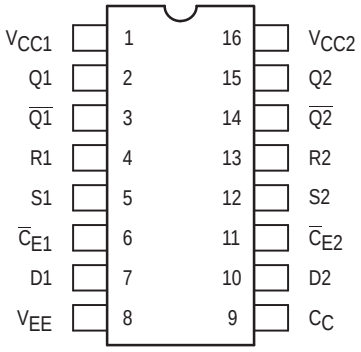
Dual Type D Master-Slave Flip-Flop

The MC10131 is a dual master–slave type D flip–flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable (C_E) inputs. Each flip–flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip–flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip–flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

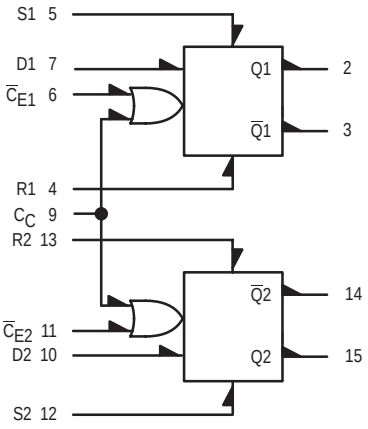
- P_D = 235 mW typ/pkg (No Load)
- F_{Tog} = 160 MHz typ
- t_{pd} = 3.0 ns typ
- t_r, t_f = 2.5 ns typ (20%–80%)

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

LOGIC DIAGRAM

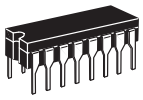


V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

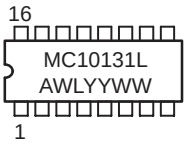
ON Semiconductor

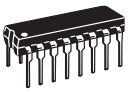
http://onsemi.com

MARKING DIAGRAMS

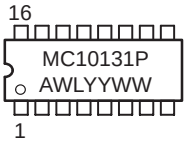


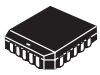
CDIP–16
L SUFFIX
CASE 620



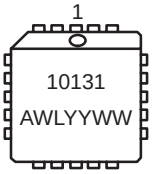


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	X	Q_n
H	L	L
H	H	H

C = C_E + C_C. A clock H is a clock transition from a low to a high state.

R–S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

ORDERING INFORMATION

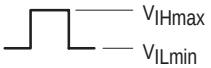
Device	Package	Shipping
MC10131L	CDIP–16	25 Units / Rail
MC10131P	PDIP–16	25 Units / Rail
MC10131FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		62		45	56		62	mAdc
Input Current	I_{inH}	4 5 6 7 9		525 525 350 390 425			330 330 220 245 265		330 330 220 245 265	μAdc
	I_{inL}	4, 5* 6, 7, 9*	0.5 0.5		0.5 0.5			0.3 0.3		μAdc
Output Voltage Logic 1	V_{OH}	2 2†	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3†	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 2†	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3†		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load) Clock Input										ns
Propagation Delay	t_{9+2-} t_{9+2+} t_{6+2+} t_{6+2-}	2 2 2 2	1.7 1.7 1.7 1.7	4.6 4.6 4.6 4.6	1.8 1.8 1.8 1.8	3.0 3.0 3.0 3.0	4.5 4.5 4.5 4.5	1.8 1.8 1.8 1.8	5.0 5.0 5.0 5.0	
Rise Time (20 to 80%)	t_{2+}	2	1.0	4.6	1.1	2.5	4.5	1.1	4.9	
Fall Time (20 to 80%)	t_{2-}	2	1.0	4.6	1.1	2.5	4.5	1.1	4.9	
Set Input										ns
Propagation Delay	t_{5+2+} t_{12+15+} t_{5+3-} t_{12+14-}	2 15 3 14	1.7 1.7 1.7 1.7	4.4 4.4 4.4 4.4	1.8 1.8 1.8 1.8	2.8 2.8 2.8 2.8	4.3 4.3 4.3 4.3	1.8 1.8 1.8 1.8	4.8 4.8 4.8 4.8	
Reset Input										ns
Propagation Delay	t_{4+2-} t_{13+15-} t_{4+3-} t_{13+14+}	2 15 3 14	1.7 1.7 1.7 1.7	4.4 4.4 4.4 4.4	1.8 1.8 1.8 1.8	2.8 2.8 2.8 2.8	4.3 4.3 4.3 4.3	1.8 1.8 1.8 1.8	4.8 4.8 4.8 4.8	
Setup Time	t_{setup}	7	2.5		2.5			2.5		ns
Hold Time	t_{hold}	7	1.5		1.5			1.5		ns
Toggle Frequency (Max)	f_{tog}	2	125		125	160		125		MHz

* Individually test each input applying V_{IH} or V_{IL} to input under test.

† Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ Input (Pin 6)

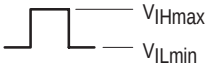


ELECTRICAL CHARACTERISTICS (continued)

			TEST VOLTAGE VALUES (Volts)					
		@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
		–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
		+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
		+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8					8	1, 16
Input Current	I_{inH}	4 5 6 7 9	4 5 6 7 9				8 8 8 8 8	1, 16 1, 16 1, 16 1, 16 1, 16
	I_{inL}	4, 5* 6, 7, 9*		* *			8 8	1, 16 1, 16
Output Voltage Logic 1	V_{OH}	2 2†	5 7				8 8	1, 16 1, 16
Output Voltage Logic 0	V_{OL}	2 3†	5 7				8 8	1, 16 1, 16
Threshold Voltage Logic 1	V_{OHA}	2 2†			5 7	 9	8 8	1, 16 1, 16
Threshold Voltage Logic 0	V_{OLA}	2 3†			5 7	 9	8 8	1, 16 1, 16
Switching Times (50Ω Load) Clock Input			+1.11Vdc		Pulse In	Pulse Out	–3.2 V	+2.0 V
Propagation Delay	t_{9+2-} t_{9+2+} t_{6+2+} t_{6+2-}	2 2 2 2	 7 7 		9 9 6 6	2 2 2 2	8 8 8 8	1, 16 1, 16 1, 16 1, 16
Rise Time (20 to 80%)	t_{2+}	2	7		9	2	8	1, 16
Fall Time (20 to 80%)	t_{2-}	2			9	2	8	1, 16
Set Input								
Propagation Delay	t_{5+2+} t_{12+15+} t_{5+3-} t_{12+14-}	2 15 3 14	 6 9		5 12 5 12	2 15 3 14	8 8 8 8	1, 16 1, 16 1, 16 1, 16
Reset Input								
Propagation Delay	t_{4+2-} t_{13+15-} t_{4+3-} t_{13+14+}	2 15 3 14	 6 9		4 13 4 13	2 15 3 14	8 8 8 8	1, 16 1, 16 1, 16 1, 16
Setup Time	t_{setup}	7			6, 7	2	8	1, 16
Hold Time	t_{hold}	7			6, 7	2	8	1, 16
Toggle Frequency (Max)	f_{tog}	2			6	2	8	1, 16

* Individually test each input applying V_{IH} or V_{IL} to input under test.

† Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ Input (Pin 6)



Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10133

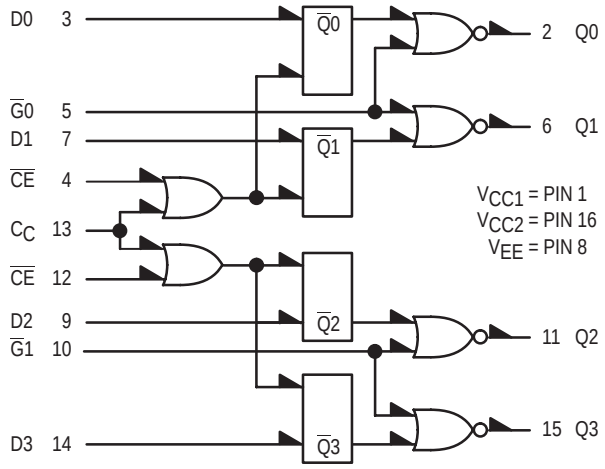
Quad Latch

The MC10133 is a high speed, low power, quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs, allowing direct wiring to a bus. When the clock is high, outputs will follow D inputs. Information is latched on the negative going transition of the clock.

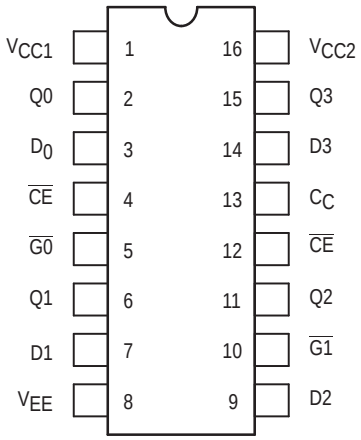
The outputs are gated when the output enable ($\overline{G}$) is low. All four latches may be clocked at one time with the common clock (C_C), or each half may be clocked separately with its clock enable ($\overline{CE}$).

- P_D=310 mW typ/pkg (No Load)
- t_{pd}= 4.0 ns typ
- t_r, t_f= 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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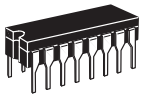
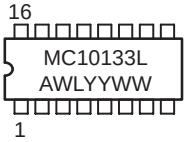
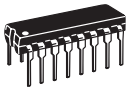
MARKING DIAGRAMS

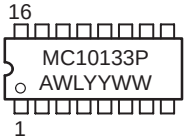


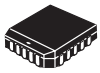
CDIP–16
L SUFFIX
CASE 620



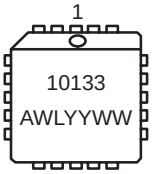


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	X	X	L
L	L	X	Q_n
L	H	L	L
L	H	H	H

$C = C_C = CE$

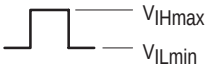
ORDERING INFORMATION

Device	Package	Shipping
MC10133L	CDIP–16	25 Units / Rail
MC10133P	PDIP–16	25 Units / Rail
MC10133FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		82			75		82	mAdc
Input Current	I_{inH}	3		390			245		245	µAdc
		4		425			265		265	
		5		560			350		350	
		13		560			350		350	
	I_{inL}	3	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	2	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	Vdc
		2	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	
Output Voltage Logic 0	V_{OL}	2	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	Vdc
		2	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	
		2	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	
Threshold Voltage Logic 1	V_{OHA}	2	–1.080		–0.980			–0.910		Vdc
		2	–1.080		–0.980			–0.910		
		2	–1.080		–0.980			–0.910		
		2†	–1.080		–0.980			–0.910		
		2‡	–1.080		–0.980			–0.910		
		2‡	–1.080		–0.980			–0.910		
		2	–1.080		–0.980			–0.910		
		2	–1.080		–0.980			–0.910		
Threshold Voltage Logic 0	V_{OLA}	2		–1.655			–1.630		–1.595	Vdc
		2		–1.655			–1.630		–1.595	
		2		–1.655			–1.630		–1.595	
		2†		–1.655			–1.630		–1.595	
		2‡		–1.655			–1.630		–1.595	
		2‡		–1.655			–1.630		–1.595	
Switching Times (50Ω Load)										ns
Propagation Delay	t_{3+2+}	2	1.0	5.6	1.0	4.0	5.4	1.1	5.9	
	t_{4+2+}	2	1.0	5.4	1.0	4.0	5.4	1.2	6.0	
	$t_{5–2+}$	2	1.0	3.2	1.0	2.0	3.1	1.0	3.4	
	t_{setup}	3	2.5		2.5	0.7		2.5		
	t_{hold}	3	1.5		1.5	0.7		1.5		
Rise Time (20 to 80%)	t_{2+}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8	
Fall Time (20 to 80%)	$t_{2–}$	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8	

† Output level to be measured after a clock pulse has been applied to the clock input (Pin 4)



‡ Data input at proper high/low level while clock pulse is high so that device latches ar proper high/low level for test. Levels are measured after device has latched.

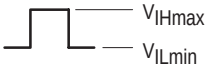
* Latch set to zero state before test.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current		I_E	8		13			8	1, 16
Input Current		I_{inH}	3	3				8	1, 16
			4	4				8	1, 16
			5	5				8	1, 16
			13	13				8	1, 16
		I_{inL}	3		3			8	1, 16
Output Voltage	Logic 1	V_{OH}	2	3, 4				8	1, 16
			2	3, 13				8	1, 16
Output Voltage	Logic 0	V_{OL}	2	13	3			8	1, 16
			2	3, 5, 13				8	1, 16
			2	4	3			8	1, 16
Threshold Voltage	Logic 1	V_{OHA}	2	3, 4			5	8	1, 16
			2	4		3		8	1, 16
			2	3, 4				8	1, 16
			2†	3				8	1, 16
			2‡					8	1, 16
			2‡				4	8	1, 16
			2	3		4		8	1, 16
			2	3		13		8	1, 16
Threshold Voltage	Logic 0	V_{OLA}	2	3, 4		5		8	1, 16
			2	4			3	8	1, 16
			2	4				8	1, 16
			2†					8	1, 16
			2‡	3				8	1, 16
			2‡	3			13	8	1, 16
Switching Times	(50Ω Load)			**+1.11V**		**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay		t_{3+2+}	2	4		3	2	8	1, 16
		t_{4+2+}	2	3*		4	2	8	1, 16
		t_{5-2+}	2			5	2	8	1, 16
		t_{setup}	3			3	2	8	1, 16
		t_{hold}	3			3	2	8	1, 16
Rise Time	(20 to 80%)	t_{2+}	2	4		3	2	8	1, 16
Fall Time	(20 to 80%)	t_{2-}	2	4		3	2	8	1, 16

† Output level to be measured after a clock pulse has been applied to the clock input (Pin 4)



‡ Data input at proper high/low level while clock pulse is high so that device latches ar proper high/low level for test. Levels are measured after device has latched.

* Latch set to zero state before test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10134

Dual Multiplexer With Latch

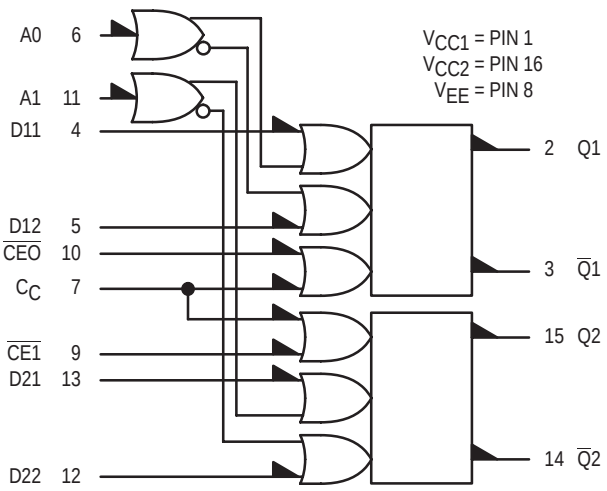
The MC10134 is a dual multiplexer with clocked D type latches. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock (C_C).

The data select inputs determine which data input is enabled. A high (H) level on the A0 input enables data input D12 and a low (L) level on the A0 input enables data input D11. A high (H) level on the A1 input enables data input D22 and a low (L) level on the A1 input enables data input D21.

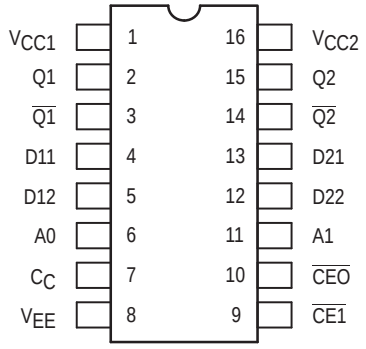
Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

- P_D = 225 mW typ/pkg (No Load)
- t_{pd} = 3.0 ns typ
- t_r, t_f = 2.5 ns typ (20%–80%)

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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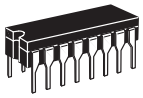
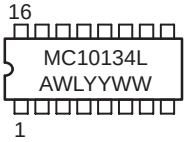
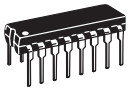
MARKING DIAGRAMS

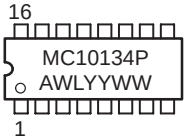


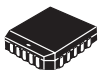
CDIP–16
L SUFFIX
CASE 620



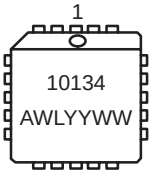


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

TRUTH TABLE

C	A0	D11	D12	Q_{n+1}
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Q_n

$C = \overline{C}_E + C_C$

ORDERING INFORMATION

Device	Package	Shipping
MC10134L	CDIP–16	25 Units / Rail
MC10134P	PDIP–16	25 Units / Rail
MC10134FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		60			55		60	mAdc
Input Current	I_{inH}	4 5 6 7 10		460 460 425 460 425			290 290 265 290 265		290 290 265 290 265	µAdc
	I_{inL}	4*	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	2 2	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 2	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 2	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 2		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay Data	t_{4+2+}	2	1.0	3.5	1.0		3.3	1.0	3.6	
Clock	t_{10-2+}	2	1.0	6.0	1.0		5.7	1.0	6.3	
Select	t_{6+2+}	2	1.0	4.8	1.0		4.6	1.0	5.0	
Setup Time Data	t_{setup}	2	2.5		2.5			2.5		
Select	t_{setup}	2	3.5		3.5			3.5		
Hold Time Data	t_{hold}	2	1.5		1.5			1.5		
Select	t_{hold}	2	1.0		1.0			1.0		
Rise Time (20 to 80%)	t_{2+}	2	1.5	3.7	1.5		3.5	1.5	3.8	
Fall Time (20 to 80%)	t_{2-}	2	1.5	3.7	1.5		3.5	1.5	3.8	

* All other inputs tested in the same manner.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

TEST VOLTAGE VALUES (Volts)

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	4 5 6 7 10	4 5 6 7 10				8 8 8	1, 16 1, 16 1, 16
		I_{inL}	4*		4			8	1, 16
Output Voltage	Logic 1	V_{OH}	2 2	4 5,6	6,7,10 7,10			8 8	1, 16 1, 16
Output Voltage	Logic 0	V_{OL}	2 2	 6	4,6,7,10 5,7,10			8 8	1, 16 1, 16
Threshold Voltage	Logic 1	V_{OHA}	2 2	 6	6,7,10 7,10	4 5		8 8	1, 16 1, 16
Threshold Voltage	Logic 0	V_{OLA}	2 2	 6	6,7,10 7,10		4 5	8 8	1, 16 1, 16
Switching Times	(50Ω Load)			**+1.11 V**	**+0.31 V**	**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	Data	t_{4+2+}	2		6,7,10	4	2	8	1, 16
	Clock	t_{10-2+}	2	4	7	10	2	8	1, 16
	Select	t_{6+2+}	2	5	7,10	6	2	8	1, 16
Setup Time	Data	t_{setup}	2		6,7	4,10	2	8	1, 16
	Select	t_{setup}	2	5	7,11	6,10	2	8	1, 16
Hold Time	Data	t_{hold}	2		6,7	4,10	2	8	1, 16
	Select	t_{hold}	2	5	7,11	6,10	2	8	1, 16
Rise Time	(20 to 80%)	t_{2+}	2		6,7,10	4	2	8	1, 16
Fall Time	(20 to 80%)	t_{2-}	2		6,7,10	4	2	8	1, 16

* All other inputs tested in the same manner.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10135

Dual J-K Master-Slave Flip-Flop

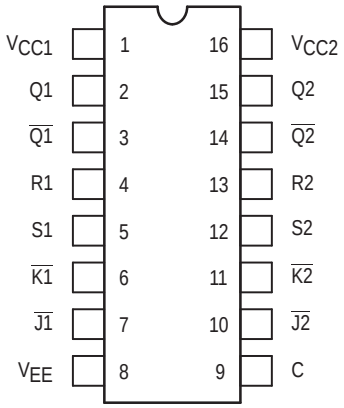
The MC10135 is a dual master–slave dc coupled J–K flip–flop. Asynchro– nous set (S) and reset (R) are provided. The set and reset inputs override the clock.

A common clock is provided with separate $\overline{J}$–$\overline{K}$ inputs. When the clock is static, the $\overline{J}$–$\overline{K}$ inputs do not effect the output.

The output states of the flip–flop change on the positive transition of the clock.

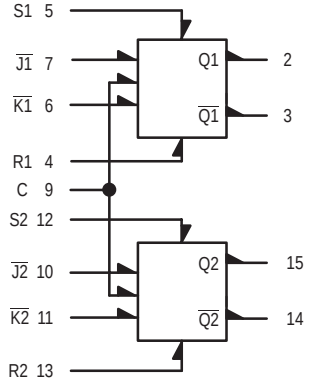
- P_D = 280 mW typ/pkg (No Load)
- f_{Tog} = 140 MHz typ
- t_{pd} = 3.0 ns typ
- t_r, t_f = 2.5 ns typ (20%–80%)

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

R–S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

CLOCK J–K TRUTH TABLE*

$\overline{J}$	$\overline{K}$	Q_{n+1}
L	L	$\overline{Q_n}$
H	L	L
L	H	H
H	H	Q_n

*Output states change on positive transition of clock for $\overline{J}$–$\overline{K}$ input condition present.

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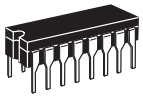
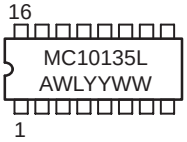
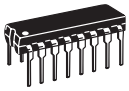
MARKING DIAGRAMS

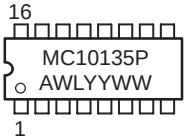


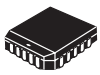
CDIP–16
L SUFFIX
CASE 620



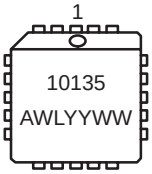


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

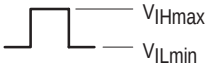
ORDERING INFORMATION

Device	Package	Shipping
MC10135L	CDIP–16	25 Units / Rail
MC10135P	PDIP–16	25 Units / Rail
MC10135FN	PLCC–20	46 Units / Rail

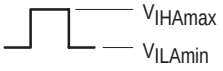
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		75		54	68		75	mAdc
Input Current	I_{inH}	6,7,9,10,11 4,5,12,13		425 620			265 390		265 390	μAdc
	I_{inL}	4,5,6,7,9, 10,11,12,13	0.5 0.5		0.5 0.5			0.3 0.3		μAdc
Output Voltage Logic 1	V_{OH}	2 2 (**3.**)	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	3 3 (**3.**)	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 2 (**4.**)	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	3 3 (**4.**)		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load) Clock Input										ns
Propagation Delay	t_{9+2+} t_{9+2-}	2 2	1.8 1.8	5.0 5.0	1.8 1.8	3.0 3.0	4.5 4.5	1.8 1.8	4.6 4.6	
Rise Time (20 to 80%)	t_{2+}, t_{3+}	2, 3	1.1	4.8	1.1	2.0	4.5	1.1	4.7	
Fall Time (20 to 80%)	t_{2-}, t_{3-}	2, 3	1.1	4.8	1.1	2.0	4.5	1.1	4.7	
Set Input										ns
Propagation Delay	t_{5+2+} t_{12+15+} t_{5+3-} t_{12+14-}	2 15 3 14	1.8 1.8 1.8 1.8	5.6 5.6 5.6 5.6	1.8 1.8 1.8 1.8	3.0 3.0 3.0 3.0	5.0 5.0 5.0 5.0	1.8	5.2 5.2 5.2 5.2	
Reset Input										ns
Propagation Delay	t_{4+2-} t_{4+3-} t_{13+15-} t_{13+14+}	2 3 15 14	1.8 1.8 1.8 1.8	5.6 5.6 5.6 5.6	1.8 1.8 1.8 1.8	3.0 3.0 3.0 3.0	5.0 5.0 5.0 5.0	1.8 1.8 1.8 1.8	5.2 5.2 5.2 5.2	
Setup Time	t_{setup}	7	2.5		2.5	1.0		2.5		ns
Hold Time	t_{hold}	7	1.5		1.5	1.0		2.5		ns
Toggle Frequency (Max)	f_{tog}	2	125		125	140		125		MHz

1. Individually test each input; apply V_{IHmax} to pin under test.
2. Individually test each input; apply V_{ILmin} to pin under test.
3. Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ Input (Pin 6)



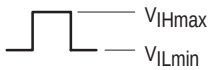
4. Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ Input (Pin 6)



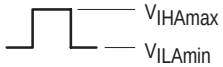
ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C			–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C			–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C			–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic	**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					**(V_{CC}) Gnd**
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8					8	1, 16
Input Current	I_{inH}	6,7,9,10,11 4,5,12,13	Note 1. Note 1.				8 8	1, 16 1, 16
	I_{inL}	4,5,6,7,9, 10,11,12,13		Note 2. Note 2.			8 8	1, 16 1, 16
Output Voltage Logic 1	V_{OH}	2 2 (**3.**)	5 6				8 8	1, 16 1, 16
Output Voltage Logic 0	V_{OL}	3 3 (**3.**)	5 6				8 8	1, 16 1, 16
Threshold Voltage Logic 1	V_{OHA}	2 2 (**4.**)	 6		5		8 8	1, 16 1, 16
Threshold Voltage Logic 0	V_{OLA}	3 3 (**4.**)	 6		5		8 8	1, 16 1, 16
Switching Times (50Ω Load) Clock Input					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	t_{9+2+} t_{9+2-}	2 2			9 9	2 2	8 8	1, 16 1, 16
Rise Time (20 to 80%)	t_{2+}, t_{3+}	2, 3			9	2, 3	8	1, 16
Fall Time (20 to 80%)	t_{2-}, t_{3-}	2, 3			9	2, 3	8	1, 16
Set Input Propagation Delay	t_{5+2+} t_{12+15+} t_{5+3-} t_{12+14-}	2 15 3 14			5 12 5 12	2 15 3 14	8 8 8 8	1, 16 1, 16 1, 16 1, 16
Reset Input Propagation Delay	t_{4+2-} t_{4+3-} t_{13+15-} t_{13+14+}	2 3 15 14			4 4 13 13	2 3 15 14	8 8 8 8	1, 16 1, 16 1, 16 1, 16
Setup Time	t_{setup}	7			6, 9	2	8	1, 16
Hold Time	t_{hold}	7			6, 9	2	8	1, 16
Toggle Frequency (Max)	f_{tog}	2			9	2	8	1, 16

1. Individually test each input; apply V_{IHmax} to pin under test.
2. Individually test each input; apply V_{ILmin} to pin under test.
3. Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ Input (Pin 6)



4. Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ Input (Pin 6)



Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10136

Universal Hexadecimal Counter

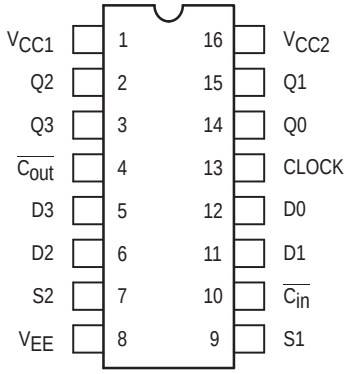
The MC10136 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. The flexibility of this device allows the designer to use one basic counter for most applications, and the synchronous count feature makes the MC10136 suitable for either computers or instrumentation.

Three control lines (S1, S2, and Carry In) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. Carry Out goes low on the terminal count, or when the counter is being preset.

This device is not designed for use with gated clocks. Control is via S1 and S2.

- P_D = 625 mW typ/pkg (No Load)
- f_{count} = 150 MHz typ
- t_{pd} = 3.3 ns typ (C-Q)
- 7.0 ns typ (C-C_{out})
- 5.0 ns typ ($\overline{C_{in}}$-C_{out})

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

FUNCTION TABLE

$\overline{C_{in}}$	S1	S2	Operating Mode
X	L	L	Preset (Program)
L	L	H	Increment (Count Up)
H	L	H	Hold Count
L	H	L	Decrement (Count Down)
H	H	L	Hold Count
X	H	H	Hold (Stop Count)

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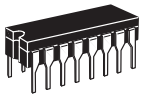
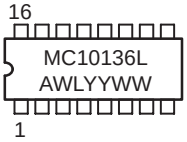
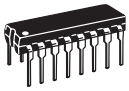
MARKING DIAGRAMS

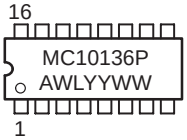


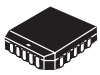
CDIP–16
L SUFFIX
CASE 620



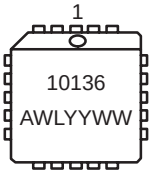


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

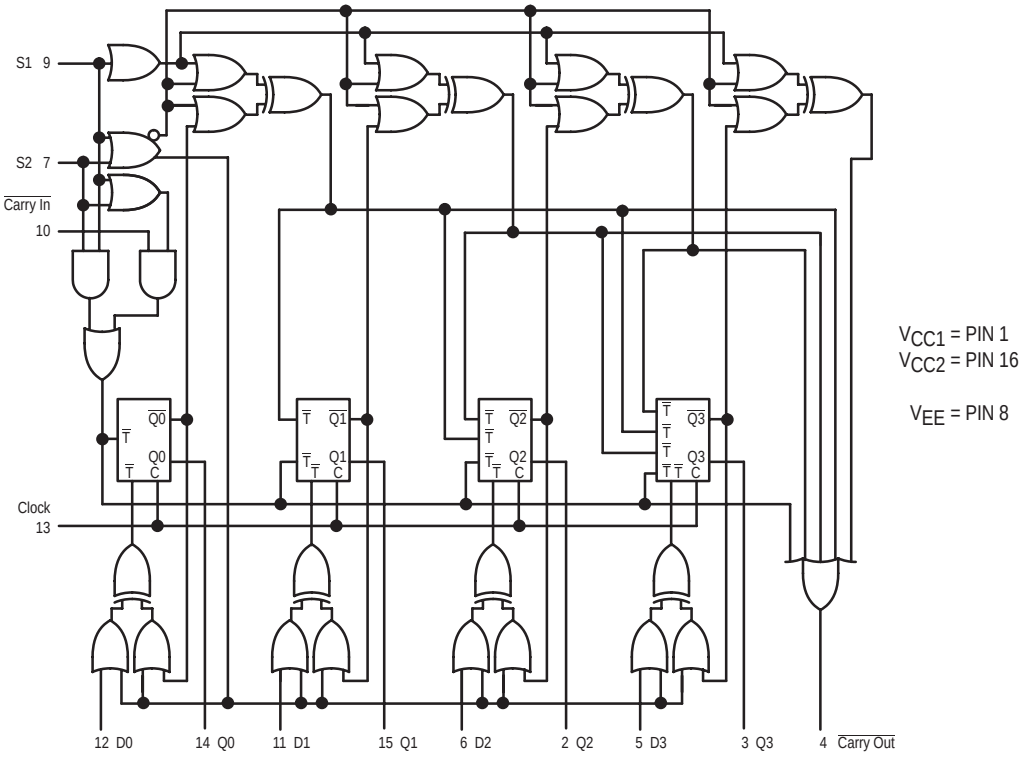


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10136L	CDIP–16	25 Units / Rail
MC10136P	PDIP–16	25 Units / Rail
MC10136FN	PLCC–20	46 Units / Rail

LOGIC DIAGRAM



NOTE: Flip-flops will toggle when all $\overline{T}$ inputs are low.

SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	L	L	H	H	X	H	L	L	H	H	L
L	H	X	X	X	X	L	H	H	L	H	H	H
L	H	X	X	X	X	L	H	L	H	H	H	H
L	H	X	X	X	X	L	H	H	H	H	H	L
L	H	X	X	X	X	H	L	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H
H	H	X	X	X	X	X	H	H	H	H	H	H
L	L	H	H	L	L	X	H	H	H	L	L	L
H	L	X	X	X	X	L	H	L	H	L	L	H
H	L	X	X	X	X	L	H	H	L	L	L	H
H	L	X	X	X	X	L	H	L	L	L	L	L
H	L	X	X	X	X	L	H	H	H	H	H	H

* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.
** A clock H is defined as a clock input transition from a low to a high logic level.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		138		100	125		138	mAdc
Input Current	I_{inH}	5,6,11,12 7 9,10 13		350 425 390 460			220 265 245 290		220 265 245 290	µAdc
	I_{inL}	All	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	14 (2.)	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	Vdc
Output Voltage Logic 0	V_{OL}	14 (2.)	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	14 (2.)	–1.080		–0.980			–0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	14 (2.)		–1.655			–1.630		–1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay Clock Input	t_{13+14+} t_{13+14-} t_{13+4+} t_{13+4-}	14 14 4 4	0.8 0.8 2.0 2.0	4.8 4.8 10.9 10.9	1.0 1.0 2.5 2.5	3.3 3.3 7.0 7.0	4.5 4.5 10.5 10.5	1.4 1.4 2.4 2.4	5.0 5.0 11.5 11.5	
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	t_{10-4-} t_{10+4+}	4 (3.) 4	1.6 1.6	7.4 7.4	1.6 1.6	5.0 5.0	6.9 6.9	1.9 1.9	7.5 7.5	
Setup Time Data Inputs	t_{12+13+} t_{12-13+}	14 14	3.5 3.5		3.5 3.5			3.5 3.5		
Select Inputs	t_{9+13+} t_{7+13+}	14 14	6.0 6.0		6.0 6.0			6.0 6.0		
$\overline{\text{Carry In}}$ Input	t_{10-13+} t_{10+13+}	14 14	2.5 1.5		2.5 1.5			3.0 1.5		
Hold Time Data Inputs	t_{13+12+} t_{13+12-}	14 14	0 0		0 0			0 0		
Select Inputs	t_{13+9+} t_{13+7+}	14 14	–1.0 –1.0		–1.0 –1.0			–1.0 –1.0		
$\overline{\text{Carry In}}$ Input	t_{13+10-} t_{13+10+}	14 14	0 0		0 0			0 0		
Counting Frequency	$f_{countup}$ $f_{countdown}$	14 14	125 125		125 125	150 150		125 125		MHz
Rise Time (20 to 80%)	t_{4+} t_{14+}	4 14	0.9 0.9	3.3 3.3	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.5 3.5	ns
Fall Time (20 to 80%)	t_{4-} t_{14-}	4 14	0.9 0.9	3.3 3.3	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.5 3.5	

1. Individually test each input; apply V_{ILmin} to pin under test.
2. Measure output after clock pulse V_{IL} ⟋ V_{IH} appears at clock input (Pin 13).
3. Before test set all Q outputs to a logic high.
4. To preserve reliable performance, the MC10136 (plastic packaged device only) is to be operated in ambient temperatures above 70°C only when 500lfpm blown air or equivalent heat sinking is provided.

ELECTRICAL CHARACTERISTICS (continued)

				TEST VOLTAGE VALUES (Volts)					
			@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
			–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
			+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
			+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	5,6,11,12 7 9,10 13	5,6,11,12 7 9,10 13				8 8 8 8	1, 16 1, 16 1, 16 1, 16
		I_{inL}	All		Note 1.			8	1, 16
Output Voltage	Logic 1	V_{OH}	14 (2.)	12	7, 9			8	1, 16
Output Voltage	Logic 0	V_{OL}	14 (2.)		7, 9			8	1, 16
Threshold Voltage	Logic 1	V_{OHA}	14 (2.)		7, 9	12		8	1, 16
Threshold Voltage	Logic 0	V_{OLA}	14 (2.)		7, 9		12	8	1, 16
Switching Times	(50Ω Load)			**+1.11V**	**+0.31V**	**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	Clock Input	t_{13+14+}	14	12		13	14	8	1, 16
		t_{13+14-}	14			13	14	8	1, 16
		t_{13+4+}	4	7		13	4	8	1, 16
		t_{13+4-}	4	7		13	4	8	1, 16
	$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	t_{10-4-}	4 (3.)	7	13	10	4	8	1, 16
		t_{10+4+}	4	7	13	10	4	8	1, 16
Setup Time	Data Inputs	t_{12+13+}	14		7, 9	12, 13	14	8	1, 16
		t_{12-13+}	14		7, 9	12, 13	14	8	1, 16
	Select Inputs	t_{9+13+}	14			9, 13	14	8	1, 16
		t_{7+13+}	14			7, 13	14	8	1, 16
	$\overline{\text{Carry In}}$ Inputs	t_{10-13+}	14	7	9	10, 13	14	8	1, 16
		t_{10+13+}	14	7	9	10, 13	14	8	1, 16
Hold Time	Data Inputs	t_{13+12+}	14		7, 9	12, 13	14	8	1, 16
		t_{13+12-}	14		7, 9	12, 13	14	8	1, 16
	Select Inputs	t_{13+9+}	14			9, 13	14	8	1, 16
		t_{13+7+}	14			7, 13	14	8	1, 16
	$\overline{\text{Carry In}}$ Inputs	t_{13+10-}	14	7	9	10, 13	14	8	1, 16
		t_{13+10+}	14	7		10, 13	14	8	1, 16
Counting Frequency		$f_{countup}$	14	7		13	14	8	1, 16
		$f_{countdown}$	14	9		13	14	8	1, 16
Rise Time	(20 to 80%)	t_{4+}	4	7		13	4	8	1, 16
		t_{14+}	14	7		13	14	8	1, 16
Fall Time	(20 to 80%)	t_{4-}	4	7		13	4	8	1, 16
		t_{14-}	14	7		13	14	8	1, 16

1. Individually test each input; apply V_{ILmin} to pin under test.
2. Measure output after clock pulse  appears at clock input (Pin 13).

3. Before test set all Q outputs to a logic high.
4. To preserve reliable performance, the MC10136 (plastic packaged device only) is to be operated in ambient temperatures above 70°C only when 500lfpm blown air or equivalent heat sinking is provided.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

NOTE:

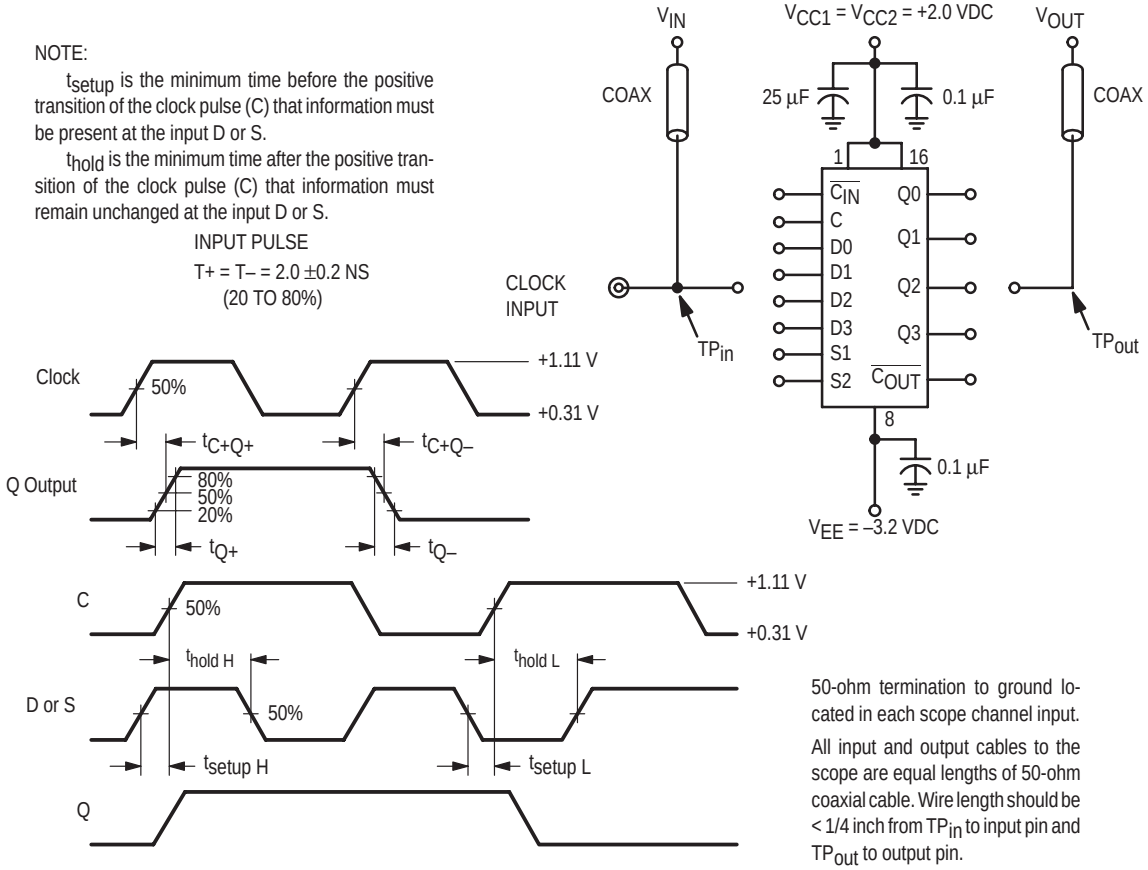
t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S.

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.

INPUT PULSE

T+ = T– = 2.0 ±0.2 NS

(20 TO 80%)

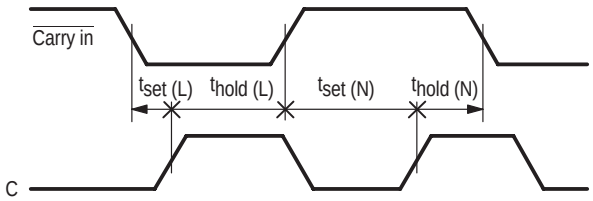


50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs are connected to a 50-ohm resistor to ground.

$\overline{\text{CARRY IN}}$ SET UP AND HOLD TIMES



APPLICATIONS INFORMATION

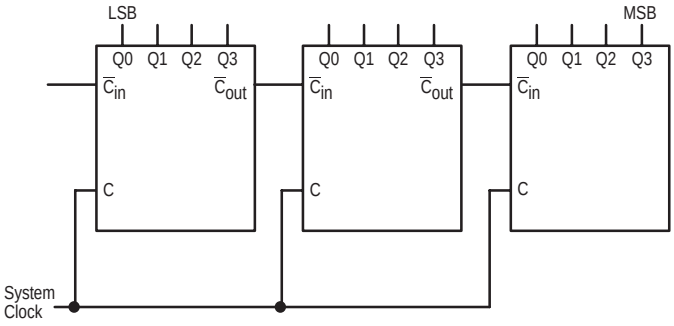
To provide more than four bits of counting capability several MC10136 counters may be cascaded. The Carry In input overrides the clock when the counter is either in the increment mode or the decrement mode of operation. This input allows several devices to be cascaded in a fully synchronous multistage counter as illustrated in Figure 1. The carry is advanced between stages as shown with no external gating. The Carry In of the first device may be left open. The system clock is common to all devices.

The various operational modes of the counter make it useful for a wide variety of applications. If used with MECL III devices, prescalers with input toggle frequencies in excess of 300 MHz are possible. Figure 2 shows such a prescaler using the MC10136 and MC1670. Use of the MC10231 in place of the MC1670 permits 200 MHz operation.

The MC10136 may also be used as a programmable counter. The configuration of Figure 3 requires no additional gates, although maximum frequency is limited to about 50 MHz. The divider modulus is equal to the program input plus one (M = N + 1), therefore, the counter will divide by a modulus varying from 1 to 16.

A second programmable configuration is also illustrated in Figure 4. A pulse swallowing technique is used to speed the counter operation up to 110 MHz typically. The divider modulus for this figure is equal to the program input (M = N). The minimum modulus is 2 because of the pulse swallowing technique, and the modulus may vary from 2 to 15. This programmable configuration requires an additional gate, such as $^{1}/_{2}$MC10109 and a flip-flop such as $^{1}/_{2}$MC10131.

Figure 1. 12 BIT SYNCHRONOUS COUNTER



NOTE: S1 and S2 are set either for increment or decrement operation.

Figure 2. 300 MHz PRESCALER

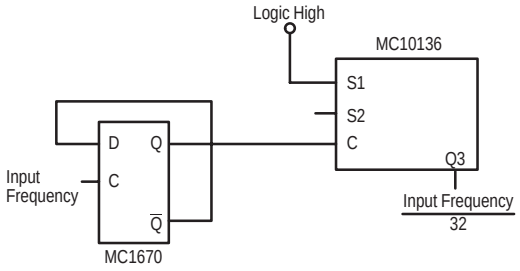
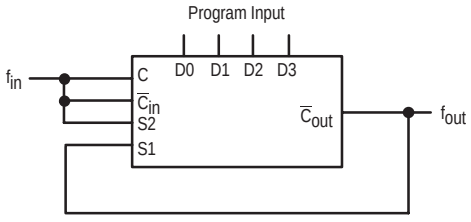


Figure 3. 50 MHz PROGRAMMABLE COUNTER

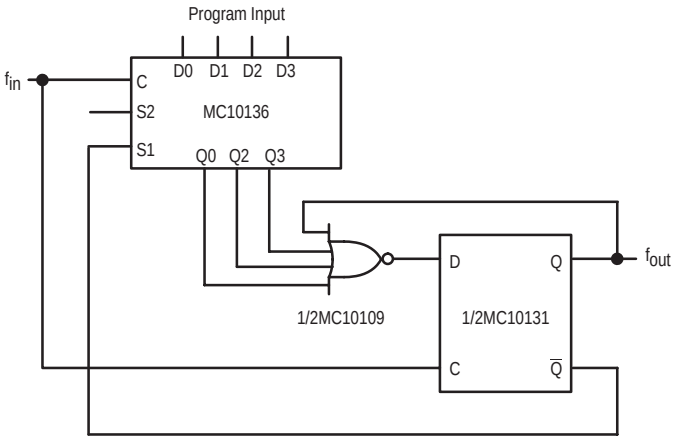


1 $f_{out} = \dfrac{f_{in}}{\text{Program Input} + 1}$

2 $f_{max} \cong$ 50 MHz Typ.

3 Divide Ratio is from 1 to 16.

Figure 4. 100 MHz PROGRAMMABLE COUNTER



1 $f_{out} = \dfrac{f_{in}}{\text{Program Input}}$

2 $f_{max} \cong$ 110 MHz Typ.

3 Divide Ratio is from 2 to 15.

MC10137

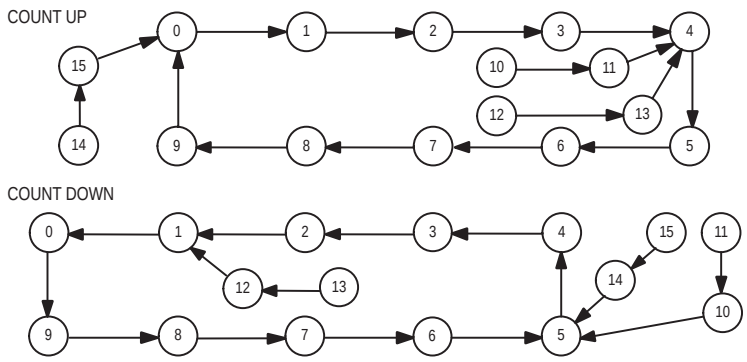
Universal Decade Counter

The MC10137 is a high speed synchronous counter that can count up, down, preset, or stop count at frequencies exceeding 100 MHz. The flexibility of this device allows the designer to use one basic counter for most applications. The synchronous count feature makes the MC10137 suitable for either computers or instrumentation.

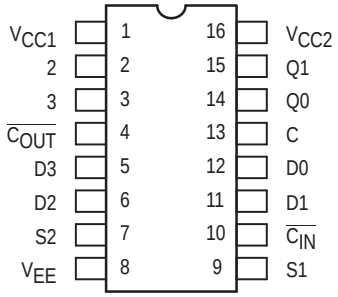
Three control lines (S1, S2, and $\overline{\text{Carry In}}$) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. $\overline{\text{Carry Out}}$ goes low on the terminal count. The $\overline{\text{Carry Out}}$ on the MC10137 is partially decoded from Q1 and Q2 directly, so in the preset mode the condition of the $\overline{\text{Carry Out}}$ after the Clock's positive excursion will depend on the condition of Q1 and/or Q2. The counter changes state only on the positive going edge of the clock. Any other input may change at any time except during the positive transition of the clock. The sequence for counting out of improper states is as shown in the State Diagrams.

- P_D = 625 mW typ/pkg (No Load)
- f_{count} = 150 MHz typ
- t_{pd} = 3.3 ns typ (C–Q)
- = 7.0 ns typ (C–$\overline{C}_{out}$)
- = 5.0 ns typ ($\overline{C}_{in}$–$\overline{C}_{out}$)

STATE DIAGRAMS



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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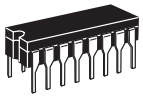
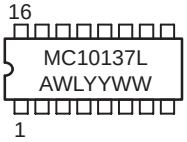
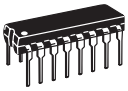
MARKING DIAGRAMS

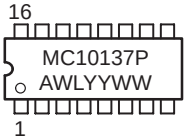


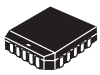
CDIP–16
L SUFFIX
CASE 620



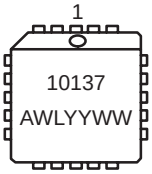


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

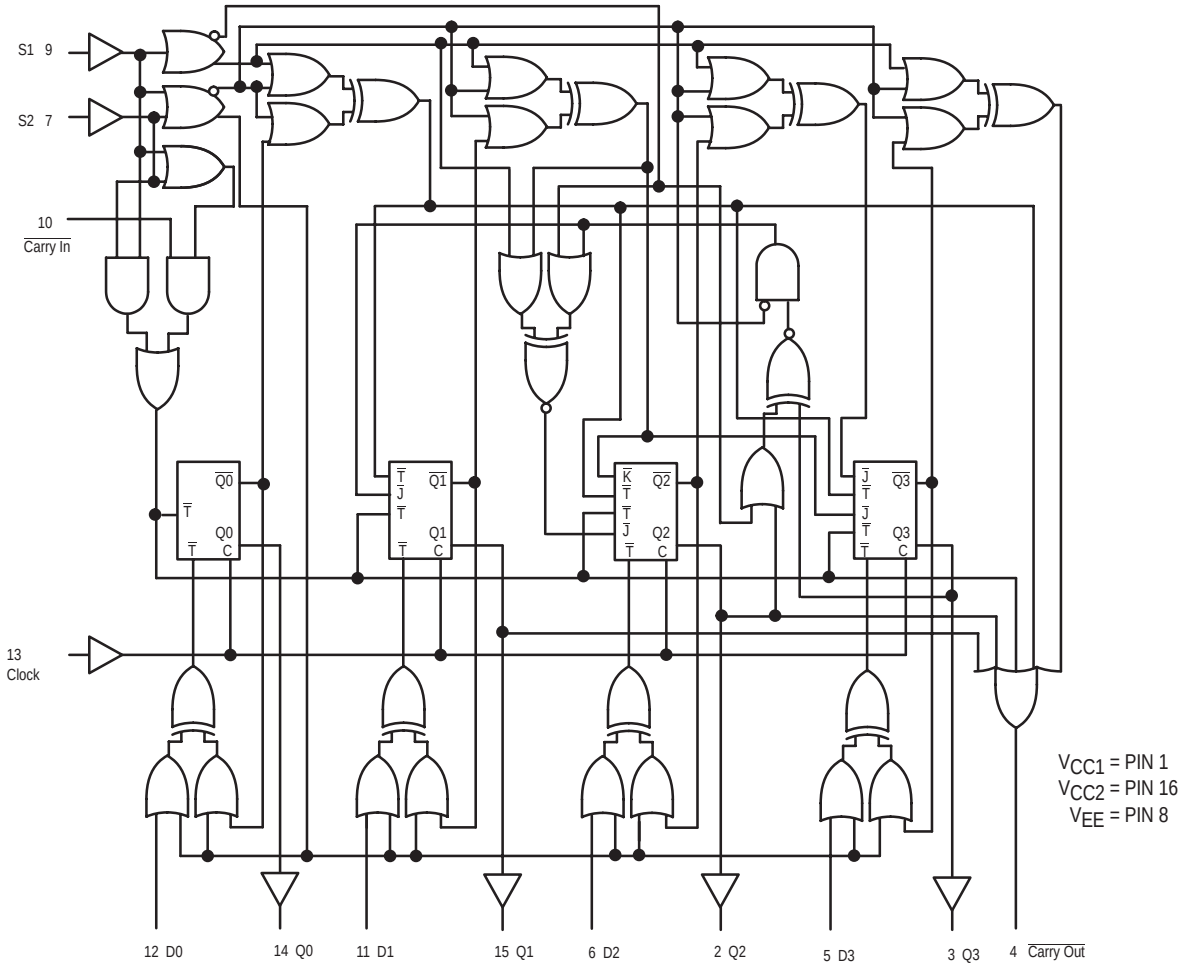
FUNCTION SELECT TABLE

S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

ORDERING INFORMATION

Device	Package	Shipping
MC10137L	CDIP–16	25 Units / Rail
MC10137P	PDIP–16	25 Units / Rail
MC10137FN	PLCC–20	46 Units / Rail

LOGIC DIAGRAM



NOTE: Flip–flops will toggle when all $\overline{T}$ inputs are low.

SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	H	H	H	L	X	H	H	H	H	L	H
L	H	X	X	X	X	L	H	L	L	L	H	H
L	H	X	X	X	X	L	H	H	L	L	H	L
L	H	X	X	X	X	L	H	L	L	L	L	H
L	H	X	X	X	X	L	H	H	L	L	L	H
L	H	X	X	X	X	H	L	H	L	L	L	H
L	H	X	X	X	X	H	H	H	L	L	L	H
H	H	X	X	X	X	X	H	H	L	L	L	H
L	L	H	H	L	L	X	H	H	H	L	L	H
H	L	X	X	X	X	L	H	L	H	L	L	H
H	L	X	X	X	X	L	H	H	L	L	L	H
H	L	X	X	X	X	L	H	L	L	L	L	L

* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.
** A clock H is defined as a clock input transition from a low to a high logic level.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		165		120	150		165	mAdc
Input Current	I_{inH}	5,6,11,12 7 9,10 13		350 425 390 460			220 265 245 290		220 265 245 290	µAdc
	I_{inL}	All	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	14 (2.)	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	Vdc
Output Voltage Logic 0	V_{OL}	14 (2.)	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	14 (2.)	–1.080		–0.980			–0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	14 (2.)		–1.655			–1.630		–1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay Clock Input	t_{13+14+} t_{13+14-} t_{13+4+} t_{13+4-}	14 14 4 4	0.8 0.8 2.0 2.0	4.8 4.8 10.9 10.9	1.0 1.0 2.5 2.5	3.3 3.3 7.0 7.0	4.5 4.5 10.5 10.5	1.1 1.1 2.4 2.4	5.0 5.0 11.5 11.5	
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	t_{10-4-} t_{10+4+}	4 (3.) 4	1.6 1.6	7.4 7.4	1.6 1.6	5.0 5.0	6.9 6.9	1.9 1.9	7.5 7.5	
Setup Time Data Inputs	t_{12+13+} t_{12-13+}	14 14	3.5 3.5		3.5 3.5			3.5 3.5		
Select Inputs	t_{9+13+} t_{7+13+}	14 14	7.5 7.5		7.5 7.5			7.5 7.5		
$\overline{\text{Carry In}}$ Input	t_{10-13+} t_{13+10+}	14 14	4.5 –1.0		3.7 –1.0			4.5 –1.0		
Hold Time Data Inputs	t_{13+12+} t_{13+12-}	14 14	0 0		0 0			0 0		
Select Inputs	t_{13+9+} t_{13+7+}	14 14	–2.5 –2.5		–2.5 –2.5			–2.5 –2.5		
$\overline{\text{Carry In}}$ Input	t_{13+10-} t_{10+13+}	14 14	–1.6 4.0		–1.6 3.1			–1.6 4.0		
Counting Frequency	$f_{countup}$ $f_{countdown}$	14 14	125 125		125 125	150 150		125 125		MHz
Rise Time (20 to 80%)	t_{4+} t_{14+}	4 14	0.9 0.9	3.3 3.3	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.5 3.5	ns
Fall Time (20 to 80%)	t_{4-} t_{14-}	4 14	0.9 0.9	3.3 3.3	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.5 3.5	

1. Individually apply V_{ILmin} to pin under test.
2. Measure output after clock pulse V_{IL} ⟋ V_{IH} appears at clock input (Pin 13).
3. Before test set Q1 and Q2 outputs to a logic low.

ELECTRICAL CHARACTERISTICS (continued)

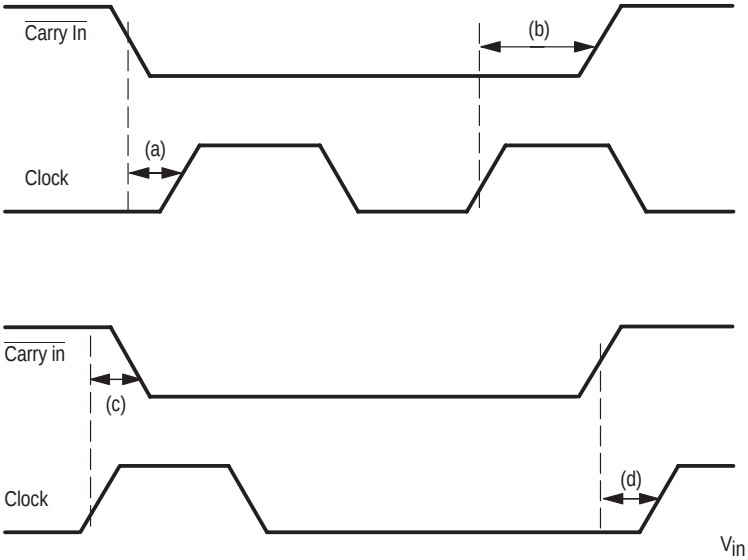
@ Test Temperature			TEST VOLTAGE VALUES (Volts)					
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C			–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C			–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C			–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					**(V_{CC}) Gnd**
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	5,6,11,12 7 9,10 13	5,6,11,12 7 9,10 13				8 8 8 8	1, 16 1, 16 1, 16 1, 16
		I_{inL}	All		Note 1.			8	1, 16
Output Voltage	Logic 1	V_{OH}	14 (2.)	12	7, 9			8	1, 16
Output Voltage	Logic 0	V_{OL}	14 (2.)		7, 9			8	1, 16
Threshold Voltage	Logic 1	V_{OHA}	14 (2.)		7, 9	12		8	1, 16
Threshold Voltage	Logic 0	V_{OLA}	14 (2.)		7, 9		12	8	1, 16
Switching Times	(50Ω Load)			**+1.11V**	**+0.31V**	**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	Clock Input	t_{13+14+}	14	12		13	14	8	1, 16
		t_{13+14-}	14			13	14	8	1, 16
		t_{13+4+}	4	7		13	4	8	1, 16
		t_{13+4-}	4	7		13	4	8	1, 16
	$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	t_{10-4-}	4 (3.)	7	13	10	4	8	1, 16
		t_{10+4+}	4	7	13	10	4	8	1, 16
Setup Time	Data Inputs	t_{12+13+}	14		7, 9	12, 13	14	8	1, 16
		t_{12-13+}	14		7, 9	12, 13	14	8	1, 16
	Select Inputs	t_{9+13+}	14			9, 13	14	8	1, 16
		t_{7+13+}	14			7, 13	14	8	1, 16
	$\overline{\text{Carry In}}$ Inputs	t_{10-13+}	14	7	9	10, 13	14	8	1, 16
		t_{13+10+}	14	7	9	10, 13	14	8	1, 16
Hold Time	Data Inputs	t_{13+12+}	14		7, 9	12, 13	14	8	1, 16
		t_{13+12-}	14		7, 9	12, 13	14	8	1, 16
	Select Inputs	t_{13+9+}	14			9, 13	14	8	1, 16
		t_{13+7+}	14			7, 13	14	8	1, 16
	$\overline{\text{Carry In}}$ Inputs	t_{13+10-}	14	7	9	10, 13	14	8	1, 16
		t_{10+13+}	14	7	9	10, 13	14	8	1, 16
Counting Frequency		$f_{countup}$	14	7		13	14	8	1, 16
		$f_{countdown}$	14	9		13	14	8	1, 16
Rise Time	(20 to 80%)	t_{4+}	4	7		13	4	8	1, 16
		t_{14+}	14	7		13	14	8	1, 16
Fall Time	(20 to 80%)	t_{4-}	4	7		13	4	8	1, 16
		t_{14-}	14	7		13	14	8	1, 16

1. Individually test each input; apply V_{ILmin} to pin under test.
2. Measure output after clock pulse  appears at clock input (Pin 13).

3. Before test set all Q outputs to a logic high.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



(a) is the minimum time to wait after the counter has been enabled to clock it.

(b) is the minimum time before the counter has been disabled that it may be clocked.

(c) is the minimum time before the counter is enabled that a clock pulse may be applied with no effect on the state of the counter.

(d) is the minimum time to wait after the counter is disabled that a clock pulse may be applied with no effect in the state of the counter.

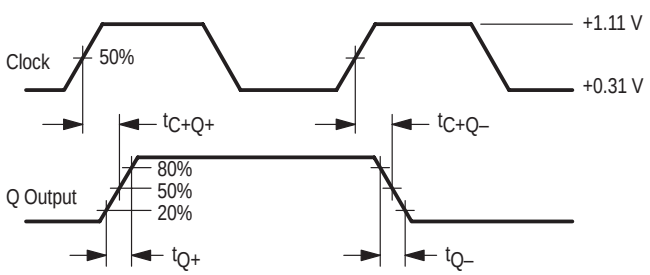
(b) and (c) may be negative numbers.

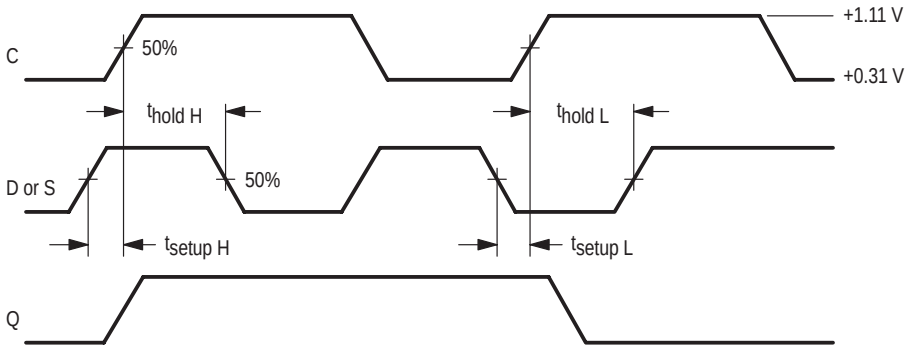
NOTE:

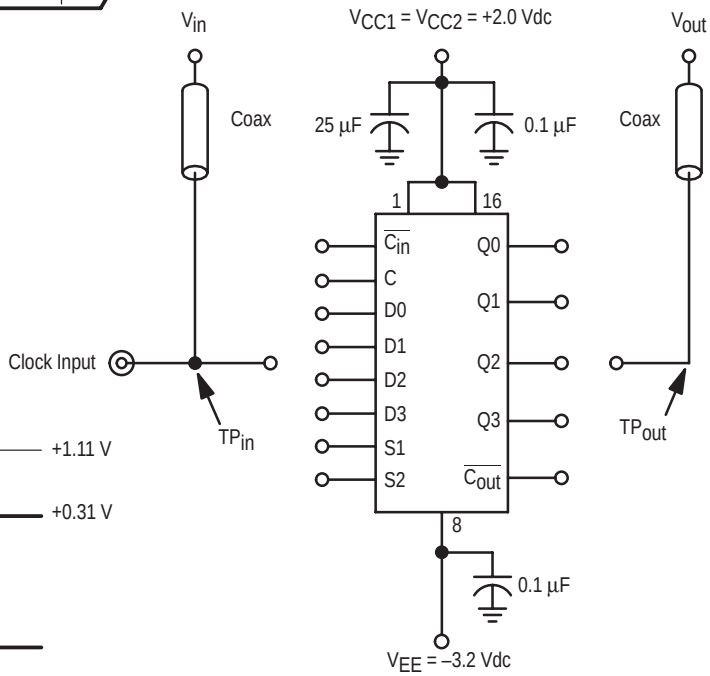
t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S.

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.

Input Pulse
t+ = t– = 2.0 ±0.2 ns
(20 to 80%)







50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs are connected to a 50-ohm resistor to ground.

MC10138

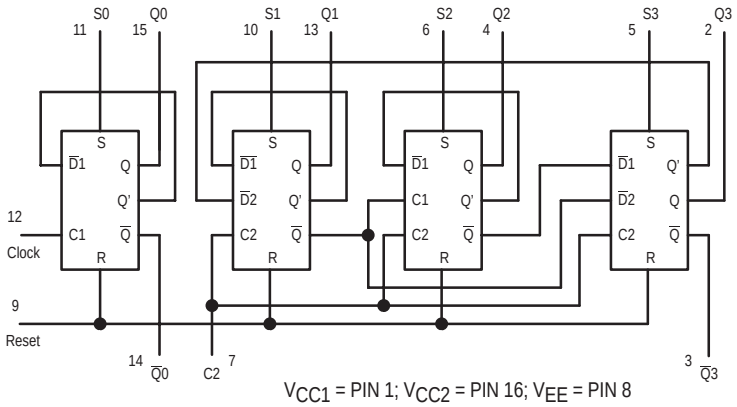
Bi-Quinary Counter

The MC10138 is a four bit counter capable of divide by two, five, or ten functions. It is composed of four set–reset master–slave flip–flops. Clock inputs trigger on the positive going edge of the clock pulse.

Set or reset input override the clock, allowing asynchronous “set” or “clear.” Individual set and common reset inputs are provided, as well as complementary outputs for the first and fourth bits.

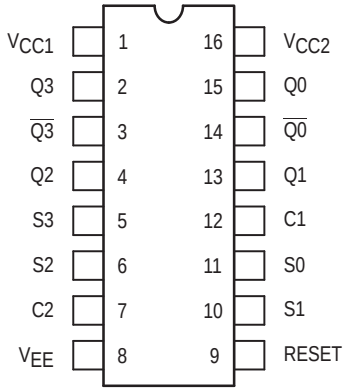
- P_D = 370 mW typ/pkg (No Load)
- f_{tog} = 150 MHz typ
- t_r, t_f = 2.5 ns typ (20%–80%)

LOGIC DIAGRAM



V_{CC1} = PIN 1; V_{CC2} = PIN 16; V_{EE} = PIN 8

DIP PIN ASSIGNMENT

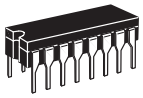


Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

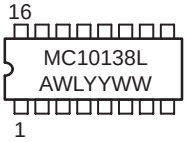
ON Semiconductor

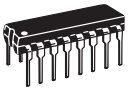
http://onsemi.com

MARKING DIAGRAMS

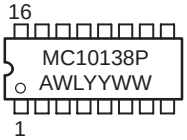


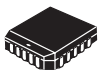
CDIP–16
L SUFFIX
CASE 620



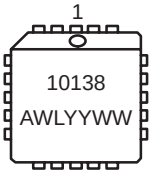


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10138L	CDIP–16	25 Units / Rail
MC10138P	PDIP–16	25 Units / Rail
MC10138FN	PLCC–20	46 Units / Rail

COUNTER TRUTH TABLES

BI–QUINARY
(Clock connected to C2
and $\overline{Q3}$ connected to C1)

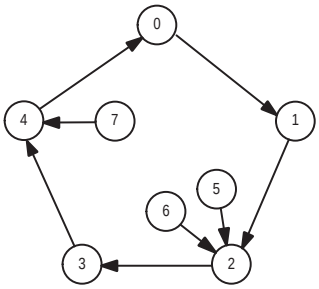
COUNT	Q1	Q2	Q3	Q0
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	L	L	L	H
6	H	L	L	H
7	L	H	L	H
8	H	H	L	H
9	L	L	H	H

BCD
(Clock connected to C1
and $\overline{Q0}$ connected to C2)

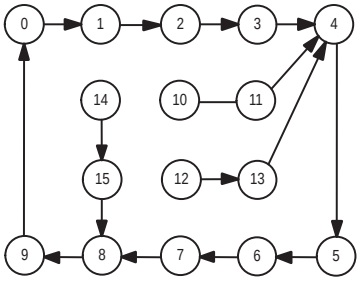
COUNT	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

COUNTER STATE DIAGRAM — POSITIVE LOGIC

CLOCK CONNECTED TO C2



$\overline{Q0}$ CONNECTED TO C2



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		97		70	88		97	mAdc
Input Current	I_{inH}	12 5,6,10,11 7 9		350 390 460 650			220 245 290 410		220 245 290	µAdc
	I_{inL}	All	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	3,14 (3.) 2,4,13,15 (2.)	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	3,14 (2.) 2,4,13,15 (3.)	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2,4,13,15 (2.) 3,14 (3.) 13,15 (2.)	–1.080 –1.080 –1.080		–0.980 –0.980 –0.980			–0.910 –0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2,4,13,15 (3.) 3,14 (2.) 13,15 (3.)		–1.655 –1.655 –1.655			–1.630 –1.630 –1.630		–1.595 –1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay Clock Delays	t_{12+15+} t_{12+14+} t_{7+13+} t_{7+4+} t_{7+2+} t_{7+3+}	15 14 13 4 2 3	1.4 1.4 1.4 1.4 1.4 1.4	5.0 5.0 5.2 5.2 5.2 5.2	1.5 1.5 1.5 1.5 1.5 1.5	3.5 3.5 3.5 3.5 3.5 3.5	4.8 4.8 5.0 5.0 5.0 5.0	1.5 1.5 1.5 1.5 1.5 1.5	5.3 5.3 5.5 5.5 5.5 5.5	
	$t_{12+15–}$ $t_{12+14–}$ $t_{7+13–}$ $t_{7+4–}$ $t_{7+2–}$ $t_{7+3–}$	15 14 13 4 2 3	1.4 1.4 1.4 1.4 1.4 1.4	5.0 5.0 5.2 5.2 5.2 5.2	1.5 1.5 1.5 1.5 1.5 1.5	3.5 3.5 3.5 3.5 3.5 3.5	4.8 4.8 5.0 5.0 5.0 5.0	1.5 1.5 1.5 1.5 1.5 1.5	5.3 5.3 5.5 5.5 5.5 5.5	
Set Delay	t_{11+15+} $t_{11+14–}$	15 14	1.4 1.4	5.2 5.2	1.5 1.5		5.0 5.0	1.5 1.5	5.5 5.5	
Reset Delay	t_{9+14+} $t_{9+15–}$	14 15	1.4 1.4	5.2 5.2	1.5 1.5		5.0 5.0	1.5 1.5	5.5 5.5	
Rise Time (20 to 80%)	t_{14+} t_{15+}	14 15	1.1 1.1	4.7 4.7	1.1 1.1	2.5 2.5	4.5 4.5	1.1 1.1	5.0 5.0	
Fall Time (20 to 80%)	$t_{14–}$ $t_{15–}$	14 15	1.1 1.1	4.7 4.7	1.1 1.1	2.5 2.5	4.5 4.5	1.1 1.1	5.0 5.0	
Counting Frequency	f_{count}	2 15	125 125		125 125	150 150		125 125		MHz

1. Individually test each input; apply V_{ILmin} to pin under test.
2. Set all four flip–flops by applying pulse 

to pins 5, 6, 10, and 11 prior to applying test voltage indicated.
3. Reset all four flip–flops by applying pulse 

to pin 9 prior to applying test voltage indicated.

ELECTRICAL CHARACTERISTICS (continued)

NOTE: Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.			TEST VOLTAGE VALUES (Volts)					
	@ Test Temperature		V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
	–30°C		–0.890	–1.890	–1.205	–1.500	–5.2	
	+25°C		–0.810	–1.850	–1.105	–1.475	–5.2	
	+85°C		–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8	9				8	1, 16
Input Current	I_{inH}	12	12				8	1, 16
		5,6,10,11	5,6,10,11				8	1, 16
		7	7				8	1, 16
		9	9				8	1, 16
	I_{inL}	All		Note 1.			8	1, 16
Output Voltage Logic 1	V_{OH}	3,14 (3.)	9				8	1, 16
		2,4,13,15 (2.)	5,6,10,11				8	1, 16
Output Voltage Logic 0	V_{OL}	3,14 (2.)	5,6,10,11				8	1, 16
		2,4,13,15 (3.)	9				8	1, 16
Threshold Voltage Logic 1	V_{OHA}	2,4,13,15 (2.)			5,6,10,11		8	1, 16
		3,14 (3.)			9		8	1, 16
		13,15 (2.)			7,12		8	1, 16
Threshold Voltage Logic 0	V_{OLA}	2,4,13,15 (3.)				5,6,10,11	8	1, 16
		3,14 (2.)				9	8	1, 16
		13,15 (3.)				7,12	8	1, 16
Switching Times (50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay Clock Delays	t_{12+15+}	15			12	15	8	1, 16
	t_{12+14+}	14			12	14	8	1, 16
	t_{7+13+}	13			7	13	8	1, 16
	t_{7+4+}	4			7	4	8	1, 16
	t_{7+2+}	2			7	2	8	1, 16
	t_{7+3+}	3			7	3	8	1, 16
	t_{12+15-}	15			12	15	8	1, 16
	t_{12+14-}	14			12	14	8	1, 16
	t_{7+13-}	13			7	13	8	1, 16
	t_{7+4-}	4			7	4	8	1, 16
	t_{7+2-}	2			7	2	8	1, 16
	t_{7+3-}	3			7	3	8	1, 16
Set Delay	t_{11+15+}	15			11	15	8	1, 16
	t_{11+14-}	14			11	14	8	1, 16
Reset Delay	t_{9+14+}	14			9	14	8	1, 16
	t_{9+15-}	15			9	15	8	1, 16
Rise Time (20 to 80%)	t_{14+}	14			11	14	8	1, 16
	t_{15+}	15			11	15	8	1, 16
Fall Time (20 to 80%)	t_{14-}	14			9	14	8	1, 16
	t_{15-}	15			9	15	8	1, 16
Counting Frequency	f_{count}	2			7	2	8	1, 16
		15			12	15	8	1, 16

1. Individually test each input; apply V_{ILmin} to pin under test.
2. Set all four flip–flops by applying pulse 

to pins 5, 6, 10, and 11 prior to applying test voltage indicated.
3. Reset all four flip–flops by applying pulse 

to pin 9 prior to applying test voltage indicated.

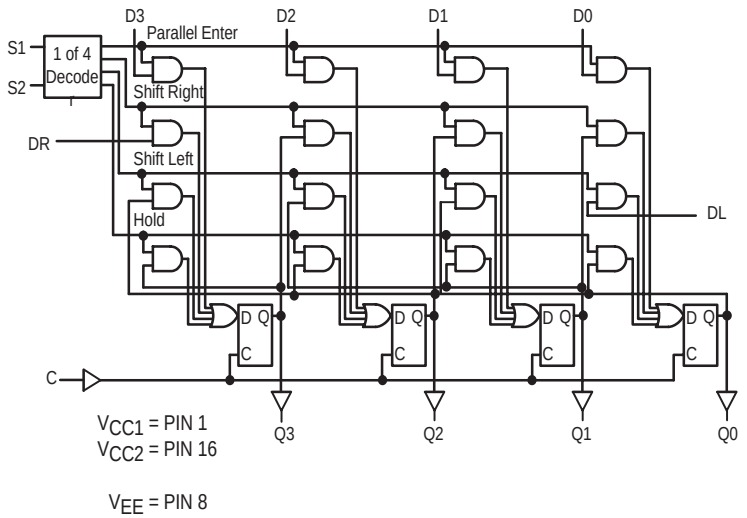
MC10141

Four Bit Universal Shift Register

The MC10141 is a four–bit universal shift register which performs shift left, or shift right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control the four possible operations of the register without external gating of the clock. The flip–flops shift information on the positive edge of the clock. The four operations are stop shift, shift left, shift right, and parallel entry of data. The other six inputs are all data type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR).

- P_D = 425 mW typ/pkg (No Load)
- f_{Shift} = 200 MHz typ
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



TRUTH TABLE

SELECT			OUTPUTS			
S1	S2	OPERATING MODE	$Q0_{n+1}$	$Q1_{n+1}$	$Q2_{n+1}$	$Q3_{n+1}$
L	L	Parallel Entry	D0	D1	D2	D3
L	H	Shift Right*	$Q1_n$	$Q2_n$	$Q3_n$	DR
H	L	Shift Left*	DL	$Q0_n$	$Q1_n$	$Q2_n$
H	H	Stop Shift	$Q0_n$	$Q1_n$	$Q2_n$	$Q3_n$

*Outputs as exist after pulse appears at “C” input with input conditions as shown. (Pulse = Positive transition of clock input).

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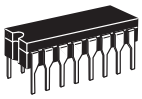
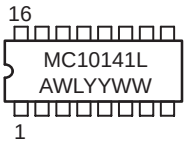
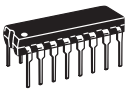
MARKING DIAGRAMS

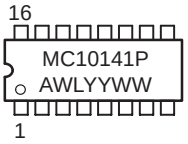


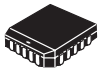
CDIP–16
L SUFFIX
CASE 620



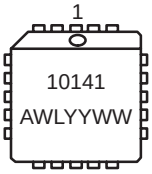


PDIP–16
P SUFFIX
CASE 648



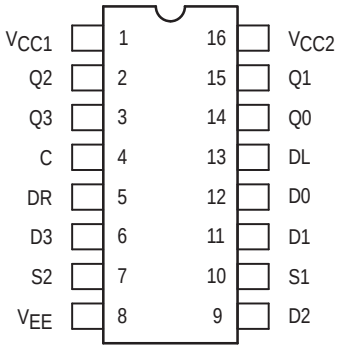


PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT

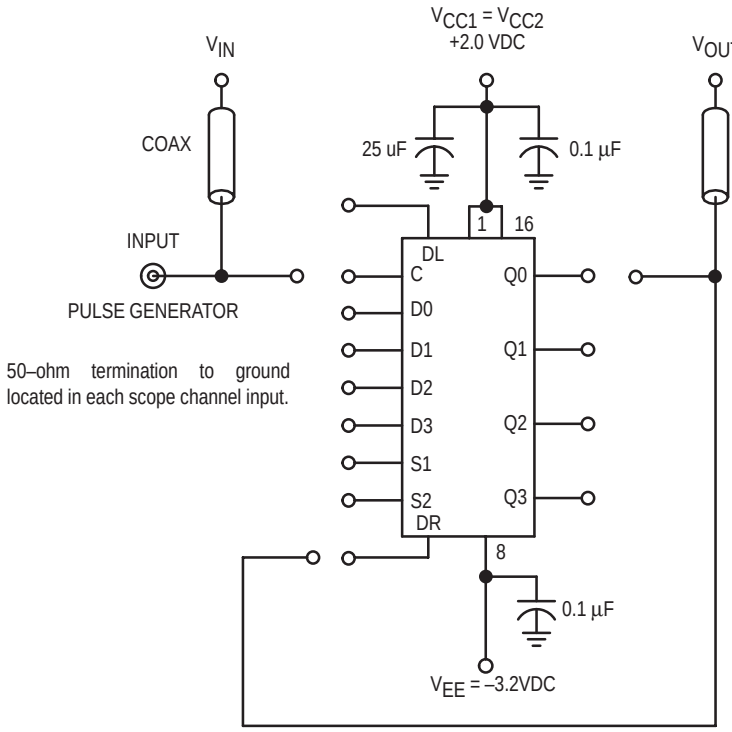


Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ORDERING INFORMATION

Device	Package	Shipping
MC10141L	CDIP–16	25 Units / Rail
MC10141P	PDIP–16	25 Units / Rail
MC10141FN	PLCC–20	46 Units / Rail

SHIFT FREQUENCY TEST CIRCUIT



50–ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50–ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

TEST PROCEDURES:

1. SET D1, D2, D3 = +0.31 VDC (LOGIC L)
   D0 = +1.11 VDC (LOGIC H)
2. APPY CLOCK PULSE V_{IH} / V_{IL} TO SET Q0 HIGH.
3. MAINTAIN CLOCK LOW.
   SET S1 = +0.31 VDC (LOGIC L)
   S2 = +1.11 VDC (LOGIC H)
4. TEST SHIFT FREQUENCY

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		112		82	102		112	mAdc
Input Current	I_{inH}	5 6 7 4		350 350 390 425			220 220 245 265		220 220 245 265	µAdc
	I_{inL}	12	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	3	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	Vdc
Output Voltage Logic 0	V_{OL}	3	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	Vdc
Threshold Voltage Logic 1	V_{OHA} (Note 1.)	3 3 3 3	–1.080 –1.080 –1.080 –1.080		–0.980 –0.980 –0.980 –0.980			–0.910 –0.910 –0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA} (Note 1.)	3 3 3 3		–1.655 –1.655 –1.655 –1.655			–1.630 –1.630 –1.630 –1.630		–1.595 –1.595 –1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{4+3+}	3	1.7	3.9	1.8	2.9	3.8	2.0	4.2	
Setup TIme (t_{setup})	t_{12+4+}	14	2.5		2.5			2.5		
	t_{10+4+}	14	5.5		5.0			5.5		
Hold Time (t_{hold})	t_{4+12+}	14	1.5		1.5			1.5		
Rise Time (20 to 80%)	t_{3+}	3	1.0	3.4	1.1	2.0	3.3	1.1	3.6	
Fall Time (20 to 80%)	$t_{3–}$	3	1.0	3.4	1.1	2.0	3.3	1.1	3.6	
Shift Frequency	f_{shift}		150		150	200		150		MHz

1. These tests to be performed in sequence as shown.

2. See shift frequency test circuit for test procedures.
3. Reset to zero before performing test.
4. Reset to one before performing test.

ELECTRICAL CHARACTERISTICS (continued)

			TEST VOLTAGE VALUES (Volts)								
@ Test Temperature			**V_{IHmax}**	**V_{ILmin}**	**V_{IHAmin}**	**V_{ILAmax}**	**V_{EE}**				
–30°C			–0.890	–1.890	–1.205	–1.500	–5.2				
+25°C			–0.810	–1.850	–1.105	–1.475	–5.2				
+85°C			–0.700	–1.825	–1.035	–1.440	–5.2				
Characteristic		**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**							
				V_{IHmax}	**V_{ILmin}**	**V_{IHAmin}**	**V_{ILAmax}**	**V_{EE}**	**P1**	**P2**	**P3**	**(V_{CC}) Gnd**
Power Supply Drain Current		I_E	8					8				1, 16
Input Current		I_{inH}	5	5				8				1, 16
			6	6				8				1, 16
			7	7				8				1, 16
			4	4				8				1, 16
		I_{inL}	12	4,5,6,7,9, 10,11,13	12			8				1, 16
Output Voltage	Logic 1	V_{OH}	3	6				8	4			1, 16
Output Voltage	Logic 0	V_{OL}	3					8	4			1, 16
Threshold Voltage	Logic 1	V_{OHA}	3			6		8	4			1, 16
		(Note 1.)	3	6	Note 3.		7	8	4			1, 16
			3	6	Note 3.			8		4		1, 16
			3					8			4	1, 16
Threshold Voltage	Logic 0	V_{OLA}	3				6	8	4			1, 16
		(Note 1.)	3		Note 4.		7	8	4			1, 16
			3		Note 4.			8		4		1, 16
			3	6				8			4	1, 16
Switching Times (50Ω Load)								**–3.2 V**				**+2.0 V**
Propagation Delay		t_{4+3+}	3					8				1, 16
Setup TIme (t_{setup})		t_{12+4+}	14					8				1, 16
		t_{10+4+}	14					8				1, 16
Hold Time (t_{hold})		t_{4+12+}	14					8				1, 16
Rise Time	(20 to 80%)	t_{3+}	3					8				1, 16
Fall Time	(20 to 80%)	$t_{3–}$	3					8				1, 16
Shift Frequency		f_{shift}		Note 2.				8				1, 16

1. These tests to be performed in sequence as shown.

2. See shift frequency test circuit for test procedures.
3. Reset to zero before performing test.
4. Reset to one before performing test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

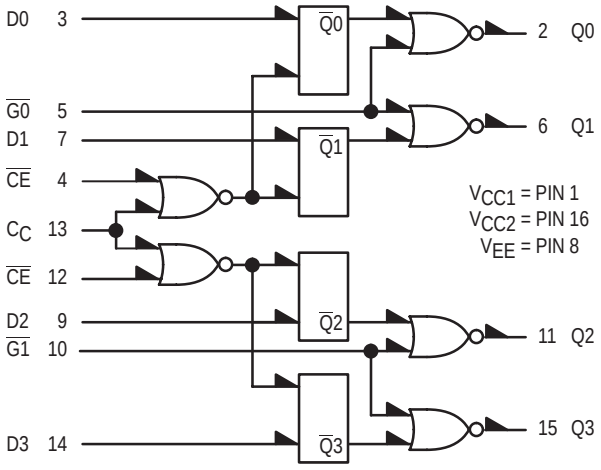
MC10153

Quad Latch

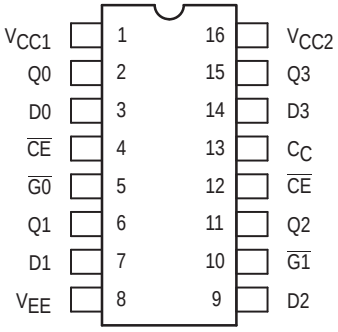
The MC10153 is a high speed, low power, MECL quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs. Open emitters allow a large number of outputs to be wire-ORed together. Latch outputs are gated, allowing direct wiring to a bus. When the clock is low, outputs will follow D inputs. Information is latched on positive going transition of the clock. The MC10153 provides the same logic function as the MC10133, except for inversion of the clock.

- P_D = 310 mW typ/pkg (No Load)
- t_{pd} = 4.0 ns typ
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	X	X	L
L	H	X	Q_n
L	L	L	L
L	L	H	H

$C = C_C + \overline{CE}$

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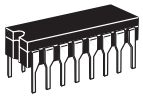
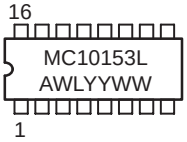
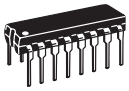
MARKING DIAGRAMS

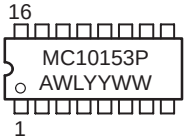


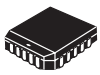
CDIP–16
L SUFFIX
CASE 620



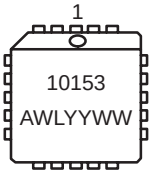


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

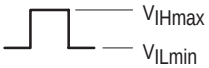
ORDERING INFORMATION

Device	Package	Shipping
MC10153L	CDIP–16	25 Units / Rail
MC10153P	PDIP–16	25 Units / Rail
MC10153FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		83			75		83	mAdc
Input Current	I_{inH}	3		390			245		245	µAdc
		4		390			245		245	
		5		560			350		350	
		13		460			290		290	
	I_{inL}	3	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	2	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	Vdc
		2	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	
Output Voltage Logic 0	V_{OL}	2	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	Vdc
		2	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	
		2	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	
Threshold Voltage Logic 1	V_{OHA}	2	–1.080		–0.980			–0.910		Vdc
		2	–1.080		–0.980			–0.910		
		2	–1.080		–0.980			–0.910		
		2†	–1.080		–0.980			–0.910		
		2‡	–1.080		–0.980			–0.910		
		2‡	–1.080		–0.980			–0.910		
		2	–1.080		–0.980			–0.910		
		2	–1.080		–0.980			–0.910		
Threshold Voltage Logic 0	V_{OLA}	2		–1.655			–1.630		–1.595	Vdc
		2		–1.655			–1.630		–1.595	
		2		–1.655			–1.630		–1.595	
		2†		–1.655			–1.630		–1.595	
		2‡		–1.655			–1.630		–1.595	
		2‡		–1.655			–1.630		–1.595	
Switching Times (50Ω Load)										ns
Propagation Delay	t_{3+2+}	2	1.0	5.6	1.0	4.0	5.4	1.1	5.9	
	$t_{4–2+}$	2	1.0	5.6	1.0	4.0	5.6	1.2	6.2	
	$t_{5–2+}$	2	1.0	3.2	1.0	2.0	3.1	1.0	3.4	
	t_{setup}	3	2.5		2.5	0.7		2.5		
	t_{hold}	3	1.5		1.5	0.7		1.5		
Rise Time (20 to 80%)	t_{2+}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8	
Fall Time (20 to 80%)	$t_{2–}$	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8	

† Output level to be measured after a clock pulse has been applied to the clock input (Pin 4)



‡ Data input at proper high/low level while clock pulse is high so that device latches ar proper high/low level for test. Levels are measured after device has latched.

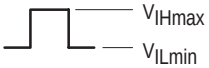
* Latch set to zero state before test.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8		13			8	1, 16
Input Current	I_{inH}	3	3				8	1, 16
		4	4				8	1, 16
		5	5				8	1, 16
		13	13				8	1, 16
	I_{inL}	3		3			8	1, 16
Output Voltage Logic 1	V_{OH}	2	3	4			8	1, 16
		2	3	13			8	1, 16
Output Voltage Logic 0	V_{OL}	2		3,13			8	1, 16
		2	3,5	13			8	1, 16
		2		3,4			8	1, 16
Threshold Voltage Logic 1	V_{OHA}	2	3	4		5	8	1, 16
		2		4	3		8	1, 16
		2	3	4			8	1, 16
		2†	3				8	1, 16
		2‡					8	1, 16
		2‡					8	1, 16
		2	3			4	8	1, 16
		2	3			13	8	1, 16
Threshold Voltage Logic 0	V_{OLA}	2	3	4	5		8	1, 16
		2		4		3	8	1, 16
		2		4			8	1, 16
		2†					8	1, 16
		2‡	3				8	1, 16
		2‡	3			13	8	1, 16
Switching Times (50Ω Load)			**+1.11 V**		**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	t_{3+2+}	2			3	2	8	1, 16
	t_{4-2+}	2	3*		4	2	8	1, 16
	t_{5-2+}	2			5	2	8	1, 16
	t_{setup}	3			3	2	8	1, 16
	t_{hold}	3			3	2	8	1, 16
Rise Time (20 to 80%)	t_{2+}	2			3	2	8	1, 16
Fall Time (20 to 80%)	t_{2-}	2			3	2	8	1, 16

† Output level to be measured after a clock pulse has been applied to the clock input (Pin 4)



‡ Data input at proper high/low level while clock pulse is high so that device latches ar proper high/low level for test. Levels are measured after device has latched.

* Latch set to zero state before test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10154

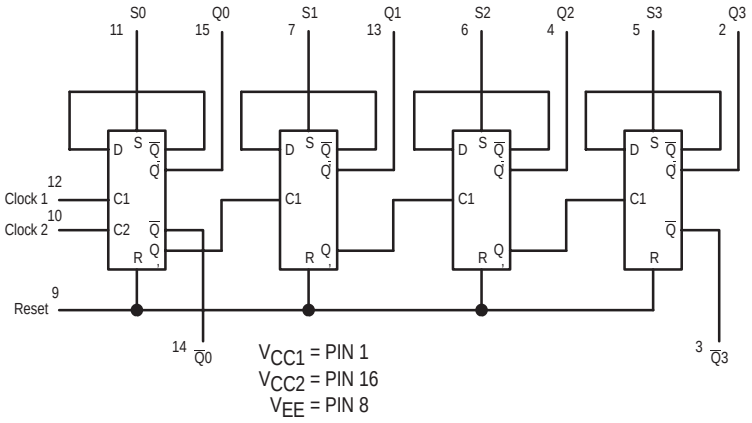
Binary Counter

The MC10154 is a four–bit counter capable of divide–by–two, divide–by– four, divide–by–eight or a divide–by–sixteen function.

Clock inputs trigger on the positive going edge of the clock pulse. Set and Reset inputs override the clock, allowing asynchronous “set” or “clear.” Individual Set and common Reset inputs are provided, as well as complemen– tary outputs for the first and fourth bits. True outputs are available at all bits.

- P_D=370 mW typ/pkg (No Load)
- f_{toggle}= 150 MHz (typ)
- t_{pd}=3.5 ns typ (C to Q_0)
- t_{pd}=11 ns typ (C to Q_3)

LOGIC DIAGRAM



TRUTH TABLE

INPUTS							OUTPUTS			
R	S0	S1	S2	S3	C1	C2	Q0	Q1	Q2	Q3
H	L	L	L	L	X	X	L	L	L	L
L	H	H	H	H	X	X	H	H	H	H
L	L	L	L	L	H	X	No Count			
L	L	L	L	L	X	H	No Count			
L	L	L	L	L	*	*	H	H	H	H
L	L	L	L	L	*	*	L	H	H	H
L	L	L	L	L	*	*	H	L	H	H
L	L	L	L	L	*	*	L	L	H	H
L	L	L	L	L	*	*	H	H	L	H
L	L	L	L	L	*	*	L	H	L	H
L	L	L	L	L	*	*	H	L	L	H
L	L	L	L	L	*	*	L	L	L	H
L	L	L	L	L	*	*	H	H	H	L
L	L	L	L	L	*	*	L	H	H	L
L	L	L	L	L	*	*	H	L	H	L
L	L	L	L	L	*	*	L	L	H	L
L	L	L	L	L	*	*	H	H	L	L
L	L	L	L	L	*	*	L	H	L	L
L	L	L	L	L	*	*	H	L	L	L
L	L	L	L	L	*	*	L	L	L	L

* Clock transitions from V_{IL} to V_{IH} may be applied to C1 or C2 or both for same effect.

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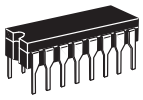
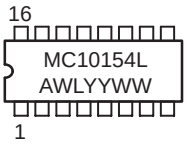
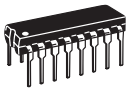
MARKING DIAGRAMS

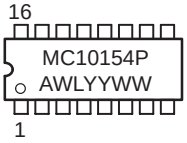


CDIP–16
L SUFFIX
CASE 620

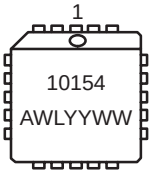




PDIP–16
P SUFFIX
CASE 648

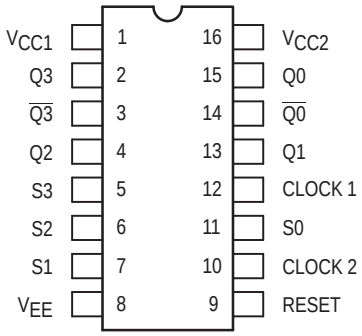


PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ORDERING INFORMATION

Device	Package	Shipping
MC10154L	CDIP–16	25 Units / Rail
MC10154P	PDIP–16	25 Units / Rail
MC10154FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		97			88		97	mAdc
Input Current	I_{inH}	12 11 9		390 350 650			245 220 410		245 220 410	μAdc
	I_{inL}	*	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	14 15	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	14 15	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	3 14 15	–1.080 –1.080 –1.080		–0.980 –0.980 –0.980			–0.910 –0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	3 14 15		–1.655 –1.655 –1.655			–1.630 –1.630 –1.630		–1.595 –1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Clock Input Propagation Delay	t_{12+15+} t_{12-13-} t_{12+4-} t_{12-3+}	15 13 4 3	1.4 1.9 2.9 3.9	5.0 9.4 12.3 14.9	1.5 2.0 3.0 4.0	3.5 6.0 8.5 11.0	4.8 9.2 12.0 14.5	1.5 2.0 3.0 4.0	5.3 9.8 12.8 15.5	
Rise Time (20 to 80%)	t_{15+}	15	1.1	4.7	1.1	2.5	4.5	1.1	5.0	
Fall Time (20 to 80%)	t_{15-}	15	1.1	4.7	1.1	2.5	4.5	1.1	5.0	
Set Input Reset Input	t_{11-15+} t_{9-15+}	15 15	1.4 1.4	5.2 5.2	1.5 1.5		5.0 5.0	1.5 1.5	5.5 5.5	
Counting Frequency	f_{count}	15	125		125	150		125		MHz

* Individually test each input applying V_{IL} to input under test.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts)				
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8	9				8	1, 16
Input Current	I_{inH}	12	12				8	1, 16
		11	11				8	1, 16
		9	9				8	1, 16
	I_{inL}	*		*			8	1, 16
Output Voltage Logic 1	V_{OH}	14	9				8	1, 16
		15	11				8	1, 16
Output Voltage Logic 0	V_{OL}	14	11				8	1, 16
		15	9				8	1, 16
Threshold Voltage Logic 1	V_{OHA}	3			5		8	1, 16
		14			11		8	1, 16
		15			9		8	1, 16
Threshold Voltage Logic 0	V_{OLA}	3				5	8	1, 16
		14				11	8	1, 16
		15				9	8	1, 16
Switching Times (50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0V**
Clock Input Propagation Delay	t_{12+15+}	15			12	15	8	1, 16
	$t_{12–13–}$	13			12	13	8	1, 16
	$t_{12+4–}$	4			12	4	8	1, 16
	$t_{12–3+}$	3			12	3	8	1, 16
Rise Time (20 to 80%)	t_{15+}	15			12	15	8	1, 16
Fall Time (20 to 80%)	$t_{15–}$	15			12	15	8	1, 16
Set Input	$t_{11–15+}$	15			11	15	8	1, 16
Reset Input	$t_{9–15+}$	15			9	15	8	1, 16
Counting Frequency	f_{count}	15			12	15	8	1, 16

* Individually test each input applying V_{IL} to input under test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

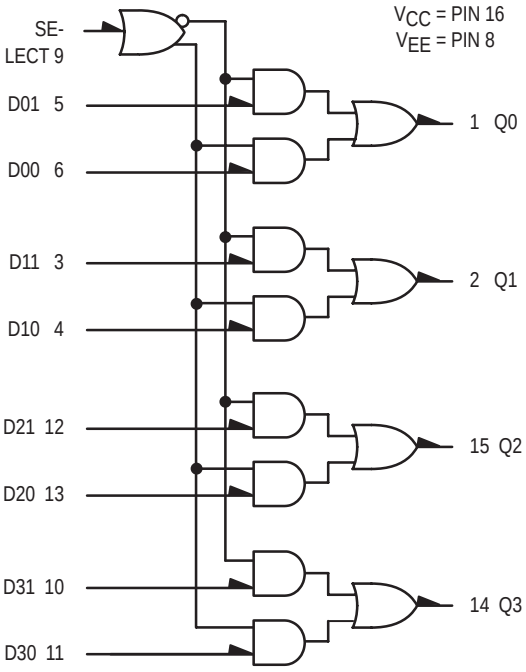
MC10158

Quad 2-Input Multiplexer
(Non–Inverting)

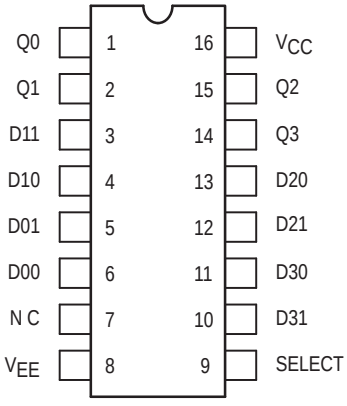
The MC10158 is a quad two channel multiplexer. A common select input determines which data inputs are enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, and D31.

- P_D=197 mW typ/pkg (No Load)
- t_{pd}=2.5 ns typ (Data to Q)
- 3.2 ns typ (Select to Q)
- t_r, t_f=2.5 ns typ (20%–80%)

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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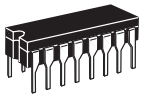
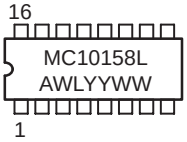
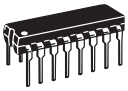
MARKING DIAGRAMS

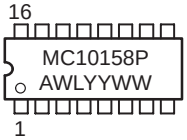


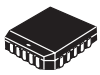
CDIP–16
L SUFFIX
CASE 620



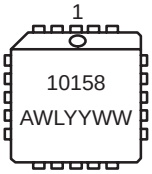


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

TRUTH TABLE

Select	D0	D1	Q
L	X	L	L
L	X	H	H
H	L	X	L
H	H	X	H

ORDERING INFORMATION

Device	Package	Shipping
MC10158L	CDIP–16	25 Units / Rail
MC10158P	PDIP–16	25 Units / Rail
MC10158FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		53		38	48		53	mAdc
Input Current	I_{inH}	9 5		360 400			225 250		225 250	µAdc
	I_{inL}	5	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	1	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	Vdc
Output Voltage Logic 0	V_{OL}	1	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	1	–1.080		–0.980			–0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	1		–1.655			–1.630		–1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay Data Input	t_{5-1-}	1	1.3	3.1	1.2	2.5	3.0	1.3	3.2	
Propagation Delay Select Input	t_{9+1+}	1	2.5	4.8	2.4	3.2	4.5	2.5	4.8	
Rise Time (20 to 80%)	t_{1+}	1	1.6	3.4	1.5	2.5	3.3	1.6	3.4	
Fall Time (20 to 80%)	t_{1-}	1	1.6	3.4	1.5	2.5	3.3	1.6	3.4	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts)					
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8					8	16
Input Current	I_{inH}	9 5	9 5				8 8	16 16
	I_{inL}	5		5			8	16
Output Voltage Logic 1	V_{OH}	1	5				8	16
Output Voltage Logic 0	V_{OL}	1					8	16
Threshold Voltage Logic 1	V_{OHA}	1			5		8	16
Threshold Voltage Logic 0	V_{OLA}	1				5	8	16
Switching Times (50Ω Load)			**+1.11V**	**+0.31V**	**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay Data Input	t_{5-1-}	1			5	1	8	16
Propagation Delay Select Input	t_{9+1+}	1	6		9	1	8	16
Rise Time (20 to 80%)	t_{1+}	1			5	1	8	16
Fall Time (20 to 80%)	t_{1-}	1			5	1	8	16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

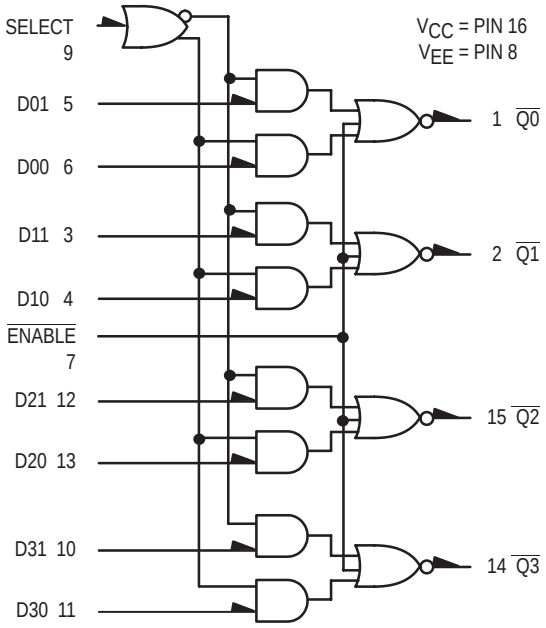
MC10159

Quad 2-Input Multiplexer
(Inverting)

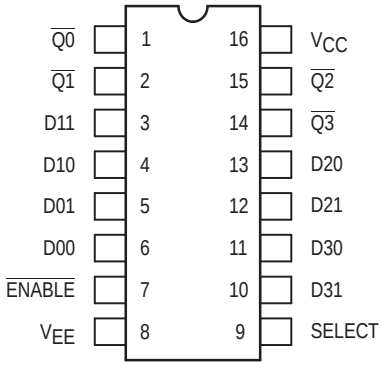
The MC10159 is a quad two channel multiplexer with enable. It incorporates common enable and common data select inputs. The select input determines which data inputs are enabled. A high (H) level enables data inputs D00, D10, D20, and D30. A low (L) level enables data inputs D01, D11, D21, and D31. Any change on the data inputs will be reflected at the outputs while the enable is low. Input levels are inverted at the output.

- P_D=218 mW typ/pkg (No Load)
- t_{pd}=2.5 ns typ (Data to Q)
- 3.2 ns typ (Select to Q)
- t_r, t_f=2.5 ns typ (20%–80%)

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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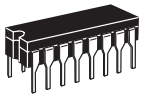
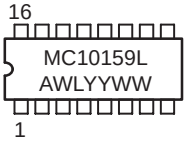
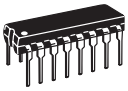
MARKING DIAGRAMS

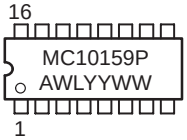


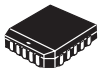
CDIP–16
L SUFFIX
CASE 620



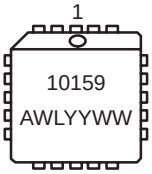


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

TRUTH TABLE

Enable	Select	D0	D1	$\overline{Q}$
L	L	X	L	H
L	L	X	H	L
L	H	L	X	H
L	H	H	X	L
H	X	X	X	L

ORDERING INFORMATION

Device	Package	Shipping
MC10159L	CDIP–16	25 Units / Rail
MC10159P	PDIP–16	25 Units / Rail
MC10159FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Pin Under Test	Test Limits							Unit
				–30°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current		I_E	8		58		42	53		58	mAdc
Input Current		I_{inH}	9 5		360 400			225 250		225 250	μAdc
		I_{inL}	5	0.5		0.5			0.3		μAdc
Output Voltage	Logic 1	V_{OH}	1	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	Vdc
Output Voltage	Logic 0	V_{OL}	1	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	Vdc
Threshold Voltage	Logic 1	V_{OHA}	1	–1.080		–0.980			–0.910		Vdc
Threshold Voltage	Logic 0	V_{OLA}	1		–1.655			–1.630		–1.595	Vdc
Switching Times (50Ω Load)											ns
Propagation Delay	Data Input	t_{5+1-}	1	1.1	3.8	1.2	2.5	3.3	1.1	3.8	
	Select Input	t_{9+1-}	1	1.5	5.3	1.5	3.2	5.0	1.5	5.3	
	Enable Input	t_{7+1-}	1	1.4	5.3	1.5	2.5	5.0	1.4	5.3	
Rise Time	(20 to 80%)	t_{1+}	1	1.0	3.7	1.1	2.5	3.5	1.0	3.7	
Fall Time	(20 to 80%)	t_{1-}	1	1.0	3.7	1.1	2.5	3.5	1.0	3.7	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts)					
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	16
Input Current		I_{inH}	9 5	9 5				8 8	16 16
		I_{inL}	5		5			8	16
Output Voltage	Logic 1	V_{OH}	1					8	16
Output Voltage	Logic 0	V_{OL}	1	5				8	16
Threshold Voltage	Logic 1	V_{OHA}	1	9			6	8	16
Threshold Voltage	Logic 0	V_{OLA}	1	9		6		8	16
Switching Times	(50Ω Load)			**+1.11V**	**+0.31V**	**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	Data Input	t_{5+1-}	1			5	1	8	16
	Select Input	t_{9+1-}	1	6		9	1	8	16
	Enable Input	t_{7+1-}	1	3, 12		7	1		
Rise Time	(20 to 80%)	t_{1+}	1	9		5	1	8	16
Fall Time	(20 to 80%)	t_{1-}	1	9		5	1	8	16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

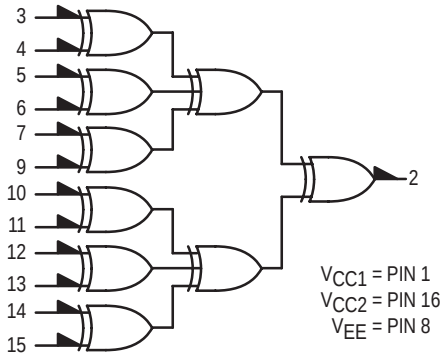
MC10160

12-Bit Parity Generator-Checker

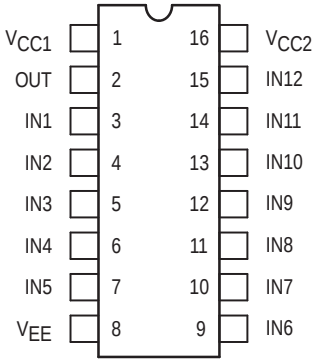
The MC10160 consists of nine Exclusive-OR gates in a single package, internally connected to provide odd parity checking or generation. Output goes high when an odd number of inputs are high. Unconnected inputs are pulled to low logic levels allowing parity detection and generation for less than 12 bits.

- P_D = 320 mW typ/pkg (No Load)
- t_{pd} = 5.0 ns typ
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

INPUT	OUTPUT
Sum of High Level Inputs	Pin 2
Even	Low
Odd	High

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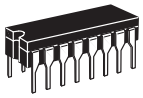
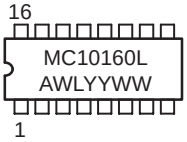
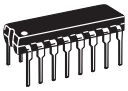
MARKING DIAGRAMS

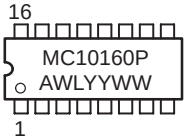


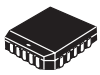
CDIP–16
L SUFFIX
CASE 620



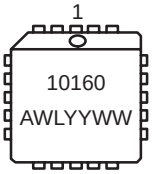


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10160L	CDIP–16	25 Units / Rail
MC10160P	PDIP–16	25 Units / Rail
MC10160FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		86		62	78		86	mAdc
Input Current	I_{inH} (Note 1.)	3 4		425 350			265 220		265 220	μAdc
	I_{inL}	3	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	2	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	Vdc
Output Voltage Logic 0	V_{OL}	2	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2	–1.080		–0.980			–0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2		–1.655			–1.630		–1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{3+2+}	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
	$t_{3+2–}$	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
	$t_{3–2–}$	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
	$t_{3–2+}$	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
	t_{4+2+}	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
	$t_{4+2–}$	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
	$t_{4–2–}$	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
	$t_{4–2+}$	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
Rise Time (20 to 80%)	t_{2+}	2	1.1	3.5	1.1	2.0	3.3	1.0	3.5	
Fall Time (20 to 80%)	$t_{2–}$	2	1.1	3.5	1.1	2.0	3.3	1.0	3.5	

1. Pins 3, 6, 7, 11, 12, 15 are similar. Pins 4, 5, 9, 10, 13, 14 are similar.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C			–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C			–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C			–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic	**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					**(V_{CC}) Gnd**
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8	4,5,9, 10,13,14				8	1,16
Input Current	I_{inH}	3	3				8	1,16
	(Note 1.)	4	4				8	1,16
	I_{inL}	3		3			8	1,16
Output Voltage Logic 1	V_{OH}	2	3	4,5,6,7,9,10, 11,12,13,14,15			8	1,16
Output Voltage Logic 0	V_{OL}	2		3,4,5,6,7,9,10, 11,12,13,14,15			8	1,16
Threshold Voltage Logic 1	V_{OHA}	2		4,5,6,7,9,10, 11,12,13,14,15	3		8	1,16
Threshold Voltage Logic 0	V_{OLA}	2		3,5,6,7,9,10, 11,12,13,14,15		4	8	1,16
Switching Times (50Ω Load)			**+1.11V**		**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	t_{3+2+}	2			3	2	8	1,16
	t_{3+2-}	2	4		3	2	8	1,16
	t_{3-2-}	2			3	2	8	1,16
	t_{3-2+}	2	4		3	2	8	1,16
	t_{4+2+}	2			4	2	8	1,16
	t_{4+2-}	2	3		4	2	8	1,16
	t_{4-2-}	2			4	2	8	1,16
	t_{4-2+}	2	3		4	2	8	1,16
Rise Time (20 to 80%)	t_{2+}	2			3	2	8	1,16
Fall Time (20 to 80%)	t_{2-}	2			3	2	8	1,16

1. Pins 3, 6, 7, 11, 12, 15 are similar. Pins 4, 5, 9, 10, 13, 14 are similar.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10161

Binary to 1-8 Decoder (Low)

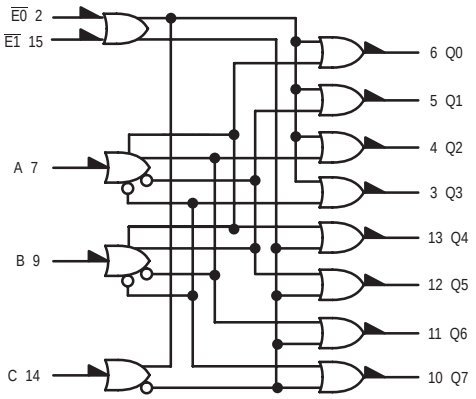
The MC10161 is designed to decode a three bit input word to a one of eight line output. The selected output will be low while all other outputs will be high. The enable inputs, when either or both are high, force all outputs high.

The MC10161 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders. This design provides the identical 4 ns delay from any address or enable input to any output.

A complete mux/demux operation on 16 bits for data distribution is illustrated in Figure 1. This system, using the MC10136 control counters, has the capability of incrementing, decrementing or holding data channels. When both S0 and S1 are low, the index counters reset, thus initializing both the mux and demux units. The four binary outputs of the counter are buffered by the MC10161s to send twisted–pair select data to the multiplexer/demultiplexer to units.

- P_D = 315 mW typ/pkg (No Load)
- t_{pd} = 4.0 ns typ
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
$\overline{E1}$	$\overline{E0}$	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	H	H	H	H	H	H	H	H

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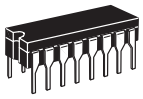
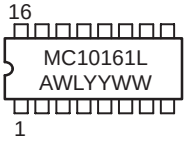
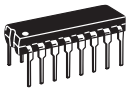
MARKING DIAGRAMS

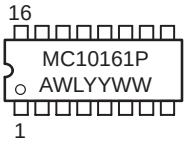


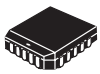
CDIP–16
L SUFFIX
CASE 620



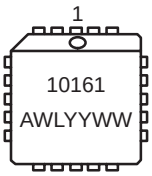


PDIP–16
P SUFFIX
CASE 648



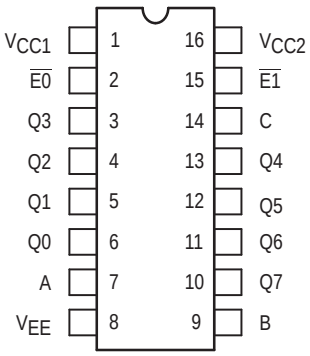


PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ORDERING INFORMATION

Device	Package	Shipping
MC10161L	CDIP–16	25 Units / Rail
MC10161P	PDIP–16	25 Units / Rail
MC10161FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		84		61	76		84	mAdc
Input Current	I_{inH}	14		350			220		220	μAdc
	I_{inL}	14	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	13 13	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	13	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	13 13	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	13		–1.655			–1.630		–1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{14+13-} t_{14-13+}	13 13	1.5 1.5	6.2 6.2	1.5 1.5	4.0 4.0	6.0 6.0	1.5 1.5	6.4 6.4	
Rise Time (20 to 80%)	t_{13+}	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5	
Fall Time (20 to 80%)	t_{13-}	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5	

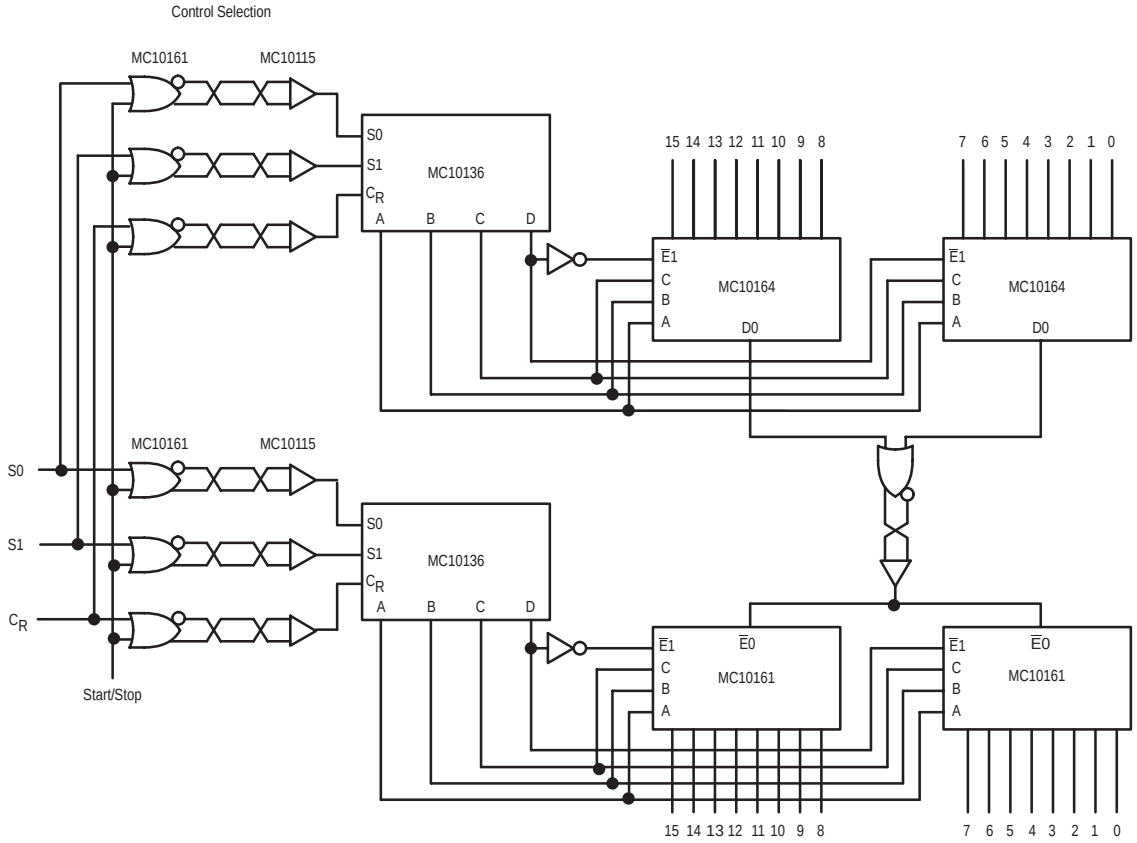
ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts)					
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8	2,7,9,14,15				8	1,16
Input Current	I_{inH}	14	14				8	1,16
	I_{inL}	14		14			8	1,16
Output Voltage Logic 1	V_{OH}	13 13	2 15				8 8	1,16 1,16
Output Voltage Logic 0	V_{OL}	13	14				8	1,16
Threshold Voltage Logic 1	V_{OHA}	13 13			2 15		8 8	1,16 1,16
Threshold Voltage Logic 0	V_{OLA}	13			14		8	1,16
Switching Times (50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	t_{14+13-} t_{14-13+}	13 13			14 14	13 13	8 8	1,16 1,16
Rise Time (20 to 80%)	t_{13+}	13			14	13	8	1,16
Fall Time (20 to 80%)	t_{13-}	13			14	13	8	1,16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

FIGURE 1 — HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER



MC10162

Binary to 1-8 Decoder (High)

The MC10162 is designed to convert three lines of input data to a one–of–eight output. The selected output will be high while all other outputs are low. The enable inputs, when either or both are high, force all outputs low.

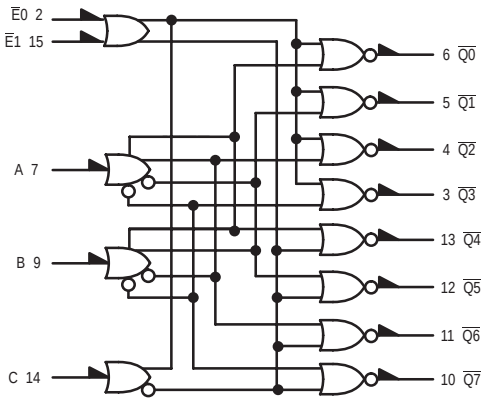
The MC10162 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders.

This device is ideally suited for demultiplexer applications. One of the two enable inputs is used as the data input, while the other is used as a data enable input.

A complete mux/demux operation on 16 bits for data distribution is illustrated in Figure 1 of the MC10161 data sheet.

- P_D = 315 ns typ/pkg (No Load)
- t_{pd} = 4.0 ns typ
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

TRUTH TABLE

INPUTS					OUTPUTS							
$\overline{E}0$	$\overline{E}1$	C	B	A	$\overline{Q0}$	$\overline{Q1}$	$\overline{Q2}$	$\overline{Q3}$	$\overline{Q4}$	$\overline{Q5}$	$\overline{Q6}$	$\overline{Q7}$
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	L	L	L	L	L	L	L	L

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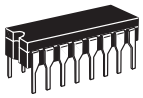
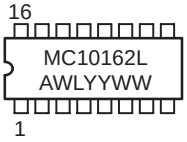
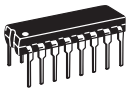
MARKING DIAGRAMS

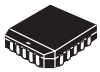


CDIP–16
L SUFFIX
CASE 620

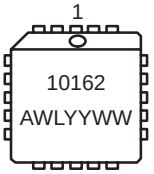




PDIP–16
P SUFFIX
CASE 648

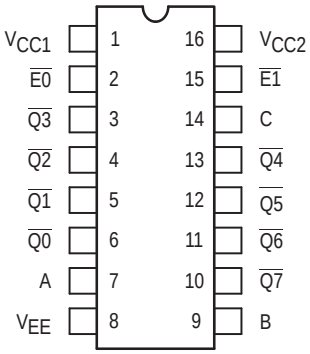


PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ORDERING INFORMATION

Device	Package	Shipping
MC10162L	CDIP–16	25 Units / Rail
MC10162P	PDIP–16	25 Units / Rail
MC10162FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		84		61	76		84	mAdc
Input Current	I_{inH}	14		350			220		220	μAdc
	I_{inL}	14	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	13	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	Vdc
Output Voltage Logic 0	V_{OL}	13 13	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	13	–1.080		–0.980			–0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	13 13		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{14+13-} t_{14-13+}	13 13	1.5 1.5	6.2 6.2	1.5 1.5	4.0 4.0	6.0 6.0	1.5 1.5	6.4 6.4	
Rise Time (20 to 80%)	t_{13+}	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5	
Fall Time (20 to 80%)	t_{13-}	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts)					
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8					8	1,16
Input Current	I_{inH}	14	14				8	1,16
	I_{inL}	14		14			8	1,16
Output Voltage Logic 1	V_{OH}	13	14				8	1,16
Output Voltage Logic 0	V_{OL}	13 13	2 15				8 8	1,16 1,16
Threshold Voltage Logic 1	V_{OHA}	13			14		8	1,16
Threshold Voltage Logic 0	V_{OLA}	13 13			2 15		8 8	1,16 1,16
Switching Times (50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	t_{14+13+} t_{14-13-}	13 13			14 14	13 13	8 8	1,16 1,16
Rise Time (20 to 80%)	t+	13			14	13	8	1,16
Fall Time (20 to 80%)	t–	13			14	13	8	1,16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

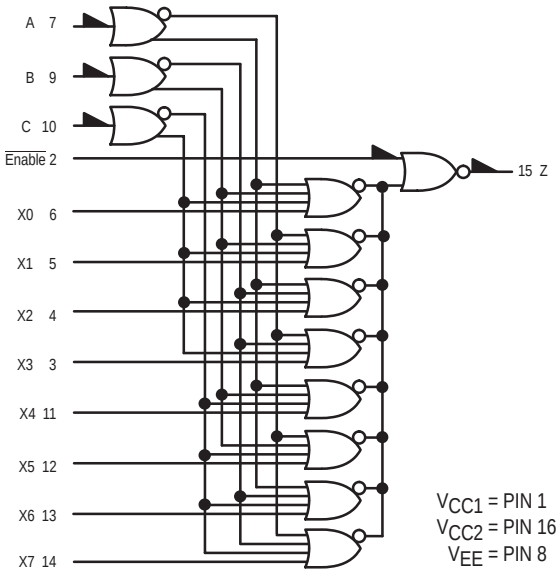
MC10164

8-Line Multiplexer

The MC10164 is a high speed, low power eight–channel data selector which routes data present at one–of–eight inputs to the output. The data is routed according to the three bit code present on the address inputs. An enable input is provided for easy bit expansion.

- P_D = 310 mW typ/pkg (No Load)
- t_{pd} = 3.0 ns typ (Data to Output)
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



TRUTH TABLE

	ADDRESS INPUTS			
ENABLE	C	B	A	Z
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	L

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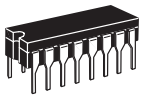
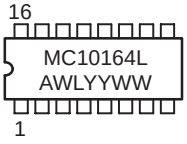
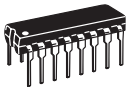
MARKING DIAGRAMS

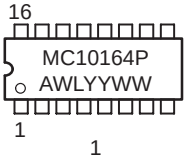


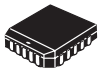
CDIP–16
L SUFFIX
CASE 620



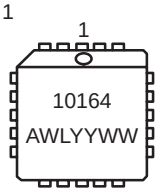


PDIP–16
P SUFFIX
CASE 648



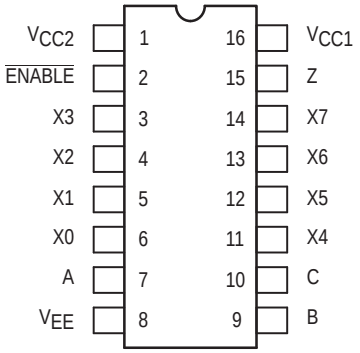


PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ORDERING INFORMATION

Device	Package	Shipping
MC10164L	CDIP–16	25 Units / Rail
MC10164P	PDIP–16	25 Units / Rail
MC10164FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Pin Under Test	Test Limits							Unit
				–30°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current		I_E	8		83		60	75		83	mAdc
Input Current		I_{inH}	2		425			265		265	μAdc
		I_{inL}	4	0.5		0.5			0.3		μAdc
Output Voltage	Logic 1	V_{OH}	15	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	Vdc
Output Voltage	Logic 0	V_{OL}	15	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	Vdc
Threshold Voltage	Logic 1	V_{OHA}	15	–1.080		–0.980			–0.910		Vdc
Threshold Voltage	Logic 0	V_{OLA}	15		–1.655			–1.630		–1.595	Vdc
Switching Times (50Ω Load)											ns
Propagation Delay		t_{4+15+}	15	1.5	4.9	1.5	3.0	4.7	1.6	5.0	
		t_{4-15-}	15	1.5	4.9	1.5	3.0	4.7	1.6	5.0	
		t_{7+15+}	15	1.9	6.5	2.0	4.0	6.2	2.2	6.7	
		t_{7-15-}	15	1.9	6.5	2.0	4.0	6.2	2.2	6.7	
		t_{2+15-}	15	0.9	3.5	1.0	2.0	3.1	1.0	3.3	
		t_{2-15+}	15	0.9	3.5	1.0	2.0	3.1	1.0	3.3	
Rise Time	(20 to 80%)	t+	15	0.9	3.3	1.1	2.0	3.3	1.2	3.6	
Fall Time	(20 to 80%)	t–	15	0.9	3.3	1.1	2.0	3.3	1.2	3.6	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
	TEST VOLTAGE VALUES (Volts)				
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1,16
Input Current		I_{inH}	2	4				8	1,16
		I_{inL}	4		4			8	1,16
Output Voltage	Logic 1	V_{OH}	15	4,9				8	1,16
Output Voltage	Logic 0	V_{OL}	15	9				8	1,16
Threshold Voltage	Logic 1	V_{OHA}	15	4,9			2	8	1,16
Threshold Voltage	Logic 0	V_{OLA}	15	9			2	8	1,16
Switching Times	(50Ω Load)			**+1.11V**		**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay		t_{4+15+}	15	9		4	15	8	1,16
		t_{4-15-}	15	9		4	15	8	1,16
		t_{7+15+}	15	5		7	15	8	1,16
		t_{7-15-}	15	5		7	15	8	1,16
		t_{2+15-}	15	7,5		2	15	8	1,16
		t_{2-15+}	15	7,5		2	15	8	1,16
Rise Time	(20 to 80%)	t+	15	9		4	15	8	1,16
Fall Time	(20 to 80%)	t–	15	9		4	15	8	1,16

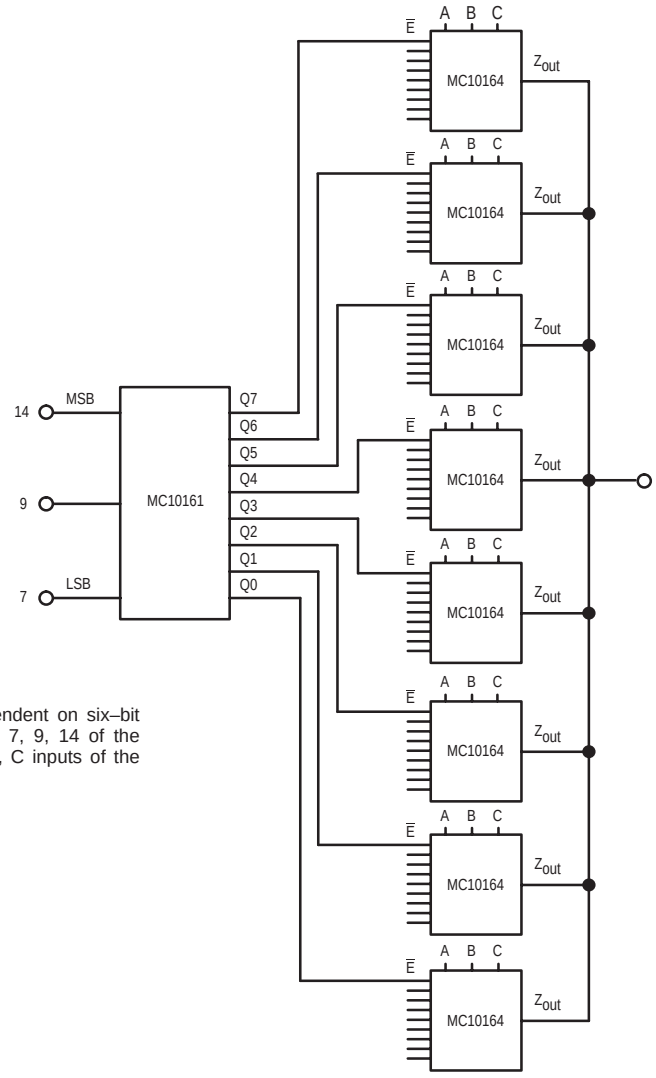
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

APPLICATION INFORMATION

The MC10164 can be used wherever data multiplexing or parallel to serial conversion is desirable. Full parallel gating permits equal delays through any data path. The output of the MC10164 incorporates a buffer gate with eight data inputs and an enable. A high level on the enable forces the output low. The MC10164 can be connected directly to a data bus, due to its open emitter output and output enable.

Figure 1 illustrates how a 1–of–64 line multiplexer can be built with eight MC10164's wire ORed at their outputs and one MC10161 to drive the enables on each multiplexer, without speed degradation over a single MC10164 being experienced.

FIGURE 1 — 1–OF–64 LINE MULTIPLEXER



The Bit chosen is dependent on six–bit code present on inputs 7, 9, 14 of the MC10161 and the A, B, C inputs of the MC10164.

MC10165

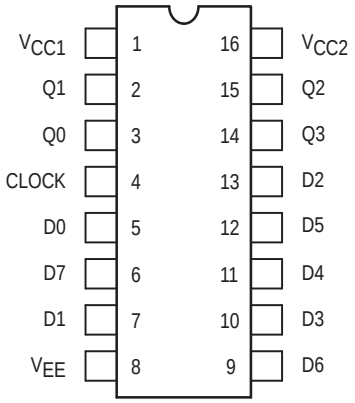
8-Input Priority Encoder

The MC10165 is a device designed to encode eight inputs to a binary coded output. The output code is that of the highest order input. Any input of lower priority is ignored. Each output incorporates a latch allowing synchronous operation. When the clock is low the outputs follow the inputs and latch when the clock goes high. This device is very useful for a variety of applications in checking system status in control processors, peripheral controllers, and testing systems.

The input is active when high, (e.g., the three binary outputs are low when input D0 is high). The Q3 output is high when any input is high. This allows direct extension into another priority encoder when more than eight inputs are necessary. The MC10165 can also be used to develop binary codes from random logic inputs, for addressing ROMs, RAMs, or for multiplexing data.

- P_D = 545 mW typ/pkg (No Load)
- t_{pd} = 4.5 ns typ (Data to Output)
- t_r, t_f = 2.0 ns typ (20%–80%)

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

TRUTH TABLE

DATA INPUTS								OUTPUTS			
D0	D1	D2	D3	D4	D5	D6	D7	Q3	Q2	Q1	Q0
H	X	X	X	X	X	X	X	H	L	L	L
L	H	X	X	X	X	X	X	H	L	L	H
L	L	H	X	X	X	X	X	H	L	H	L
L	L	L	H	X	X	X	X	H	L	H	H
L	L	L	L	H	X	X	X	H	H	L	L
L	L	L	L	L	H	X	X	H	H	L	H
L	L	L	L	L	L	H	X	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L

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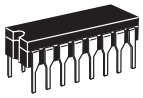
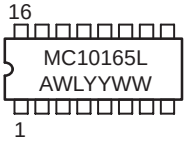
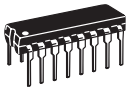
MARKING DIAGRAMS

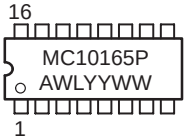


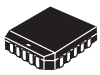
CDIP–16
L SUFFIX
CASE 620



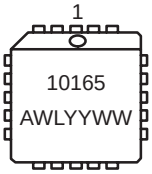


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

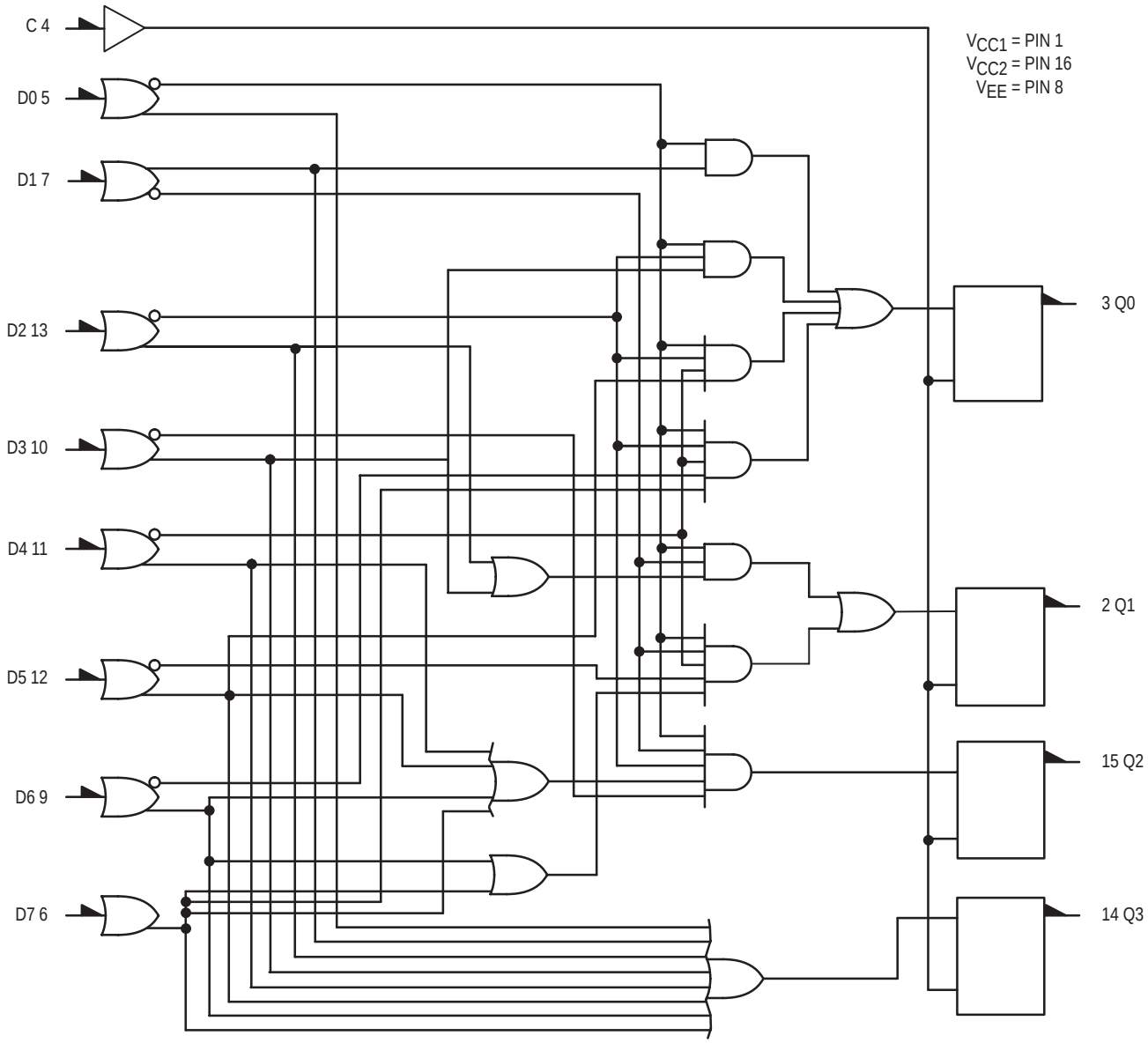


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10165L	CDIP–16	25 Units / Rail
MC10165P	PDIP–16	25 Units / Rail
MC10165FN	PLCC–20	46 Units / Rail

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		144		105	131		144	mAdc
Input Current	I_{inH}	4 5		390 350			245 220		245 220	µAdc
	I_{inL}	4 5	0.5 0.5		0.5 0.5			0.3 0.3		µAdc
Output Voltage Logic 1	V_{OH}	2 3 14 15	–1.060 –1.060 –1.060 –1.060	–0.890 –0.890 –0.890 –0.890	–0.960 –0.960 –0.960 –0.960		–0.810 –0.810 –0.810 –0.810	–0.890 –0.890 –0.890 –0.890	–0.700 –0.700 –0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3 14 15	–1.890 –1.890 –1.890 –1.890	–1.675 –1.675 –1.675 –1.675	–1.850 –1.850 –1.850 –1.850		–1.650 –1.650 –1.650 –1.650	–1.825 –1.825 –1.825 –1.825	–1.615 –1.615 –1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3 14 15	–1.080 –1.080 –1.080 –1.080		–0.980 –0.980 –0.980 –0.980			–0.910 –0.910 –0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3 14 15		–1.655 –1.655 –1.655 –1.655			–1.630 –1.630 –1.630 –1.630		–1.595 –1.595 –1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay Data Input	t_{5+14+} t_{5-14-} t_{7+3+} t_{11+15+} t_{13+2+}	14 14 3 15 2	2.0 2.0 2.0 2.0 2.0	7.0 7.0 7.0 7.0 7.0	3.0 3.0 3.0 3.0 3.0		7.0 7.0 7.0 7.0 7.0	2.0 2.0 2.0 2.0 2.0	8.0 8.0 8.0 8.0 8.0	
Clock Input	t_{4-3+} t_{4-3-} t_{4-14+} t_{4-14-}	3 (2.) 3 (3.) 14 (2.) 14 (3.)	1.5 1.5 1.5 1.5	4.5 4.5 4.5 4.5	2.0 2.0 2.0 2.0		4.0 4.0 4.0 4.0	1.5 1.5 1.5 1.5	4.5 4.5 4.5 4.5	
Setup Time	t_{setupH} t_{setupL}	3 3	6.0 6.0		6.0 6.0	3.4 3.0		6.0 6.0		
Hold Time	t_{holdH} t_{holdL}	3 3	1.0 1.0		1.0 1.0	–2.3 –2.7		1.0 1.0		
Rise Time (20 to 80%)	t_{3+}	3	1.1	3.5	1.1	2.0	3.3	1.1	3.5	
Fall Time (20 to 80%)	t_{3-}	3	1.1	3.5	1.1	2.0	3.3	1.1	3.5	

1. The same limit applies for all D type input pins. To test input currents for other D inputs, individually apply proper voltage to pin under test.
2. Output latched to low state prior to test.
3. Output latched to high state prior to test.

* To preserve reliable performance, the MC10165P (plastic packaged device only) is to be operated in ambient temperatures above 70°C only when 500 lfpm blown air or equivalent heat sinking is provided.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8					8	1, 16
Input Current	I_{inH}	4	4				8	1, 16
		5	5 (1.)				8	1, 16
	I_{inL}	4		4			8	1, 16
		5		5 (1.)			8	1, 16
Output Voltage Logic 1	V_{OH}	2	6	4			8	1, 16
		3	6	4			8	1, 16
		14	6	4			8	1, 16
		15	6	4			8	1, 16
Output Voltage Logic 0	V_{OL}	2		4			8	1, 16
		3		4			8	1, 16
		14		4			8	1, 16
		15		4			8	1, 16
Threshold Voltage Logic 1	V_{OHA}	2		4	6		8	1, 16
		3		4	6		8	1, 16
		14		4	6		8	1, 16
		15		4	6		8	1, 16
Threshold Voltage Logic 0	V_{OLA}	2		4		6	8	1, 16
		3		4		6	8	1, 16
		14		4		6	8	1, 16
		15		4		6	8	1, 16
Switching Times (50Ω Load)			**+1.11V**	**+0.31V**	**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0**
Propagation Delay Data Input	t_{5+14+}	14		4	5	14	8	1, 16
	$t_{5–14–}$	14		4	5	14	8	1, 16
	t_{7+3+}	3		4	7	3	8	1, 16
	t_{11+15+}	15		4	11	15	8	1, 16
	t_{13+2+}	2		4	13	2	8	1, 16
Clock Input	$t_{4–3+}$	3 (2.)	7		4	3	8	1, 16
	$t_{4–3–}$	3 (3.)			4	3	8	1, 16
	$t_{4–14+}$	14 (2.)	7		4	14	8	1, 16
	$t_{4–14–}$	14 (3.)			4	14	8	1, 16
Setup Time	t_{setupH}	3			4,7	3	8	1, 16
	t_{setupL}	3			4,7	3	8	1, 16
Hold Time	t_{holdH}	3			4,7	3	8	1, 16
	t_{holdL}	3			4,7	3	8	1, 16
Rise Time (20 to 80%)	t_{3+}	3		4	7	3	8	1, 16
Fall Time (20 to 80%)	$t_{3–}$	3		4	7	3	8	1, 16

1. The same limit applies for all D type input pins. To test input currents for other D inputs, individually apply proper voltage to pin under test.
2. Output latched to low state prior to test.
3. Output latched to high state prior to test.

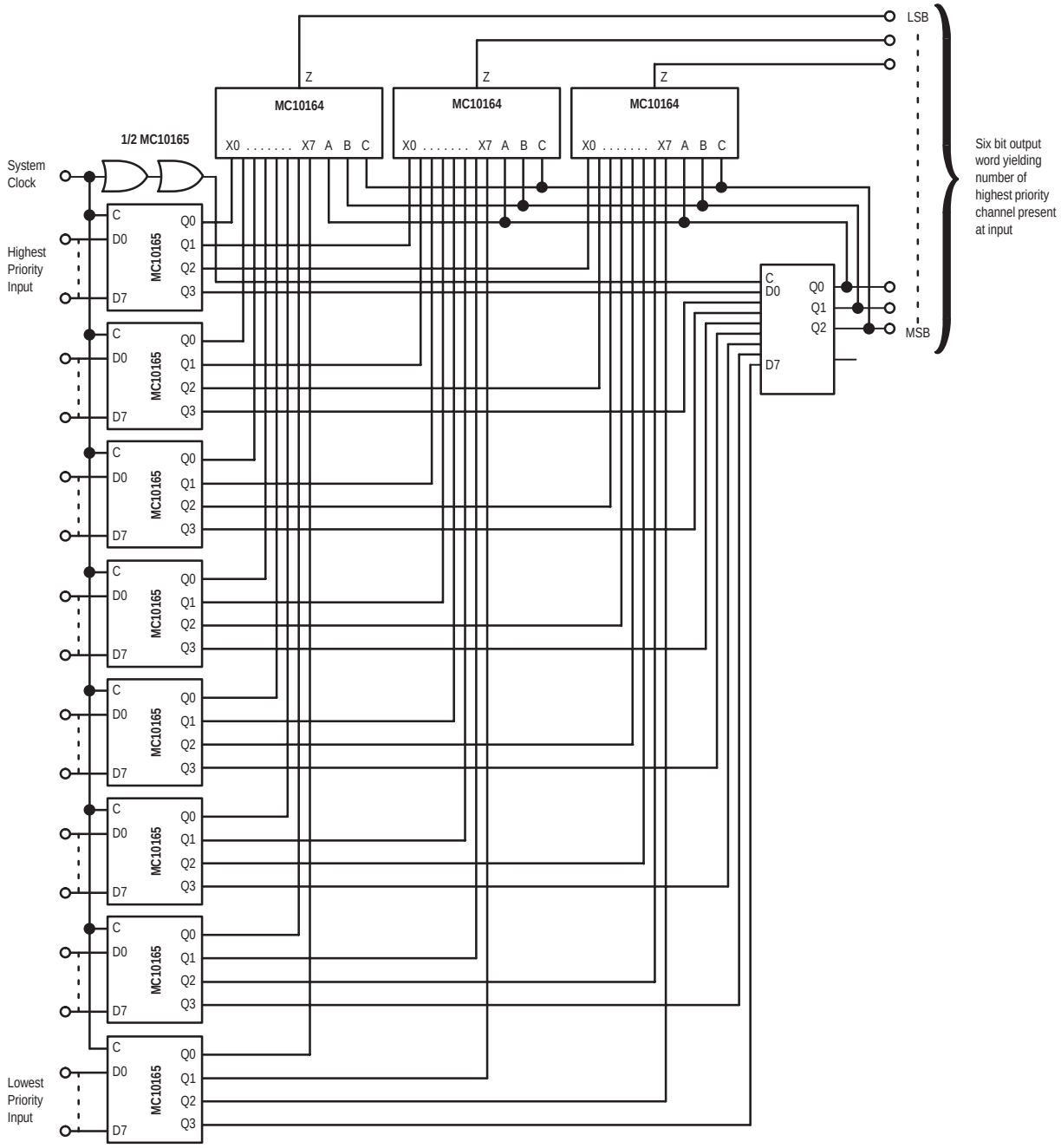
* To preserve reliable performance, the MC10165P (plastic packaged device only) is to be operated in ambient temperatures above 70°C only when 500 lfpm blown air or equivalent heat sinking is provided.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

APPLICATION INFORMATION

A typical application of the MC10165 is the decoding of system status on a priority basis. A 64 line priority encoder is shown in the figure below. System status lines are connected to this encoder such that, when a given condition exists, the respective input will be at a logic high level. This scheme will select the one of 64 different system conditions, as represented at the encoder inputs, which has priority in determining the next system operation to be performed. The binary code showing the address of the highest priority input present will appear at the encoder outputs to control other system logic functions.

64–LINE PRIORITY ENCODER



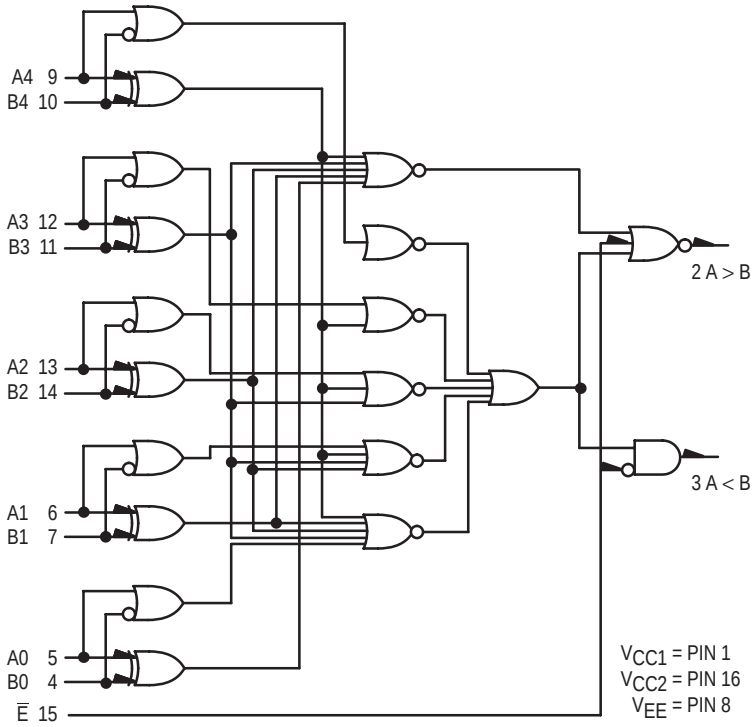
MC10166

5-Bit Magnitude Comparator

The MC10166 is a high speed expandable 5–bit comparator for comparing the magnitude of two binary words. Two outputs are provided: A < B and A > B. A = B can be obtained by NORing the two outputs with an additional gate. A high level on the enable function forces both outputs low. Multiple MC10166s may be used for larger word comparisons.

- P_D = 440 mW typ/pkg (No Load)
- t_{pd} =Data to Output 6.0 ns typ
- E to output 2.5 ns typ
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



TRUTH TABLE

Inputs			Outputs	
$\overline{E}$	A	B	A < B	A > B
H	X	X	L	L
L	Word A = Word B		L	L
L	Word A > Word B		L	H
L	Word A < Word B		H	L

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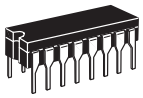
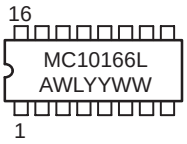
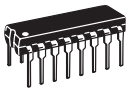
MARKING DIAGRAMS

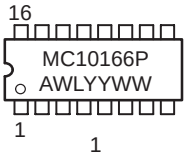


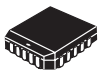
CDIP–16
L SUFFIX
CASE 620



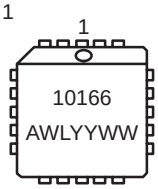


PDIP–16
P SUFFIX
CASE 648



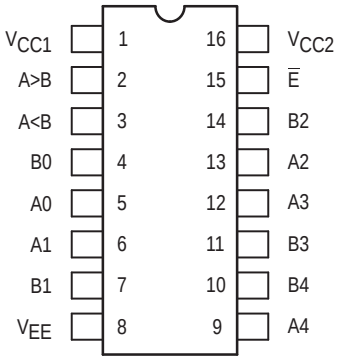


PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ORDERING INFORMATION

Device	Package	Shipping
MC10166L	CDIP–16	25 Units / Rail
MC10166P	PDIP–16	25 Units / Rail
MC10166FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		117		85	106		117	mAdc
Input Current	I_{inH}	5		350			220		220	μAdc
	I_{inL}	5	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	2 3	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Data to Output Delay	t_{9+2+} t_{9-2-} t_{11-2+} t_{11+2-} t_{7+3+} t_{7-3-}	2 2 2 2 3 3	1.0 1.0 1.0 1.0 1.0 1.0	8.0 8.0 8.0 8.0 8.0 8.0	1.0 1.0 1.0 1.0 1.0 1.0	6.0 6.0 6.0 6.0 6.0 6.0	7.6 7.6 7.6 7.6 7.6 7.6	1.0 1.0 1.0 1.0 1.0 1.0	8.4 8.4 8.4 8.4 8.4 8.4	
Enable to Output	t_{15-3+} t_{15+3-}	3 3	1.0 1.0	3.8 3.8	1.0 1.0	2.5 2.5	3.6 3.6	1.0 1.0	4.0 4.0	
Rise Time (20 to 80%)	t_{2+}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8	
Fall Time (20 to 80%)	t_{2-}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8	

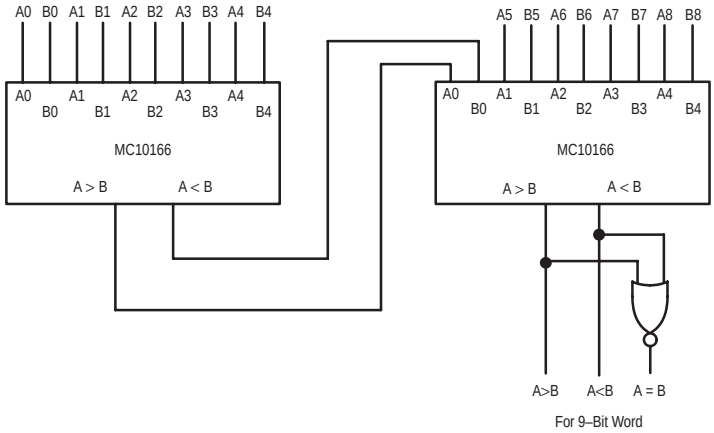
ELECTRICAL CHARACTERISTICS (continued)

			TEST VOLTAGE VALUES (Volts)					
		@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
		–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
		+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
		+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic	**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					**(V_{CC}) Gnd**
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8		4,7,10,11,14			8	1, 16
Input Current	I_{inH}	5	5				8	1, 16
	I_{inL}	5		5			8	1, 16
Output Voltage Logic 1	V_{OH}	2 3	5 4				8 8	1, 16 1, 16
Output Voltage Logic 0	V_{OL}	2 3	5, 15 4, 15				8 8	1, 16 1, 16
Threshold Voltage Logic 1	V_{OHA}	2 3	5 4			15 15	8 8	1, 16 1, 16
Threshold Voltage Logic 0	V_{OLA}	2 3	5 4		15 15		8 8	1, 16 1, 16
Switching Times (50Ω Load)			**+1.11V**		**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0**
Propagation Delay Data to Output	t_{9+2+}	2			9	2	8	1, 16
	t_{9-2-}	2			9	2	8	1, 16
	t_{11-2+}	2	12		11	2	8	1, 16
	t_{11+2-}	2	12		11	2	8	1, 16
	t_{7+3+}	3	6		7	3	8	1, 16
	t_{7-3-}	3	6		7	3	8	1, 16
Enable to Output	t_{15-3+}	3	10		15	3	8	1, 16
	t_{15+3-}	3	10		15	3	8	1, 16
Rise Time (20 to 80%)	t_{2+}	2			9	2	8	1, 16
Fall Time (20 to 80%)	t_{2-}	2			9	2	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

APPLICATION INFORMATION

FIGURE 1 — 9–BIT MAGNITUDE COMPARATOR



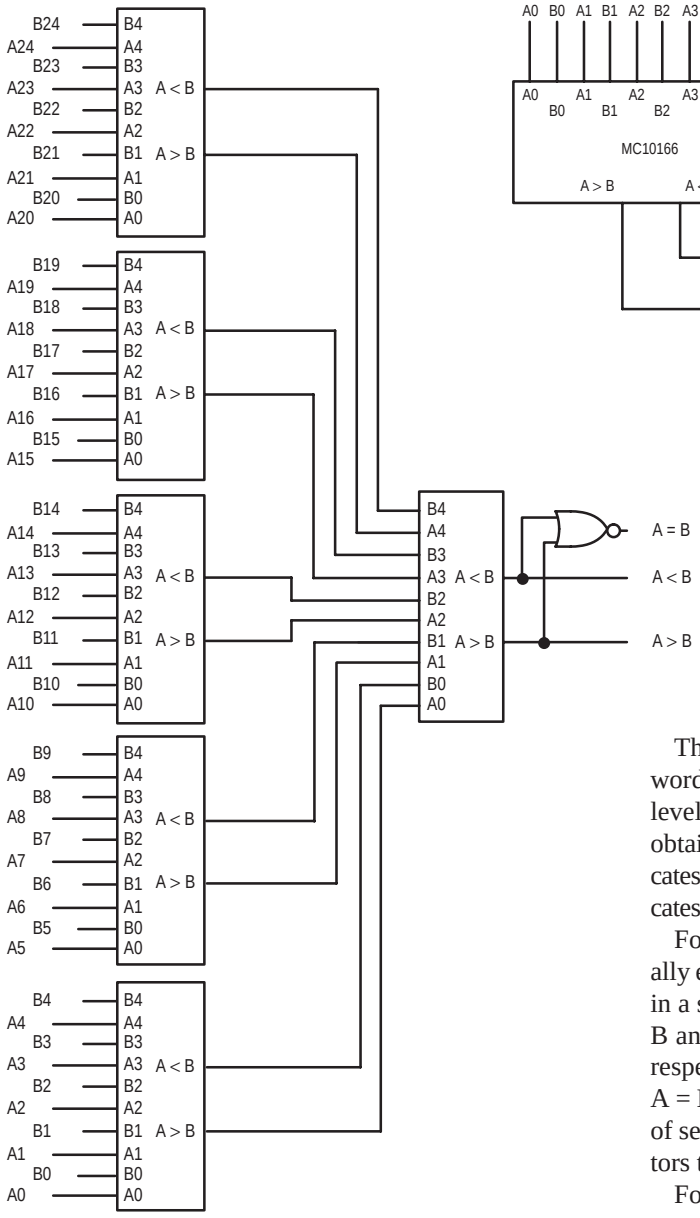


FIGURE 2 — 25–BIT MAGNITUDE COMPARATOR

The MC10166 compares the magnitude of two 5–bit words. Two outputs are provided which give a high level for A > B and A < B. The A = B function can be obtained by wire–ORing these outputs (a low level indicates A = B) or by NORing the outputs (a high level indicates A = B).

For longer word lengths, the MC10166 can be serially expanded or cascaded. Figure 1 shows two devices in a serial expansion for a 9–bit word length. The A > B and A < B outputs are fed to the A0 and B0 inputs respectively of the next device. The connection for an A = B output is also shown. The worst case delay time of serial expansion is equal to the number of comparators times the data–to–output delay.

For shorter delay times than possible with serial expansion, devices can be cascaded. Figure 2 shows a 25–bit cascaded comparator whose worst case delay is two data–to–output delays. The cascaded scheme can be extended to longer word lengths.

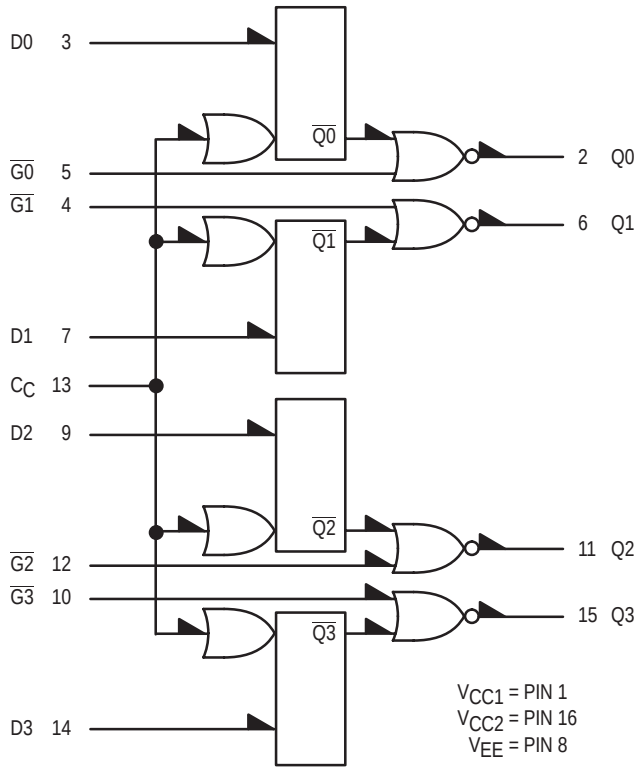
MC10168

Quad Latch

The MC10168 is a Quad Latch with common clocking to all four latches. Separate output enabling gates are provided for each latch, allowing direct wiring to a bus. When the clock is high, outputs will follow the D inputs. Information is latched on the negative–going transition of the clock.

- P_D = 310 mW typ/pkg (No Load)
- t_{pd} = G to Q = 2 ns typ
  D to Q = 3 ns typ
  C to Q = 4 ns typ
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	X	X	L
L	L	X	Q_n
L	H	L	L
L	H	H	H

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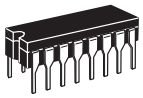
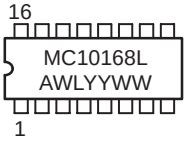
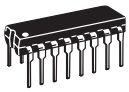
MARKING DIAGRAMS

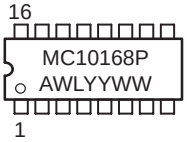


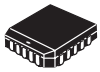
CDIP–16
L SUFFIX
CASE 620



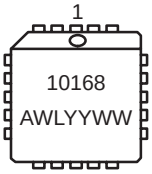


PDIP–16
P SUFFIX
CASE 648



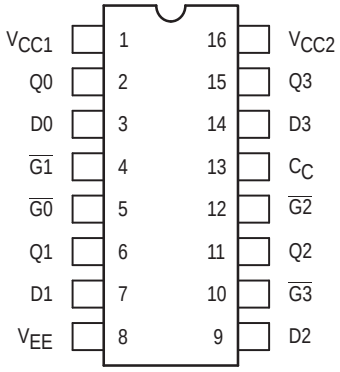


PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ORDERING INFORMATION

Device	Package	Shipping
MC10168L	CDIP–16	25 Units / Rail
MC10168P	PDIP–16	25 Units / Rail
MC10168FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		82		60	75		82	mAdc
Input Current	I_{inH}	3,7,9,14 4,5,10,12 13		390 425 460			245 265 290		245 265 290	µAdc
	I_{inL}	*	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	2 6	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 6	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 6	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 6		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay Data	t_{3+2+}	2	1.0	5.6	1.0	3.0	5.4	1.1	5.9	
Gate	t_{5-2+}	2	1.0	3.2	1.0	2.0	3.1	1.0	3.4	
Clock	t_{13+2+}	2	1.0	5.8	1.0	4.0	5.6	1.2	6.2	
Setup Time	t_{3+13+}	2	2.5		2.5			2.5		
Hold Time	t_{13+3+}	2	1.0		1.0			1.0		
Rise Time (20 to 80%)	t_{2+}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8	
Fall Time (20 to 80%)	t_{2-}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8	

* Individually test each input applying V_{IH} or V_{IL} to input under test.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
	TEST VOLTAGE VALUES (Volts)				
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8					8	1, 16
Input Current	I_{inH}	3,7,9,14 4,5,10,12 13	* * 13				8 8 8	1, 16 1, 16 1, 16
	I_{inL}	*		*			8	1, 16
Output Voltage Logic 1	V_{OH}	2 6	3, 13 7, 13				8 8	1, 16 1, 16
Output Voltage Logic 0	V_{OL}	2 6	3, 5 4, 7				8 8	1, 16 1, 16
Threshold Voltage Logic 1	V_{OHA}	2 6	13 13		3 7		8 8	1, 16 1, 16
Threshold Voltage Logic 0	V_{OLA}	2 6	13 13			3 7	8 8	1, 16 1, 16
Switching Times (50Ω Load)			**+1.11V**		**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay Data	t_{3+2+}	2			3	2	8	1, 16
Gate	t_{5-2+}	2			5	2	8	1, 16
Clock	t_{13+2+}	2			13	2	8	1, 16
Setup Time	t_{3+13+}	2					8	1, 16
Hold Time	t_{13+3+}	2					8	1, 16
Rise Time (20 to 80%)	t_{2+}	2			3	2	8	1, 16
Fall Time (20 to 80%)	t_{2-}	2			3	2	8	1, 16

* Individually test each input applying V_{IH} or V_{IL} to input under test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10170

9+2-Bit Parity Generator/ Checker

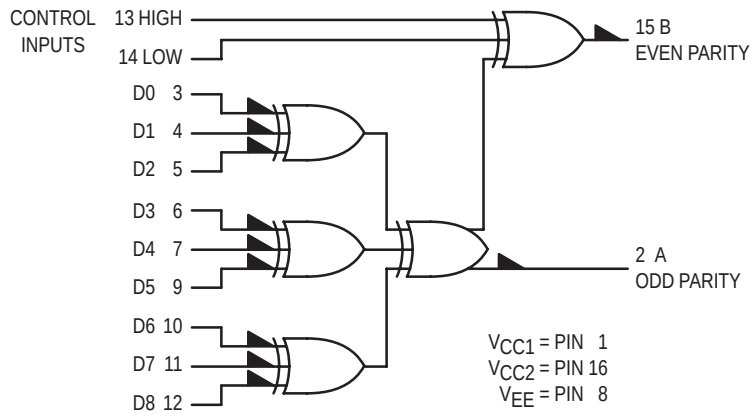
The MC10170 is a 11–bit parity circuit, which is segmented into 9 data bits and 2 control bits.

Output A generates odd parity on 9 bits; that is, Output A goes high for an odd number of high logic levels on the bit inputs in only 2 gate delays.

The Control Inputs can be used to expand parity to larger numbers of bits with minimal delay or can be used to generate even parity. To expand parity to larger words, the MC10170 can be used with the MC10160 or other MC10170's. The MC10170 can generate both even and odd parity.

- P_D = 300 mW typ/pkg (No Load)
- t_{pd} = 2.5 ns typ (Control Inputs to B Output)
  4.0 ns typ (Data Inputs to A Output)
  6.0 ns typ (Data Inputs to B Output)
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



INPUTS	OUTPUTS	
Sum of D Inputs at High Level	Odd Parity Output A	Even Parity Output B
Even	Low	High
Odd	High	Low

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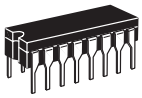
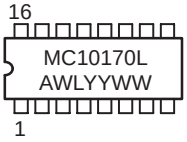
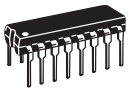
MARKING DIAGRAMS

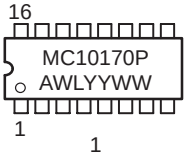


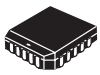
CDIP–16
L SUFFIX
CASE 620



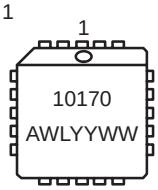


PDIP–16
P SUFFIX
CASE 648



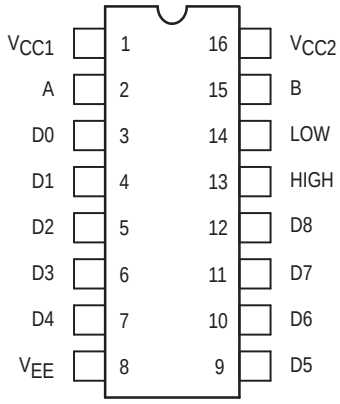


PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ORDERING INFORMATION

Device	Package	Shipping
MC10170L	CDIP–16	25 Units / Rail
MC10170P	PDIP–16	25 Units / Rail
MC10170FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		78		57	71		78	mAdc
Input Current	I_{inH}	3 5		350 350			200 220		220 220	μAdc
	I_{inL}	3	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	2 15	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 15	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 15	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 15		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{13+15+} t_{14-15-} t_{3+2-} t_{3-15+}	15 15 2 15	1.5 1.5 2.0 4.0	4.2 4.2 6.6 9.5	1.5 1.5 2.0 4.0	2.5 2.5 4.0 6.0	4.0 4.0 6.0 8.8	1.5 1.5 2.0 4.0	4.4 4.4 6.6 9.5	
Rise Time (20 to 80%)	t_{2+}	2	1.5	4.3	1.5	2.0	3.9	1.5	4.3	
Fall Time (20 to 80%)	t_{2-}	2	1.5	4.3	1.5	2.0	3.9	1.5	4.3	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C			–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C			–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C			–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					**(V_{CC}) Gnd**
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8						1, 16
Input Current		I_{inH}	3 5	3 5				8 8	1, 16 1, 16
		I_{inL}	3		3			8	1, 16
Output Voltage	Logic 1	V_{OH}	2 15	3, 4, 5 14				8 8	1, 16 1, 16
Output Voltage	Logic 0	V_{OL}	2 15	4, 5 13, 14				8 8	1, 16 1, 16
Threshold Voltage	Logic 1	V_{OHA}	2 15			5 13		8 8	1, 16 1, 16
Threshold Voltage	Logic 0	V_{OLA}	2 15				5 13	8 8	1, 16 1, 16
Switching Times	(50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0**
Propagation Delay		t_{13+15+}	15			13	15	8	1, 16
		t_{14-15-}	15			14	15	8	1, 16
		t_{3+2-}	2			3	2	8	1, 16
		t_{3-15+}	15			3	15	8	1, 16
Rise Time	(20 to 80%)	t_{2+}	2			3	2	8	1, 16
Fall Time	(20 to 80%)	t_{2-}	2			3	2	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

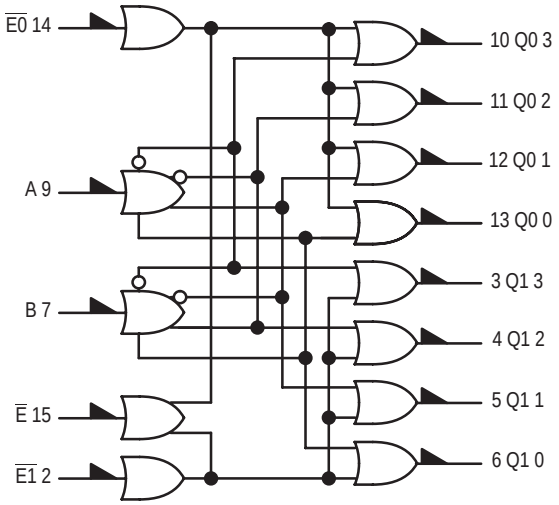
MC10171

Dual Binary to 1-4 Decoder (Low)

The MC10171 is a binary coded 2 line to dual 4 line decoder with selected outputs low. With either $\overline{E}0$ or $\overline{E}1$ high, the corresponding selected 4 outputs are high. The common enable $\overline{E}$, when high, forces all outputs high.

- P_D = 325 mW typ/pkg (No Load)
- t_{pd} = 4.0 ns typ
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

TRUTH TABLE

ENABLE INPUTS			INPUTS		OUTPUTS							
$\overline{E}$	$\overline{E0}$	$\overline{E1}$	A	B	Q10	Q11	Q12	Q13	Q00	Q01	Q02	Q03
L	L	L	L	L	L	H	H	H	L	H	H	H
L	L	L	L	H	H	L	H	H	H	L	H	H
L	L	L	H	L	H	H	L	H	H	H	L	H
L	L	L	H	H	H	H	H	L	H	H	H	L
L	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	L	L	L	H	H	H	H	H	H	H
H	X	X	X	X	H	H	H	H	H	H	H	H

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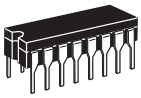
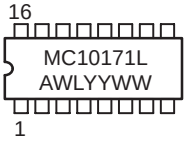
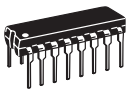
MARKING DIAGRAMS

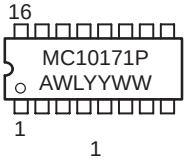


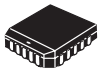
CDIP–16
L SUFFIX
CASE 620



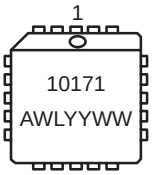


PDIP–16
P SUFFIX
CASE 648



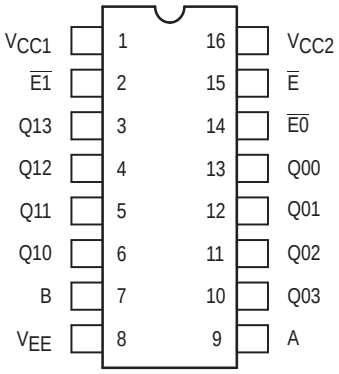


PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ORDERING INFORMATION

Device	Package	Shipping
MC10171L	CDIP–16	25 Units / Rail
MC10171P	PDIP–16	25 Units / Rail
MC10171FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		85		65	77		85	mAdc
Input Current	I_{inH}	14		350			220		220	μAdc
	I_{inL}	14	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	6 13	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	13	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	6 13	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	6 13		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{7+6+} t_{7-6-} t_{7+13+} t_{7-13-}	6 6 13 13	1.5 1.5 1.5 1.5	6.2 6.2 6.2 6.2	1.5 1.5 1.5 1.5	4.0 4.0 4.0 4.0	6.0 6.0 6.0 6.0	1.5 1.5 1.5 1.5	6.4 6.4 6.4 6.4	
Rise Time (20 to 80%)	t_{6+} t_{13+}	6 13	1.0 1.0	3.3 3.3	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.4 3.4	
Fall Time (20 to 80%)	t_{6-} t_{13-}	6 13	1.0 1.0	3.3 3.3	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.4 3.4	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C			–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C			–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C			–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**				**(V_{CC}) Gnd**
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8	2,7,9,14,15				8	1, 16
Input Current		I_{inH}	14	14				8	1, 16
		I_{inL}	14		14			8	1, 16
Output Voltage	Logic 1	V_{OH}	6 13	15 15				8 8	1, 16 1, 16
Output Voltage	Logic 0	V_{OL}	13		2,7,9,14,15			8	1, 16
Threshold Voltage	Logic 1	V_{OHA}	6 13			15 15		8 8	1, 16 1, 16
Threshold Voltage	Logic 0	V_{OLA}	6 13		2,9,14,15 2,7,14,15		7 9	8 8	1, 16 1, 16
Switching Times	(50Ω Load)				**+0.31V**	**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay		t_{7+6+} t_{7-6-} t_{7+13+} t_{7-13-}	6 6 13 13		2,9,14,15 2,9,14,15 2,9,14,15 2,9,14,15	7 7 7 7	6 6 13 13	8 8 8 8	1, 16 1, 16 1, 16 1, 16
Rise Time	(20 to 80%)	t_{6+} t_{13+}	6 13			7 7	6 13	8 8	1, 16 1, 16
Fall Time	(20 to 80%)	t_{6-} t_{13-}	6 13			7 7	6 13	8 8	1, 16 1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

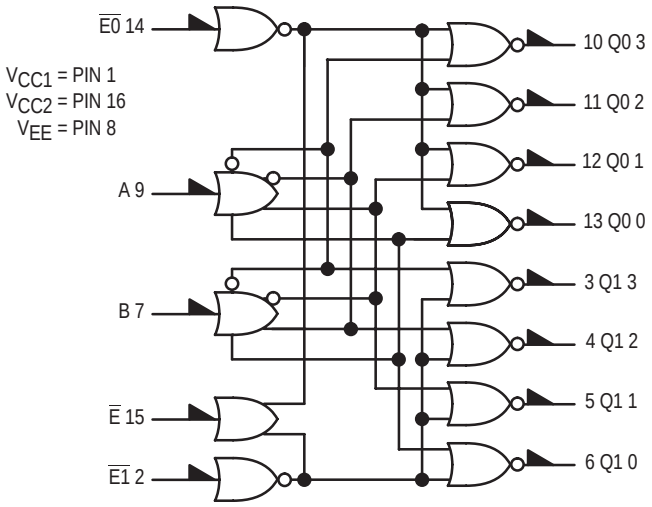
MC10172

Dual Binary to 1-4 Decoder (High)

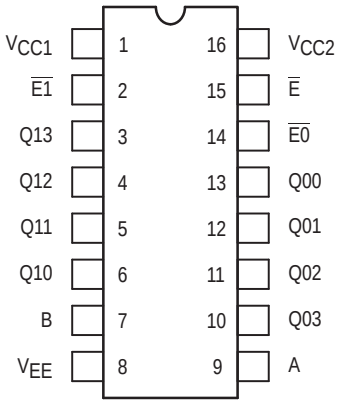
The MC10172 is a binary-coded 2 line to dual 4 line decoder with selected outputs high. With either $\overline{E0}$ or $\overline{E1}$ low, the corresponding selected 4 outputs are low. The common enable $\overline{E}$, when high, forces all outputs low.

- P_D = 325 mW typ/pkg (No Load)
- t_{pd} = 4.0 ns typ
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

TRUTH TABLE

$\overline{E}$	$\overline{E1}$	$\overline{E0}$	A	B	Q10	Q11	Q12	Q13	Q00	Q01	Q02	Q03
L	H	H	L	L	H	L	L	L	H	L	L	L
L	H	H	L	H	L	H	L	L	L	H	L	L
L	H	H	H	L	L	L	H	L	L	L	H	L
L	H	H	H	H	L	L	L	H	L	L	L	H
L	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	L	L	H	L	L	L	L	L	L	L
H	X	X	X	X	L	L	L	L	L	L	L	L

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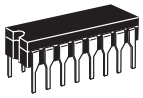
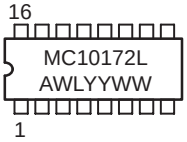
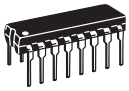
MARKING DIAGRAMS

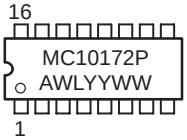


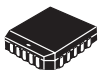
CDIP–16
L SUFFIX
CASE 620



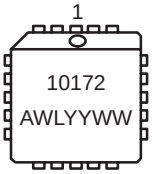


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10172L	CDIP–16	25 Units / Rail
MC10172P	PDIP–16	25 Units / Rail
MC10172FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		85		65	77		85	mAdc
Input Current	I_{inH}	14		350			220		220	μAdc
	I_{inL}	14	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	6 13	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	13	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	6 13	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	6 13		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{7+6-} t_{7-6+} t_{7+13-} t_{7-13+}	6 6 13 13	1.5 1.5 1.5 1.5	6.2 6.2 6.2 6.2	1.5 1.5 1.5 1.5	4.0 4.0 4.0 4.0	6.0 6.0 6.0 6.0	1.5 1.5 1.5 1.5	6.4 6.4 6.4 6.4	
Rise Time (20 to 80%)	t_{6+} t_{13+}	6 13	1.0 1.0	3.3 3.3	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.4 3.4	
Fall Time (20 to 80%)	t_{6-} t_{13-}	6 13	1.0 1.0	3.3 3.3	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.4 3.4	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C			–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C			–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C			–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					**(V_{CC}) Gnd**
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	14	14				8	1, 16
		I_{inL}	14		14			8	1, 16
Output Voltage	Logic 1	V_{OH}	6 13	2 14				8 8	1, 16 1, 16
Output Voltage	Logic 0	V_{OL}	13	15	2,7,9,14			8	1, 16
Threshold Voltage	Logic 1	V_{OHA}	6 13			2 14		8 8	1, 16 1, 16
Threshold Voltage	Logic 0	V_{OLA}	6 13		2,9,14 2,7,14		7 9	8 8	1, 16 1, 16
Switching Times	(50Ω Load)			**+1.11V**	**+0.31V**	**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay		t_{7+6-}	6	2	9, 14	7	6	8	1, 16
		t_{7-6+}	6	2	9, 14	7	6	8	1, 16
		t_{7+13-}	13	14	2, 9	7	13	8	1, 16
		t_{7-13+}	13	14	2,9	7	13	8	1, 16
Rise Time	(20 to 80%)	t_{6+}	6	2	9, 14	7	6	8	1, 16
		t_{13+}	13	14	2, 9	7	13	8	1, 16
Fall Time	(20 to 80%)	t_{6-}	6	2	9, 14	7	6	8	1, 16
		t_{13-}	13	14	2, 9	7	13	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

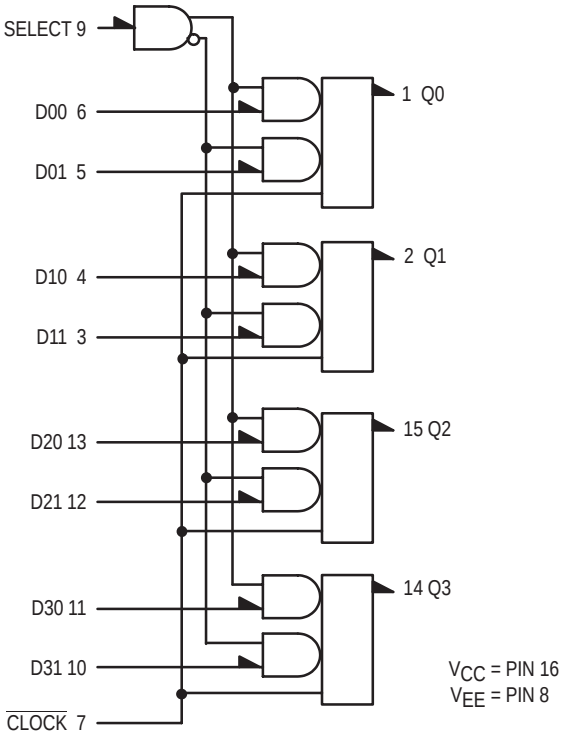
MC10173

Quad 2-Input Multiplexer/ Latch

The MC10173 is a quad two channel multiplexer with latch. It incorporates common clock and common data select inputs. The select input determines which data input is enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, D31. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

- P_D = 275 mW typ/pkg (No Load)
- t_{pd} = 2.5 ns typ
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



TRUTH TABLE

SELECT	$\overline{\text{CLOCK}}$	$Q0_{n+1}$
H	L	D00
L	L	D01
X	H	$Q0_n$

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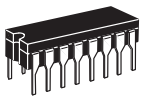
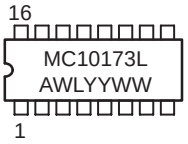
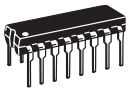
MARKING DIAGRAMS

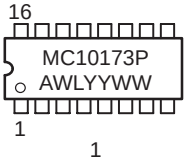


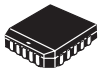
CDIP–16
L SUFFIX
CASE 620



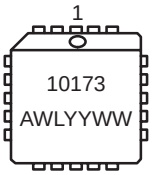


PDIP–16
P SUFFIX
CASE 648



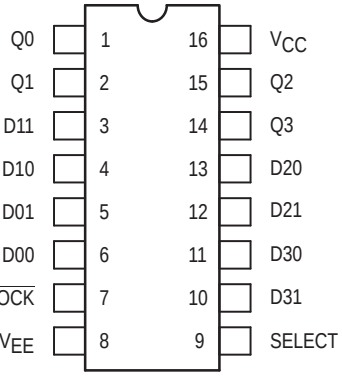


PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ORDERING INFORMATION

Device	Package	Shipping
MC10173L	CDIP–16	25 Units / Rail
MC10173P	PDIP–16	25 Units / Rail
MC10173FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		73			66		73	mAdc
Input Current	I_{inH}	5 6 7 9		470 470 400 400			295 295 250 250		295 295 250 250	μAdc
	I_{inL}	All	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	1 2	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	1 2	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	1 2	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	1 2		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay Data Input	t_{6+1+} t_{6-1-} t_{5+1+} t_{5-1-}	1 1 1 1	0.8 0.8 0.8 0.8	3.7 3.7 3.7 3.7	1.0 1.0 1.0 1.0	2.5 2.5 2.5 2.5	3.5 3.5 3.5 3.5	1.1 1.1 1.1 1.1	5.3 5.3 5.3 5.3	
Clock Input	t_{7-1+} t_{7-1-}	1 1	1.6 1.6	7.2 7.2	1.6 1.6	4.5 4.5	6.8 6.8	1.4 1.4	6.8 6.8	
Select Input	t_{9+1+} t_{9+1-} t_{9-1+} t_{9-1-}	1 1 1 1	1.1 1.1 1.1 1.1	6.2 6.2 6.2 6.2	1.3 1.3 1.3 1.3	3.5 3.5 3.5 3.5	5.7 5.7 5.7 5.7	1.2 1.2 1.2 1.2	6.7 6.7 6.7 6.7	
Setup TIme Data Input Select Input	t_{setup} t_{setup}	1 1	2.0 3.0		2.0 3.0	1.5 2.5		2.0 3.0		
Hold TIme Data Input Select Input	t_{hold} t_{hold}	1 1	2.5 1.5		2.5 1.5	0.0 –0.5		2.5 1.5		
Rise Time (20 to 80%)	t+	1	1.2	4.0	1.5	2.0	3.5	1.4	4.0	
Fall Time (20 to 80%)	t–	1	1.2	4.0	1.5	2.0	3.5	1.4	4.0	

* V_{ILmin} applied to each input pin, one at a time.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

TEST VOLTAGE VALUES (Volts)

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	16
Input Current			5	5				8	16
			6	6				8	16
			7	7				8	16
			9	9				8	16
		I_{inL}	All		*			8	16
Output Voltage	Logic 1	V_{OH}	1	6, 9	7			8	16
			2	5	7			8	16
Output Voltage	Logic 0	V_{OL}	1	9	7			8	16
			2		7			8	16
Threshold Voltage	Logic 1	V_{OHA}	1	9	7	6		8	16
			2		7	5		8	16
Threshold Voltage	Logic 0	V_{OLA}	1	9	7		6	8	16
			2		7		5	8	16
Switching Times	(50Ω Load)			**+1.11V**	**+0.31V**	**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	Data Input	t_{6+1+}	1	9	7	6	1	8	16
		$t_{6–1–}$	1	9	7	6	1	8	16
		t_{5+1+}	1		7	5	1	8	16
		$t_{5–1–}$	1		7	5	1	8	16
	Clock Input	$t_{7–1+}$	1			5, 7	1	8	16
		$t_{7–1–}$	1			5, 7	1	8	16
	Select Input	t_{9+1+}	1	6	7	9	1	8	16
		$t_{9+1–}$	1	5	7	9	1	8	16
		$t_{9–1+}$	1	5	7	9	1	8	16
		$t_{9–1–}$	1	6	7	9	1	8	16
Setup TIme	Data Input	t_{setup}	1			5, 7	1	8	16
	Select Input	t_{setup}	1	6		7, 9	1	8	16
Hold TIme	Data Input	t_{hold}	1			5, 7	1	8	16
	Select Input	t_{hold}	1	6		7, 9	1	8	16
Rise Time	(20 to 80%)	t+	1	5		7	1	8	16
Fall Time	(20 to 80%)	t–	1			7	1	8	16

* V_{ILmin} applied to each input pin, one at a time.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

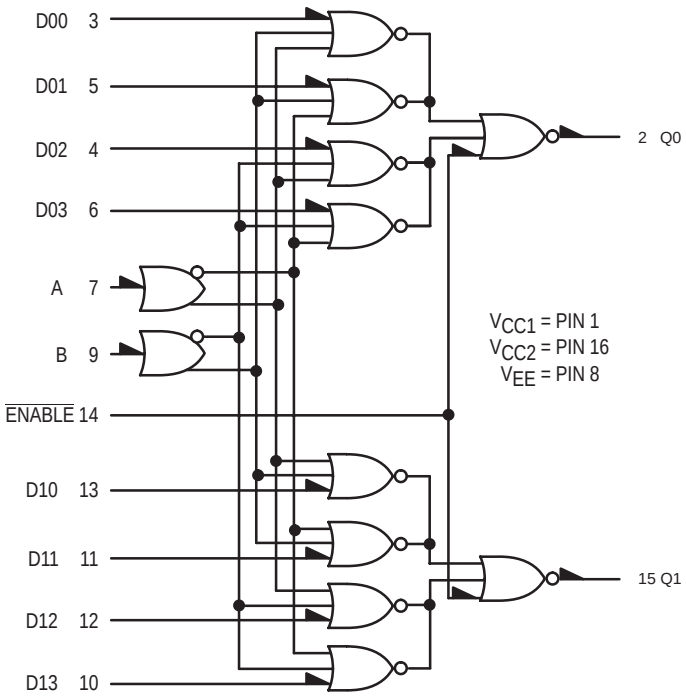
MC10174

Dual 4 to 1 Multiplexer

The MC10174 is a high speed dual channel multiplexer with output enable capability. The select inputs determine one of four active data inputs for each multiplexer. An output enable forces both outputs low when in the high state.

- P_D = 305 mW typ/pkg (No Load)
- t_{pd} = 3.5 ns typ (Dta to output)
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



TRUTH TABLE

ENABLE	ADDRESS INPUTS		OUTPUTS	
$\overline{E}$	B	A	Q0	Q1
H	X	X	L	L
L	L	L	D00	D10
L	L	H	D01	D11
L	H	L	D02	D12
L	H	H	D03	D13

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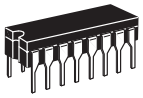
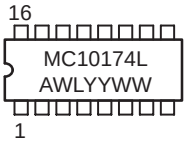
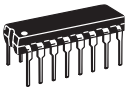
MARKING DIAGRAMS

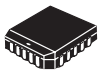


CDIP–16
L SUFFIX
CASE 620

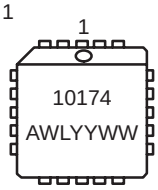




PDIP–16
P SUFFIX
CASE 648

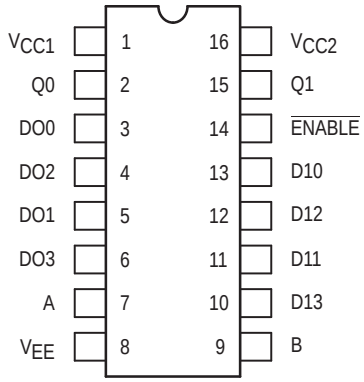


PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ORDERING INFORMATION

Device	Package	Shipping
MC10174L	CDIP–16	25 Units / Rail
MC10174P	PDIP–16	25 Units / Rail
MC10174FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Pin Under Test	Test Limits							Unit
				–30°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current		I_E	8		80		58	73	80		mAdc
Input Current		I_{inH}	4 14		350 525			220 330		220 330	µAdc
		I_{inL}	4	0.5		0.5			0.3		µAdc
Output Voltage	Logic 1	V_{OH}	15	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	Vdc
Output Voltage	Logic 0	V_{OL}	15	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	Vdc
Threshold Voltage	Logic 1	V_{OHA}	15	–1.080		–0.980			–0.910		Vdc
Threshold Voltage	Logic 0	V_{OLA}	15		–1.655			–1.630		–1.595	Vdc
Switching Times (50Ω Load)											ns
Propagation Delay		t_{13+15+}	15	1.4	5.0	1.5	3.5	4.7	1.4	5.0	
		$t_{13–15–}$	15	1.4	5.0	1.5	3.5	4.7	1.4	5.0	
		$t_{7+15–}$	15	1.9	6.6	2.0	5.0	6.2	2.1	6.6	
		$t_{7–15+}$	15	1.9	6.6	2.0	5.0	6.2	2.1	6.6	
		$t_{14+15–}$	15	1.0	3.3	1.0	2.0	3.1	0.9	3.4	
		$t_{14–15+}$	15	1.0	3.3	1.0	2.0	3.1	0.9	3.4	
Rise Time	(20 to 80%)	t+	15	1.0	3.4	1.1	2.0	3.3	1.1	3.6	
Fall Time	(20 to 80%)	t–	15	1.0	3.4	1.1	2.0	3.3	1.1	3.6	

ELECTRICAL CHARACTERISTICS (continued)

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts)				
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	4	4				8	1, 16
			14	14				8	1, 16
		I_{inL}	4		4			8	1, 16
Output Voltage	Logic 1	V_{OH}	15	13				8	1, 16
Output Voltage	Logic 0	V_{OL}	15	14				8	1, 16
Threshold Voltage	Logic 1	V_{OHA}	15			13		8	1, 16
Threshold Voltage	Logic 0	V_{OLA}	15			14		8	1, 16
Switching Times	(50Ω Load)			+1.11V		Pulse In	Pulse Out	–3.2 V	+2.0 V
Propagation Delay		t_{13+15+}	15			13	15	8	1, 16
		$t_{13–15–}$	15			13	15	8	1, 16
		$t_{7+15–}$	15	11		7	15	8	1, 16
		$t_{7–15+}$	15	11		7	15	8	1, 16
		$t_{14+15–}$	15	13		14	15	8	1, 16
		$t_{14–15+}$	15	13		14	15	8	1, 16
Rise Time	(20 to 80%)	t+	15	13		14	15	8	1, 16
Fall Time	(20 to 80%)	t–	15	13		14	15	8	1, 16

MC10175

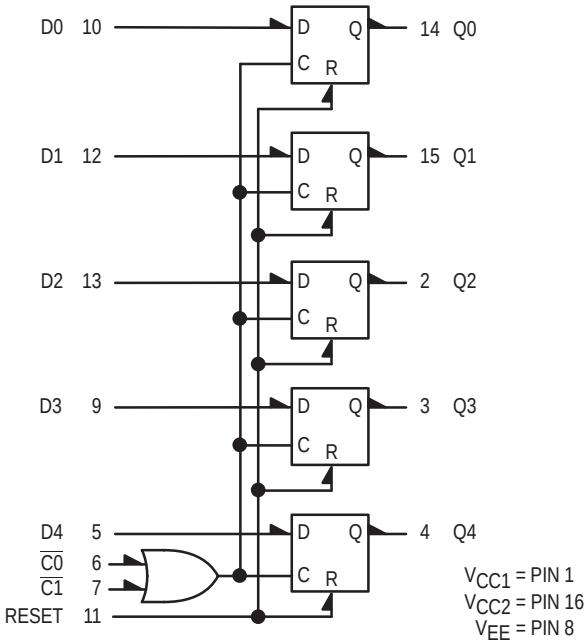
Quint Latch

The MC10175 is a high speed, low power quint latch. It features five D type latches with common reset and a common two–input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are “OR”ed together.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled only when the clock is in the high state.

- P_D = 400 mW typ/pkg (No Load)
- t_{pd} = 2.5 ns typ (Data to Output)
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



TRUTH TABLE

D	$\overline{C0}$	$\overline{C1}$	Reset	Q_{n+1}
L	L	L	X	L
H	L	L	X	H
X	H	X	L	Q n
X	X	H	L	Q n
X	H	X	H	L
X	X	H	H	L

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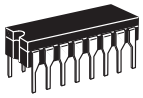
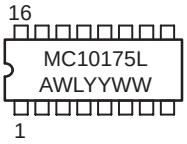
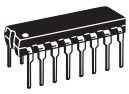
MARKING DIAGRAMS

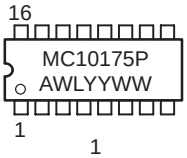


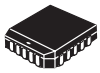
CDIP–16
L SUFFIX
CASE 620



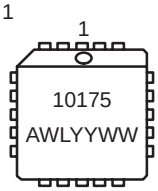


PDIP–16
P SUFFIX
CASE 648



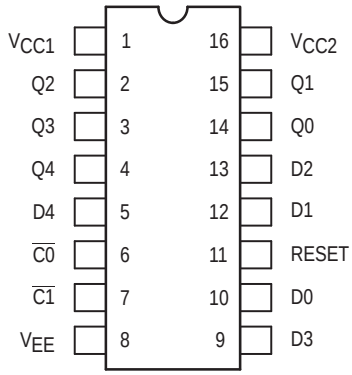


PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ORDERING INFORMATION

Device	Package	Shipping
MC10175L	CDIP–16	25 Units / Rail
MC10175P	PDIP–16	25 Units / Rail
MC10175FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		107		78	97		107	mAdc
Input Current	I_{inH}	6 7 10 11		460 460 460 1000			290 290 290 650		290 290 290 650	µAdc
	I_{inL}	All	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	14 15	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	14 15	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	14 15	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	14 15		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Data Input	t_{10+14+} t_{10-14-}	14 14	1.0 1.0	3.6 3.6	1.0 1.0		3.5 3.5	1.0 1.0	3.6 3.6	
Clock Input	t_{6-14+} t_{6-14-}	14 14	1.0 1.0	4.7 4.7	1.0 1.0		4.3 4.3	1.0 1.0	4.4 4.4	
Reset Input	t_{11+4-} t_{11+14-}	4 14	1.0 1.0	4.0 4.0	1.0 1.0		3.9 3.9	1.0 1.0	4.2 4.2	
Setup TIme Hold Time	t_{setup} t_{hold}	14 14	2.5 1.5		2.5 1.5			2.5 1.5		
Rise Time (20 to 80%)	t+	14	1.0	3.6	1.1		3.5	1.1	3.7	
Fall Time (20 to 80%)	t–	14	1.0	3.6	1.1		3.5	1.1	3.7	

1. Individually test each input; apply V_{ILmin} to pin under test.
2. Output latched to high logic state prior to test.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

TEST VOLTAGE VALUES (Volts)

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	6 7 10 11	6 7 10 11				8 8 8 8	1, 16 1, 16 1, 16 1, 16
		I_{inL}	All		Note 1.			8	1, 16
Output Voltage	Logic 1	V_{OH}	14 15	10 12	6 6			8 8	1, 16 1, 16
Output Voltage	Logic 0	V_{OL}	14 15		6, 10 6, 12			8 8	1, 16 1, 16
Threshold Voltage	Logic 1	V_{OHA}	14 15		6 6	10 12		8 8	1, 16 1, 16
Threshold Voltage	Logic 0	V_{OLA}	14 15		6 6		10 12	8 8	1, 16 1, 16
Switching Times	(50Ω Load)			**+1.11V**	**+0.31V**	**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
	Data Input	t_{10+14+} t_{10-14-}	14 14		6, 7 6, 7	10 10	14 14	8 8	1, 16 1, 16
	Clock Input	t_{6-14+} t_{6-14-}	14 14		7 7	10, 6 10, 6	14 14	8 8	1, 16 1, 16
	Reset Input	t_{11+4-} t_{11+14-}	4 14	5 10	6 6	7, 11 7, 11	4 (2.) 14 (2.)	8 8	1, 16 1, 16
Setup TIme Hold Time		t_{setup} t_{hold}	14 14		7 7	6, 10 6, 10	14 14	8 8	1, 16 1, 16
Rise Time	(20 to 80%)	t+	14		6, 7	10	14	8	1, 16
Fall Time	(20 to 80%)	t–	14		6, 7	10	14	8	1, 16

1. Individually test each input; apply V_{ILmin} to pin under test.
2. Output latched to high logic state prior to test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

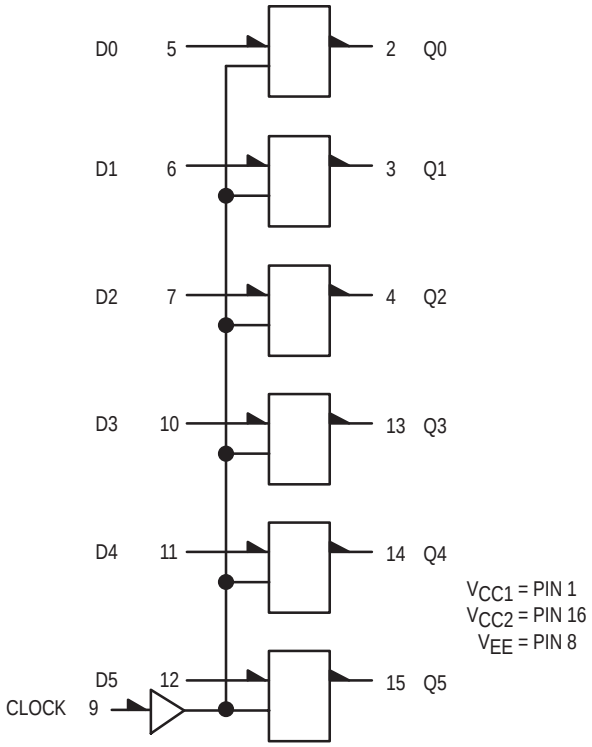
MC10176

Hex D Master/Slave Flip-Flop

The MC10176 contains six high-speed, master slave type “D” flip-flops. Clocking is common to all six flip-flops. Data is entered into the master when the clock is low. Master to slave data transfer takes place on the positive-going Clock transition. Thus, outputs may change only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device.

- P_D = 460 mW typ/pkg (No Load)
- f_{toggle} = 150 MHz (typ)
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	X	Q_n
H*	L	L
H*	H	H

*A clock H is a clock transition from a low to a high state.

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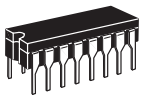
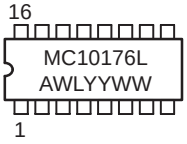
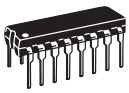
MARKING DIAGRAMS

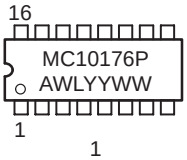


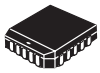
CDIP–16
L SUFFIX
CASE 620



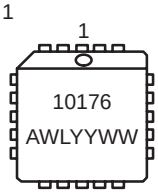


PDIP–16
P SUFFIX
CASE 648



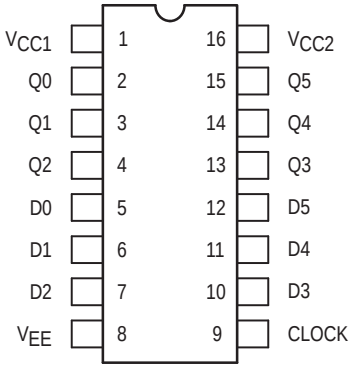


PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ORDERING INFORMATION

Device	Package	Shipping
MC10176L	CDIP–16	25 Units / Rail
MC10176P	PDIP–16	25 Units / Rail
MC10176FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		121		88	110		121	mAdc
Input Current	I_{inH}	5 9		350 495			220 310		220 310	μAdc
	I_{inL}	5 9	0.5 0.5		0.5 0.5			0.3 0.3		μAdc
Output Voltage Logic 1	V_{OH}	2† 15†	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2† 15†	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2† 15†	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2† 15†		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load) Clock Input										ns
Propagation Delay	t_{9+2+} t_{9+2-}	2 2	1.6 1.6	4.6 4.6	1.6 1.6		4.5 4.5	1.6 1.6	5.0 5.0	
Rise Time (20 to 80%)	t_{2+}	2	1.0	4.1	1.1		4.0	1.1	4.4	
Fall Time (20 to 80%)	t_{2-}	2	1.0	4.1	1.1		4.0	1.1	4.4	
Setup Time	t_{setup}	2	2.5		2.5			2.5		ns
Hold Time	t_{hold}	2	1.5		1.5			1.5		ns
Toggle Frequency (Max)	f_{tog}	2	125		125	150		125		MHz

† Output level to be measured after a clock pulse has been applied to the C Input (Pin 9)

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C			–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C			–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C			–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					**(V_{CC}) Gnd**
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	5 9	5 9				8 8	1, 16 1, 16
		I_{inL}	5 9		5 9			8 8	1, 16 1, 16
Output Voltage	Logic 1	V_{OH}	2† 15†	5 12				8 8	1, 16 1, 16
Output Voltage	Logic 0	V_{OL}	2† 15†		5 12			8 8	1, 16 1, 16
Threshold Voltage	Logic 1	V_{OHA}	2† 15†			5 12		8 8	1, 16 1, 16
Threshold Voltage	Logic 0	V_{OLA}	2† 15†				5 12	8 8	1, 16 1, 16
Switching Times	(50Ω Load)			**+1.11Vdc**	**+0.31V**	**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Clock Input Propagation Delay		t_{9+2+} t_{9+2-}	2 2			5, 9 5, 9	2 2	8 8	1, 16 1, 16
Rise Time	(20 to 80%)	t_{2+}	2			5, 9	2	8	1, 16
Fall Time	(20 to 80%)	t_{2-}	2			5, 9	2	8	1, 16
Setup Time		t_{setup}	2			5, 9	2	8	1, 16
Hold Time		t_{hold}	2			5, 9	2	8	1, 16
Toggle Frequency (Max)		f_{tog}	2					8	1, 16

† Output level to be measured after a clock pulse has been applied to the C Input (Pin 9)

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10178

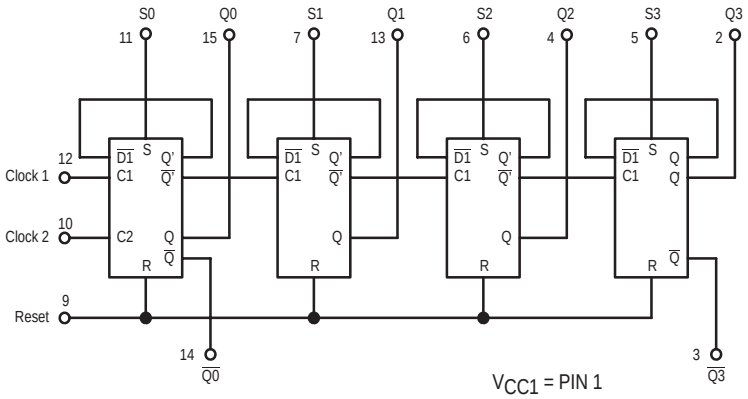
Binary Counter

The MC10178 is a four–bit counter capable of divide–by–two, divide–by–four, divide–by–eight or a divide–by–sixteen function.

Clock inputs trigger on the positive going edge of the clock pulse. Set and Reset inputs override the clock, allowing asynchronous “set” or “clear.” Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

- P_D = 370 mW typ/pkg (No Load)
- f_{toggle}=150 MHz (typ)
- t_r, t_f = 2.7 ns typ (20%–80%)

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

TRUTH TABLE

INPUTS							OUTPUTS			
R	S0	S1	S2	S3	C1	C2	Q0	Q1	Q2	Q3
H	L	L	L	L	X	X	L	L	L	L
L	H	H	H	H	X	X	H	H	H	H
L	L	L	L	L	H	X	No Count			
L	L	L	L	L	X	H	No Count			
L	L	L	L	L	**		L	L	L	L
L	L	L	L	L	**		H	L	L	L
L	L	L	L	L	**		L	H	L	L
L	L	L	L	L	**		H	H	L	L
L	L	L	L	L	**		L	L	H	L
L	L	L	L	L	**		H	L	H	L
L	L	L	L	L	**		L	H	H	L
L	L	L	L	L	**		H	H	H	L
L	L	L	L	L	**		L	L	L	H
L	L	L	L	L	**		H	L	L	H
L	L	L	L	L	**		L	H	L	H
L	L	L	L	L	**		H	H	L	H
L	L	L	L	L	**		L	L	H	H
L	L	L	L	L	**		H	L	H	H
L	L	L	L	L	**		L	H	H	H
L	L	L	L	L	**		H	H	H	H

** V_{IL} → V_{IH} Clock transition from V_{IL} to V_{IH} may be applied to C_1 or C_2 or both for same effect.

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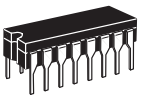
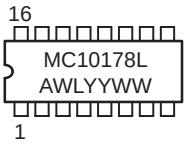
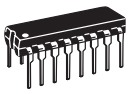
MARKING DIAGRAMS

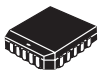


CDIP–16
L SUFFIX
CASE 620

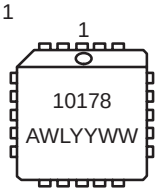




PDIP–16
P SUFFIX
CASE 648

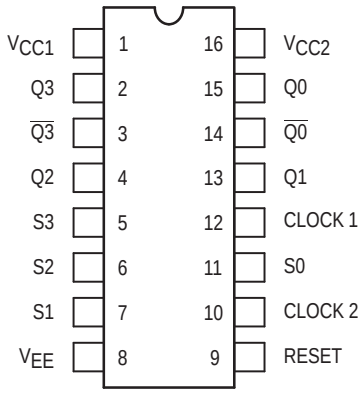


PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ORDERING INFORMATION

Device	Package	Shipping
MC10178L	CDIP–16	25 Units / Rail
MC10178P	PDIP–16	25 Units / Rail
MC10178FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		97			88		97	mAdc
Input Current	I_{inH}	12 11 9		390 350 650			245 220 410		245 220 410	µAdc
	I_{inL}	*	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	14 15	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	14 15	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	3 14 15	–1.080 –1.080 –1.080		–0.980 –0.980 –0.980			–0.910 –0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	3 14 15		–1.655 –1.655 –1.655			–1.630 –1.630 –1.630		–1.595 –1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Clock Input Delay	t_{12+15+} t_{12-13-} t_{12+4-} t_{12-3+}	15 13 4 3	1.4 1.9 2.9 3.9	5.0 9.4 12.3 14.9	1.5 2.0 3.0 4.0	3.5 6.0 8.5 11.0	4.8 9.2 12.0 14.5	1.5 2.0 3.0 4.0	5.3 9.8 12.8 15.5	
Rise Time (20 to 80%)	t_{15+}	15	1.1	4.7	1.1	2.5	4.5	1.1	5.0	
Fall Time (20 to 80%)	t_{15-}	15	1.1	4.7	1.1	2.5	4.5	1.1	5.0	
Set Input Reset Input	t_{11-15+} t_{9-15+}	15 15	1.4 1.4	5.2 5.2	1.5 1.5		5.0 5.0	1.5 1.5	5.5 5.5	
Counting Frequency	f_{count}	15	125		125	150		125		MHz

* Individually test each input applying V_{IL} to input under test.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
	TEST VOLTAGE VALUES (Volts)				
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8	9				8	1, 16
Input Current	I_{inH}	12	12				8	1, 16
		11	11				8	1, 16
		9	9				8	1, 16
	I_{inL}	*		*			8	1, 16
Output Voltage Logic 1	V_{OH}	14	9				8	1, 16
		15	11				8	1, 16
Output Voltage Logic 0	V_{OL}	14	11				8	1, 16
		15	9				8	1, 16
Threshold Voltage Logic 1	V_{OHA}	3			5		8	1, 16
		14			11		8	1, 16
		15			9		8	1, 16
Threshold Voltage Logic 0	V_{OLA}	3				5	8	1, 16
		14				11	8	1, 16
		15				9	8	1, 16
Switching Times (50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay Data Input	t_{12+15+}	15			12	15	8	1, 16
	t_{12-13-}	13			12	13	8	1, 16
	t_{12+4-}	4			12	4	8	1, 16
	t_{12-3+}	3			12	3	8	1, 16
Rise Time (20 to 80%)	t+	15			12	15	8	1, 16
Fall Time (20 to 80%)	t–	15			12	15	8	1, 16
Set Input	t_{11-15+}	15			11	15	8	1, 16
Reset Input	t_{9-15+}	15			9	15	8	1, 16
Counting Frequency	f_{count}	15			12	15	8	1, 16

* Individually test each input applying V_{IL} to input under test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10181

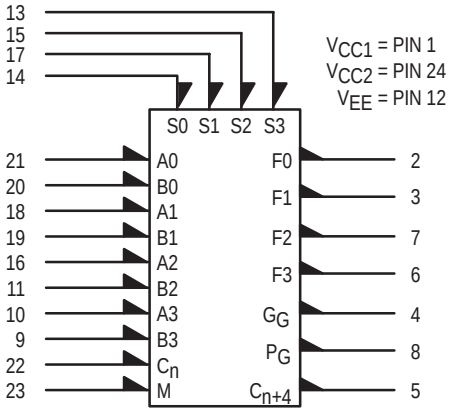
4-Bit Arithmetic Logic Unit/ Function Generator

The MC10181 is a high–speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two four–bit words. Full internal carry is incorporated for ripple through operation.

Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast operations on very long words using a second order look ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

- P_D = 600 mW typ/pkg (No Load)
- t_{pd} (typ): A1 to F = 6.5 ns
- C_n to C_{n+4} = 3.1 ns
- A1 to P_G = 5.0 ns
- A1 to G_G = 4.5 ns
- A1 to C_{n+4} = 5.0

LOGIC DIAGRAM



Function Select				Logic Functions M is High C = D.C.	Arithmetic Operation M is Low C_n is low
S3	S2	S1	S0	F	F
L	L	L	L	F = $\overline{A}$	F = A
L	L	L	H	F = $\overline{A}$ + $\overline{B}$	F = A plus (A • $\overline{B}$)
L	L	H	L	F = $\overline{A}$ + B	F = A plus (A • B)
L	L	H	H	F = Logical “1”	F = A times 2
L	H	L	L	F = $\overline{A}$ • $\overline{B}$	F = (A + B) plus 0
L	H	L	H	F = $\overline{B}$	F = (A + B) plus (A • $\overline{B}$)
L	H	H	L	F = A $\odot$ B	F = A plus B
L	H	H	H	F = A + $\overline{B}$	F = A plus (A + B)
H	L	L	L	F = $\overline{A}$ • B	F = (A + $\overline{B}$) plus 0
H	L	L	H	F = A $\oplus$ B	F = A minus B minus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) plus (A • B)
H	L	H	H	F = A + B	F = A plus (A + $\overline{B}$)
H	H	L	L	F = Logical “0”	F = minus 1 (two’s complement)
H	H	L	H	F = A • $\overline{B}$	F = (A • $\overline{B}$) minus 1
H	H	H	L	F = A • B	F = (A • B) minus 1
H	H	H	H	F = A	F = A minus 1

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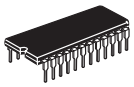
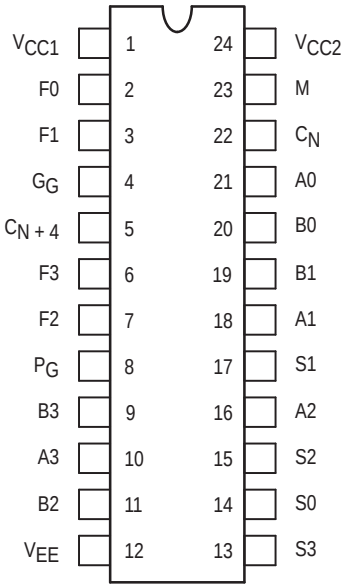
MARKING DIAGRAMS



CDIP–24
L SUFFIX
CASE 623

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

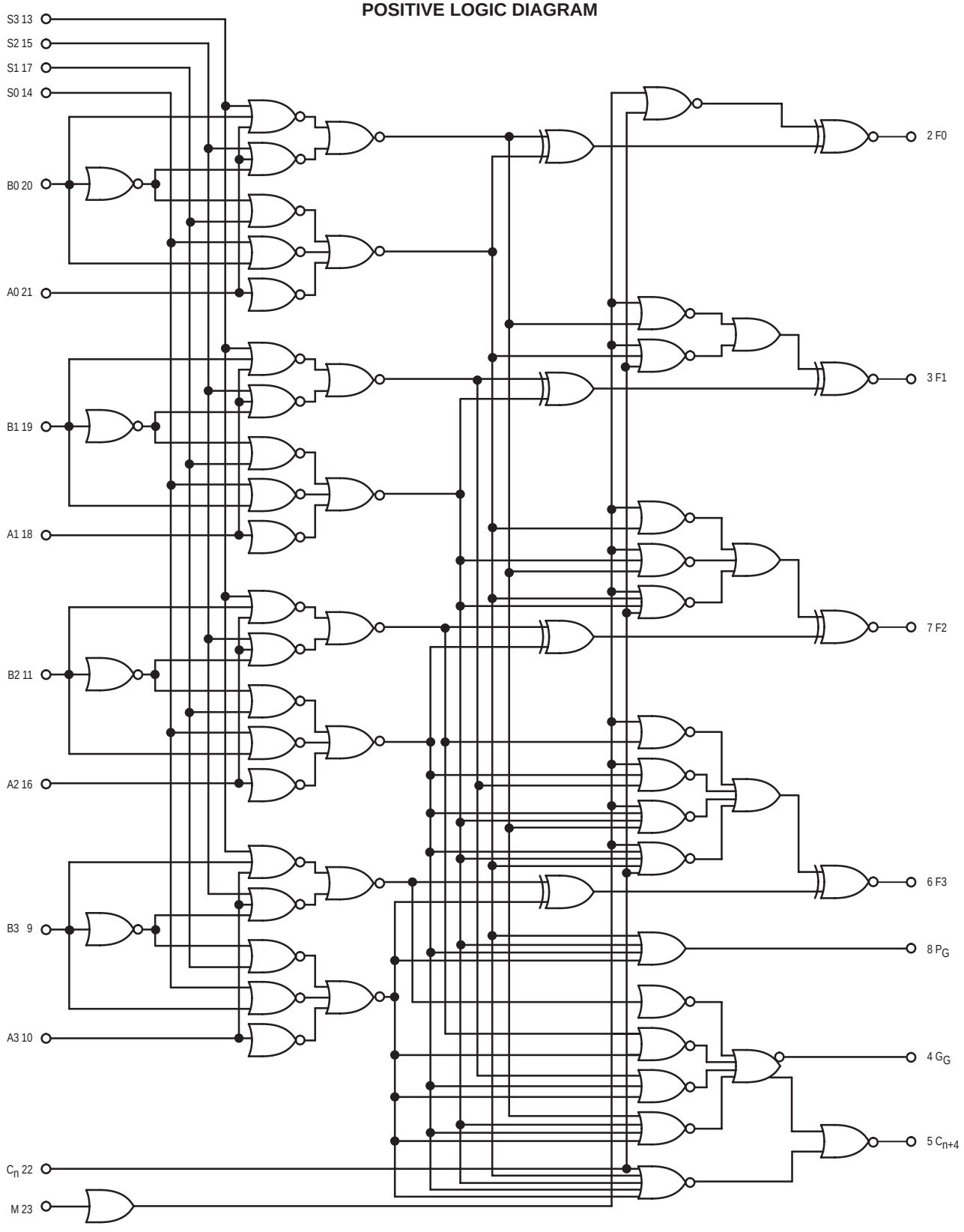
PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC10181L	CDIP–24	15 Units / Rail

POSITIVE LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	12		159			145		159	mAdc
Input Current	I_{inH}	9		390			245		245	µAdc
		10		350			220		220	
		11		390			245		245	
		13		320			200		200	
		14		425			265		265	
		15		425			265		265	
		16		350			220		220	
		17		425			265		265	
		18		350			220		220	
		19		390			245		245	
		20		390			245		245	
		21		350			220		220	
		22		460			290		290	
		23		320			200		200	
Input Leakage Current	I_{inL}	9	0.5		0.5			0.3		µAdc
		10	0.5		0.5			0.3		
		11	0.5		0.5			0.3		
		13	0.5		0.5			0.3		
		14	0.5		0.5			0.3		
		15	0.5		0.5			0.3		
		16	0.5		0.5			0.3		
		17	0.5		0.5			0.3		
		18	0.5		0.5			0.3		
		19	0.5		0.5			0.3		
		20	0.5		0.5			0.3		
		21	0.5		0.5			0.3		
		22	0.5		0.5			0.3		
		23	0.5		0.5			0.3		
Output Voltage Logic 1	V_{OH}	*	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	Vdc
Output Voltage Logic 0	V_{OL}	*	–2.000	–1.675	–1.990		–1.650	–1.920	–1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	*	–1.080		–0.980			–0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	*		–1.655			–1.630		–1.595	Vdc

* Test all input–output combinations according to Function Table.

** For threshold level test, apply threshold input level to only one input pin at a time.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C			–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C			–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C			–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					**(V_{CC}) Gnd**
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	12					12	1, 24
Input Current		I_{inH}	9	9				12	1, 24
			10	10				12	1, 24
			11	11				12	1, 24
			13	13				12	1, 24
			14	14				12	1, 24
			15	15				12	1, 24
			16	16				12	1, 24
			17	17				12	1, 24
			18	18				12	1, 24
			19	19				12	1, 24
			20	20				12	1, 24
			21	21				12	1, 24
			22	22				12	1, 24
			23	23				12	1, 24
Input Leakage Current		I_{inL}	9		9			12	1, 24
			10		10			12	1, 24
			11		11			12	1, 24
			13		13			12	1, 24
			14		14			12	1, 24
			15		15			12	1, 24
			16		16			12	1, 24
			17		17			12	1, 24
			18		18			12	1, 24
			19		19			12	1, 24
			20		20			12	1, 24
			21		21			12	1, 24
			22		22			12	1, 24
			23		23			12	1, 24
Output Voltage	Logic 1	V_{OH}	*	*	*			12	1, 24
Output Voltage	Logic 0	V_{OL}	*	*	*			12	1, 24
Threshold Voltage	Logic 1	V_{OHA}	*			**	**	12	1, 24
Threshold Voltage	Logic 0	V_{OLA}	*			**	**	12	1, 24

* Test all input–output combinations according to Function Table.

** For threshold level test, apply threshold input level to only one input pin at a time.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

Characteristic	Symbol	Input	Output	Conditions†	AC Switching Characteristics							
					–30°C *		+25°C			+85°C *		
					Min	Max	Min	Typ	Max	Min	Max	Unit
Propagation Delay	t++,t– –	C_n	C_{n+4}	A0,A1,A2,A3	1.0	5.1	1.1	3.1	5.0	1.1	5.4	ns
Rise Time, Fall Time	t+,t–	C_n	C_{n+4}	A0,A1,A2,A3	1.0	3.2	1.0	2.0	3.0	1.0	3.2	ns
Propagation Delay	t++,t+–	C_n	F1	A0	1.7	7.2	2.0	4.5	7.0	2.0	7.5	ns
	t–+,t– –	C_n	F1	A0	1.7	7.2	2.0	4.5	7.0	2.0	7.5	ns
Rise Time, Fall Time	t+,t–	C_n	F1	A0	1.3	5.3	1.5	3.0	5.0	1.5	5.3	ns
Propagation Delay	t++,t+–	A1	F1	—	2.6	10.4	3.0	6.5	10	3.0	10.8	ns
	t–+,t– –	A1	F1	—	2.6	10.4	3.0	6.5	10	3.0	10.8	ns
Rise Time, Fall Time	t+,t–	A1	F1	—	1.3	5.4	1.5	3.0	5.0	1.5	5.3	ns
Propagation Delay	t++,t– –	A1	P_G	S0,S3	1.6	7.0	2.0	5.0	6.5	2.0	7.0	ns
Rise Time, Fall Time	t+,t–	A1	P_G	S0,S3	0.8	3.7	1.1	2.0	3.5	1.1	3.8	ns
Propagation Delay	t++,t– –	A1	G_G	A0,A2,A3,C_n	1.1	7.4	2.0	4.5	7.0	1.3	7.7	ns
Rise Time, Fall Time	t+,t–	A1	G_G	A0,A2,A3,C_n	1.2	5.1	1.5	4.0	5.0	1.2	5.3	ns
Propagation Delay	t+–,t–+	A1	C_{n+4}	A0,A2,A3,C_n	1.7	7.3	2.0	5.0	7.0	2.0	7.8	ns
Rise Time, Fall Time	t+,t–	A1	C_{n+4}	A0,A2,A3,C_n	1.0	3.1	1.0	2.0	3.0	1.0	3.2	ns
Propagation Delay	t++,t–+	B1	F1	S3,C_n	2.7	11.3	3.0	8.0	11	3.0	11.9	ns
Rise Time, Fall Time	t+,t–	B1	F1	S3,C_n	1.2	5.3	1.5	3.5	5.0	1.5	5.3	ns
Propagation Delay	t++,t– –	B1	P_G	S0,A1	1.6	7.7	2.0	6.0	7.5	2.0	8.0	ns
Rise Time, Fall Time	t+,t–	B1	P_G	S0,A1	1.0	3.6	1.1	2.0	3.5	1.1	3.9	ns
Propagation Delay	t++,t– –	B1	G_G	S3,C_n	1.7	8.2	2.0	6.0	8.0	2.0	8.6	ns
Rise Time, Fall Time	t+,t–	B1	G_G	S3,C_n	1.4	5.2	1.5	3.0	5.0	1.2	5.4	ns
Propagation Delay	t+–,t–+	B1	C_{n+4}	S3,C_n	1.8	8.2	2.0	6.0	8.0	2.0	8.7	ns
Rise Time, Fall Time	t+,t–	B1	C_{n+4}	S3,C_n	0.9	3.1	1.0	2.0	3.0	1.0	3.2	ns
Propagation Delay	t++,t+–	M	F1	—	2.4	10.3	3.0	6.5	10	3.0	10.8	ns
Rise Time, Fall Time	t+,t–	M	F1	—	1.1	5.1	1.5	4.0	5.0	1.5	5.3	ns
Propagation Delay	t+–,t–+	S1	F1	A1,B1	2.5	10.7	3.0	6.5	10	3.0	10.8	ns
Rise Time, Fall Time	t+,t–	S1	F1	A1,B1	1.0	5.4	1.5	3.0	5.0	1.5	5.4	ns
Propagation Delay	t–+,t+–	S1	P_G	A3,B3	1.7	8.3	2.0	6.0	8.0	2.0	8.4	ns
Rise Time, Fall Time	t+,t–	S1	P_G	A3,B3	0.8	5.1	1.1	3.0	5.0	1.1	5.2	ns
Propagation Delay	t+–,t–+	S1	C_{n+4}	A3,B3	1.6	9.3	2.0	6.0	9.0	2.0	9.9	ns
Rise Time, Fall Time	t+,t–	S1	C_{n+4}	A3,B3	0.9	5.3	1.1	3.0	5.0	1.0	5.2	ns
Propagation Delay	t+–,t–+	S1	G_G	A3,B3	1.5	9.6	2.0	6.0	9.0	1.9	9.7	ns
Rise Time, Fall Time	t+,t–	S1	G_G	A3,B3	0.8	6.2	0.8	3.0	6.0	0.8	6.5	ns

† Logic high level (+1.11 Vdc) applied to pins listed. All other input pins are left floating or tied to +0.31 Vdc.
$V_{CC1} = V_{CC2} = +2.0$ Vdc, $V_{EE} = -3.2$ Vdc

* L Suffix Only

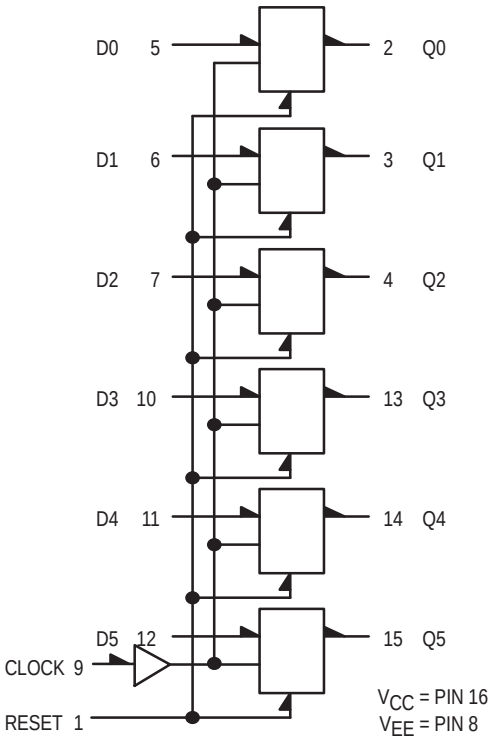
MC10186

Hex D Master-Slave Flip-Flop with Reset

The MC10186 contains six high–speed, master slave type “D” flip–flops. Clocking is common to all six flip–flops. Data is entered into the master when the clock is low. Master to slave data transfer takes place on the positive–going Clock transition. Thus, outputs may change only on a positive–going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master–slave construction of this device. **A COMMON RESET IS INCLUDED IN THIS CIRCUIT. RESET ONLY FUNCTIONS WHEN CLOCK IS LOW**.

- P_D = 460 mW typ/pkg (No Load)
- f_{toggle} = 150 MHz (typ)
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



CLOCKED TRUTH TABLE

R	C	D	Qn + 1
L	L	X	Q_n
L	H*	L	L
L	H*	H	H
H	L	X	L

*A clock H is a clock transition from a low to a high state.

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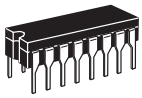
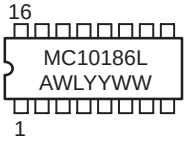
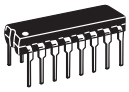
MARKING DIAGRAMS

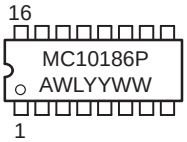


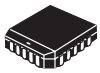
CDIP–16
L SUFFIX
CASE 620



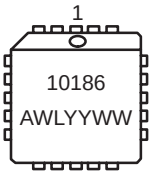


PDIP–16
P SUFFIX
CASE 648



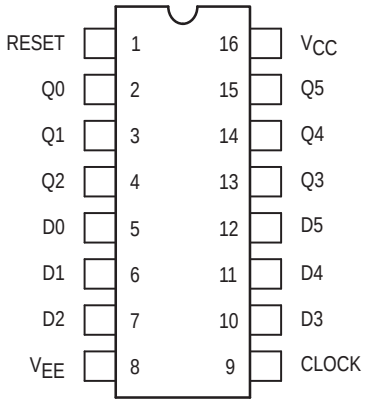


PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ORDERING INFORMATION

Device	Package	Shipping
MC10186L	CDIP–16	25 Units / Rail
MC10186P	PDIP–16	25 Units / Rail
MC10186FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		121		88	110		121	mAdc
Input Current	I_{inH}	5 9 1		350 495 920			220 310 575		220 310 575	µAdc
	I_{inL}	5	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	2† 15†	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2† 15†	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2† 15†	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2† 15†		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{1+3-} t_{1+4-} t_{9+2+} t_{9+2-}	3 4 2 2	1.6 1.6 1.6 1.6	4.6 4.6 4.6 4.6	1.6 1.6 1.6 1.6	2.5 2.5 3.5 3.5	4.5 4.5 4.5 4.5	1.6 1.6 1.6 1.6	5.0 5.0 5.0 5.0	
Rise Time (20 to 80%)	t_{2+}	2	1.0	4.1	1.1	1.8	4.0	1.1	4.4	
Fall Time (20 to 80%)	t_{2-}	2	1.0	4.1	1.1	1.8	4.0	1.1	4.4	
Setup Time	t_{setup}	2	2.5		2.5	2.5		2.5		ns
Hold Time	t_{hold}	2	1.5		1.5	–1.5		1.5		ns
Toggle Frequency (Max)	f_{tog}	2	125		125	150		125		MHz

† Output level to be measured after clock pulse. V_{IL} to V_{IH} appears at clock input (Pin 9).

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8					8	16
Input Current	I_{inH}	5 9 1	5 9 1				8 8 8	16 16 16
	I_{inL}	5		5			8	16
Output Voltage Logic 1	V_{OH}	2† 15†	5 12				8 8	16 16
Output Voltage Logic 0	V_{OL}	2† 15†		5 12			8 8	16 16
Threshold Voltage Logic 1	V_{OHA}	2† 15†			5 12		8 8	16 16
Threshold Voltage Logic 0	V_{OLA}	2† 15†				5 12	8 8	16 16
Switching Times (50Ω Load)			**+1.11Vdc**	**+0.31V**	**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	t_{1+3-} t_{1+4-} t_{9+2+} t_{9+2-}	3 4 2 2	6 7		1, 9 1, 9 5, 9 5, 9	3 4 2 2	8 8 8 8	16 16 16 16
Rise Time (20 to 80%)	t_{2+}	2			5, 9	2	8	16
Fall Time (20 to 80%)	t_{2-}	2			5, 9	2	8	16
Setup Time	t_{setup}	2			5, 9	2	8	16
Hold Time	t_{hold}	2			5, 9	2	8	16
Toggle Frequency (Max)	f_{tog}	2					8	16

† Output level to be measured after clock pulse. V_{IL} ⟋ V_{IH} appears at clock input (Pin 9).

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

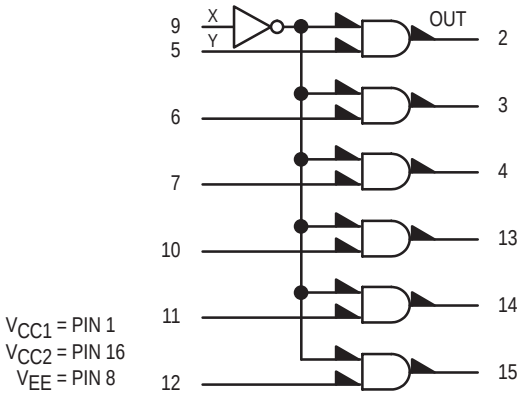
MC10188

Hex Buffer With Enable

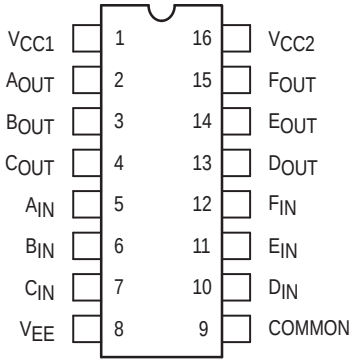
The MC10188 is a high–speed hex buffer with a common Enable input. When Enable is in the high state, all outputs are in the low state. When Enable is in the low state, the outputs take the same state as the inputs.

- Power Dissipation = 180 mW typ/pkg (No Load)
- Propagation Delay = 2.0 ns typ (B – Q)
  2.5 ns typ (A – Q)

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

TRUTH TABLE

Inputs		Output
X	Y	OUT
L	L	L
L	H	H
H	L	L
H	H	L

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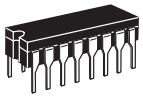
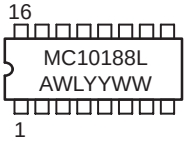
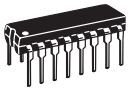
MARKING DIAGRAMS

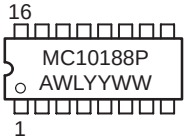


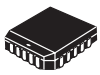
CDIP–16
L SUFFIX
CASE 620



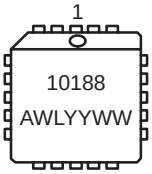


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10188L	CDIP–16	25 Units / Rail
MC10188P	PDIP–16	25 Units / Rail
MC10188FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Pin Under Test	Test Limits						Unit
				–30°C		+25°C		+85°C		
				Min	Max	Min	Max	Min	Max	
Power Supply Drain Current		I_E	8		46		42		46	mAdc
Input Current		I_{inH}	5		425		265		265	μAdc
		I_{inH}	9		460		290		290	μAdc
Output Voltage	Logic 1	V_{OH}	2	–1.060	–0.890	–0.960	–0.810	–0.890	–0.700	Vdc
Output Voltage	Logic 0	V_{OL}	2	–1.890	–1.675	–1.850	–1.650	–1.825	–1.615	Vdc
Threshold Voltage	Logic 1	V_{OHA}	2	–1.080		–0.980		–0.910		Vdc
Threshold Voltage	Logic 0	V_{OLA}	2		–1.655		–1.630		–1.595	Vdc
Switching Times	(50Ω Load)									ns
Propagation Delay	Enable	t_{PHL}	2	1.1	3.9	1.1	3.5	1.1	3.9	
	Data	t_{PLH}	2	1.0	3.3	1.0	2.9	1.0	3.3	
Rise/Fall Time	(20 to 80%)	t_{TLH} t_{THL}	2	1.1	3.7	1.1	3.3	1.1	3.7	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts)					
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	5	5				8	1, 16
		I_{inH}	9	9				8	1, 16
Output Voltage	Logic 1	V_{OH}	2	5				8	1, 16
Output Voltage	Logic 0	V_{OL}	2		9			8	1, 16
Threshold Voltage	Logic 1	V_{OHA}	2			5		8	1, 16
Threshold Voltage	Logic 0	V_{OLA}	2				5	8	1, 16
Switching Times	(50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	Enable	t_{PHL}	2			9	2	8	1, 16
	Data	t_{PLH}	2			5	2	8	1, 16
Rise/Fall Time	(20 to 80%)	t_{TLH} t_{THL}	2			5	2	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

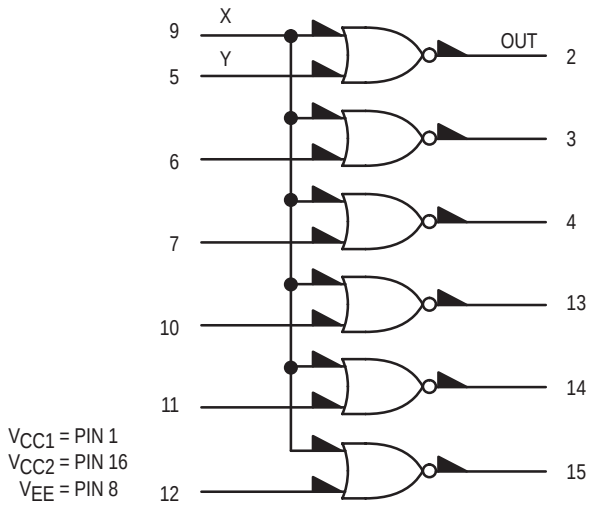
MC10189

Hex Inverter With Enable

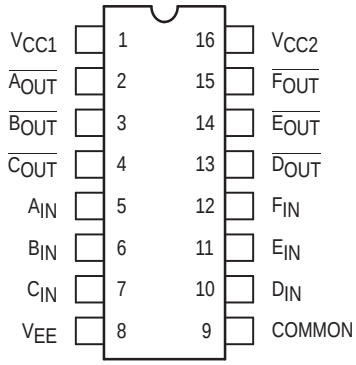
The MC10189 provides a high-speed Hex Inverter with a common Enable input. The hex inverting function is provided when Enable is in the low state. When Enable is in the high state all outputs are low.

- P_D = 200 mW typ/pkg (No Load)
- t_{pd} = 2.0 ns (Y–Q)
  = 2.5 ns (X–Q)

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

TRUTH TABLE

Inputs		Output
X	Y	OUT
L	L	H
L	H	L
H	L	L
H	H	L

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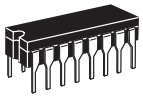
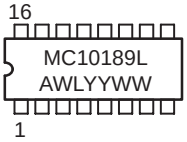
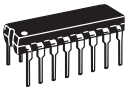
MARKING DIAGRAMS

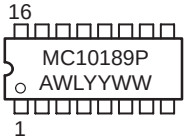


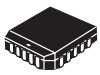
CDIP–16
L SUFFIX
CASE 620



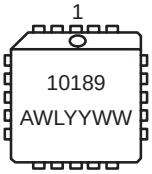


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10189L	CDIP–16	25 Units / Rail
MC10189P	PDIP–16	25 Units / Rail
MC10189FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Pin Under Test	Test Limits						Unit
				–30°C		+25°C		+85°C		
				Min	Max	Min	Max	Min	Max	
Power Supply Drain Current		I_E	8		44		40		44	mAdc
Input Current		I_{inH}	5		425		265		265	μAdc
		I_{inL}	9		890		555		555	μAdc
Output Voltage	Logic 1	V_{OH}	2	–1.060	–0.890	–0.960	–0.810	–0.890	–0.700	Vdc
Output Voltage	Logic 0	V_{OL}	2	–1.890	–1.675	–1.850	–1.650	–1.825	–1.615	Vdc
Threshold Voltage	Logic 1	V_{OHA}	2	–1.080		–0.980		–0.910		Vdc
Threshold Voltage	Logic 0	V_{OLA}	2		–1.655		–1.630		–1.595	Vdc
Switching Times	(50Ω Load)									ns
Propagation Delay	Enable	t_{PHL}	2	1.1	3.9	1.1	3.5	1.1	3.9	
	Data	t_{PLH}	2	1.0	3.3	1.0	2.9	1.0	3.3	
Rise/Fall Time	(20 to 80%)	t_{TLH} t_{THL}	2	1.1	3.7	1.1	3.3	1.1	3.7	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts)					
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	5	5				8	1, 16
		I_{inL}	9	9				8	1, 16
Output Voltage	Logic 1	V_{OH}	2		5			8	1, 16
Output Voltage	Logic 0	V_{OL}	2	9				8	1, 16
Threshold Voltage	Logic 1	V_{OHA}	2				5	8	1, 16
Threshold Voltage	Logic 0	V_{OLA}	2			5		8	1, 16
Switching Times	(50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	Enable	t_{PHL}	2			9	2	8	1, 16
	Data	t_{PLH}	2			5	2	8	1, 16
Rise/Fall Time	(20 to 80%)	t_{TLH} t_{THL}	2			5	2	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

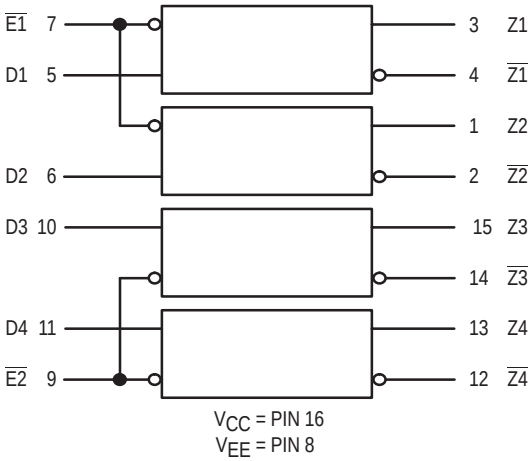
MC10192

Quad Bus Driver

The MC10192 contains four line drivers with complementary outputs. Each driver has a Data (D) input and shares an Enable ($\overline{E}$) input with another driver. The two driver outputs are the uncommitted collectors of a pair of NPN transistors operating as a current switch. Each driver accepts 10K MECL input signals and provides a nominal signal swing of 800 mV across a 50 Ω load at each output collector. Outputs can drive higher values of load resistance, provided that the combination of I_R drop and load return voltage V_{LR} does not cause an output collector to go more negative than –2.4 V with respect to V_{CC}. To avoid output transistor breakdown, the load return voltage should not be more positive than +5.5 V with respect to V_{CC}. When the $\overline{E}$ input is high, both output transistors of a driver are nonconducting. When not used, the $\overline{E}$ inputs, as well as the D inputs, may be left open.

- Open Collector Outputs Drive Terminated Lines or Transformers
- 50 kW Input Pulldown Resistors on All Inputs (Unused Inputs May Be Left Open)
- Power Dissipation = 575 mW typ/pkg (No Load)
- Propagation Delay = 3.5 ns typ ($\overline{E}$ — Output)
  3.0 ns typ (D — Output)

LOGIC DIAGRAM



V_{CC} = PIN 16
V_{EE} = PIN 8

TRUTH TABLE

Inputs		Output	
$\overline{E}$	D	Z	$\overline{Z}$
H	X	H	H
L	H	H	L
L	L	L	H

Note: Unused outputs must be terminated to V_{CC} for proper operation.

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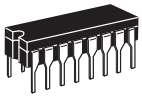
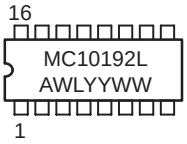
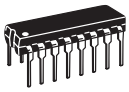
MARKING DIAGRAMS

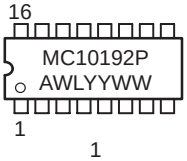


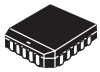
CDIP–16
L SUFFIX
CASE 620



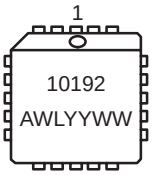


PDIP–16
P SUFFIX
CASE 648



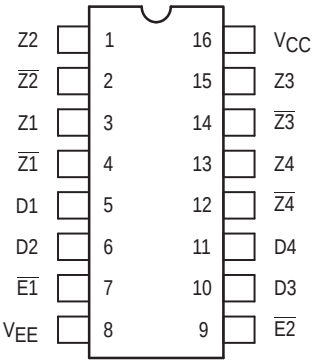


PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ORDERING INFORMATION

Device	Package	Shipping
MC10192L	CDIP–16	25 Units / Rail
MC10192P	PDIP–16	25 Units / Rail
MC10192FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Pin Under Test	Test Limits						Unit
				–30°C		+25°C		+85°C		
				Min	Max	Min	Max	Min	Max	
Power Supply Drain Current		I_E	8		154		140		154	mAdc
Input Current		I_{inH}	5		350		220		220	μAdc
		I_{inL}	5	0.5		0.5		0.3		μAdc
Output Current High	Logic 1	I_{OH}	2				2.0			mAdc
Output Current Low	Logic 0	I_{OL}	2	13.5	18.0	14.0	18.0	14.0	19.0	mAdc
Threshold Current High	Logic 1	I_{OHC}	2		2.0		2.0		2.0	mAdc
Threshold Current Low	Logic 0	I_{OLC}	2	13.5		14.0		14.0		mAdc
Output Sink Current Low	Logic 0	I_{OS}	2	13.3		13.9		13.3		mAdc
Load Return Voltage Absolute Max Rating (Note 1.)		V_{LR}			5.5		5.5		5.5	V
Output Voltage Low (Note 2.)		V_{OLS}				–2.4				V
Switching Times	(50Ω Load)									ns
Propagation Delay	$\overline{E}$ to Output	t_{PHL}				2.0	6.0			
	D to Output	t_{PLH}				1.5	4.5			
Rise/Fall Time	(20 to 80%)	t_{TLH}					3.3			
		t_{THL}								

1. The 5.5V value is a maximum rating, do not exceed. A 270Ω resistor will prevent output transistor breakdown.
2. Limitations of load resistor and load return voltage combinations. Refer to page 405 description.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
	TEST VOLTAGE VALUES (Volts)				
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	16
Input Current		I_{inH}	5	5				8	16
		I_{inL}	5		5			8	16
Output Current High	Logic 1	I_{OH}	2		5,6,10,11			8	16
Output Current Low	Logic 0	I_{OL}	2	5,6,10,11				8	16
Threshold Current High	Logic 1	I_{OHC}	2		5,7,9,10,11		6	8	16
Threshold Current Low	Logic 0	I_{OLC}		5,10,11	7,9	6		8	16
Output Sink Current Low	Logic 0	I_{OS}	2	5,6,10,11				8	16
Load Return Voltage Absolute Max Rating (Note 1.)		V_{LR}						8	16
Output Voltage Low (Note 2.)		V_{OLS}						8	16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

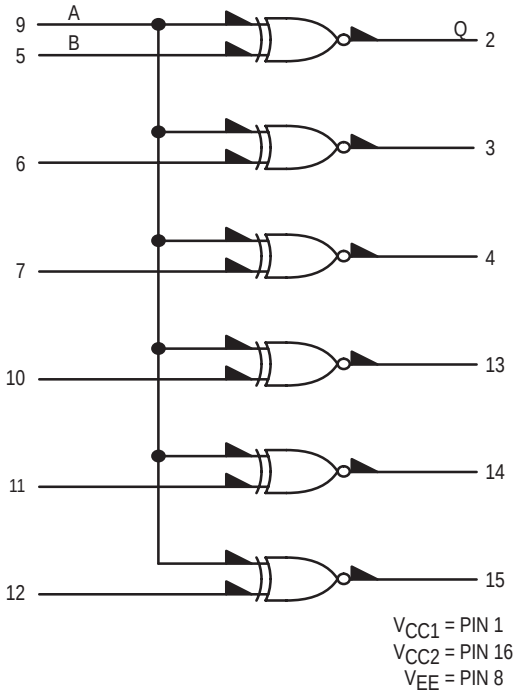
MC10195

Hex Inverter/Buffer

The MC10195 is a Hex Buffer Inverter which is built using six EXCLUSIVE NOR gates. There is a common input to these gates which when placed low or left open allows them to act as inverters. With the common input connected to a high logic level the MC10195 is a hex buffer, useful for high fanout clock driving and reducing stub lengths on long bus lines.

- P_D = 200 mW typ/pkg (No Load)
- t_{pd} = 2.8 ns typ (B–Q)
- t_{pd} = 3.8 ns typ (A–Q)
- t_r, t_f = 2.5 ns typ (20%–80%)

LOGIC DIAGRAM



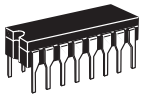
TRUTH TABLE

Inputs		Output
A	**B**	**Q**
L	L	H
L	H	L
H	L	L
H	H	H

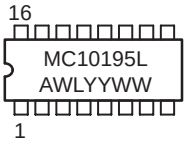
ON Semiconductor

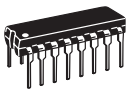
http://onsemi.com

MARKING DIAGRAMS

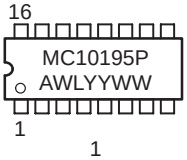


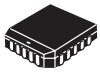
CDIP–16
L SUFFIX
CASE 620



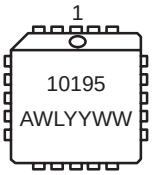


PDIP–16
P SUFFIX
CASE 648



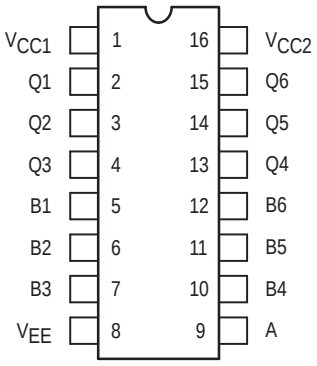


PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ORDERING INFORMATION

Device	Package	Shipping
MC10195L	CDIP–16	25 Units / Rail
MC10195P	PDIP–16	25 Units / Rail
MC10195FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Pin Under Test	Test Limits							Unit
				–30°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current		I_E	8		54		39	49		54	mAdc
Input Current		I_{inH}	5 9		425 460			265 290		265 290	μAdc
		I_{inL}	5	0.5		0.5			0.3		μAdc
Output Voltage	Logic 1	V_{OH}	2	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	Vdc
Output Voltage	Logic 0	V_{OL}	2	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	Vdc
Threshold Voltage	Logic 1	V_{OHA}	2	–1.080		–0.980			–0.910		Vdc
Threshold Voltage	Logic 0	V_{OLA}	2		–1.655			–1.630		–1.595	Vdc
Switching Times (50Ω Load)											ns
Propagation Delay		t_{5+2-}	2	1.1	4.2	1.1	2.8	4.0	1.1	4.4	
		t_{7-4+}	4	1.1	4.2	1.1	2.8	4.0	1.1	4.4	
		t_{10+13+}	13	1.1	4.2	1.1	2.8	4.0	1.1	4.4	
		t_{11-14-}	14	1.1	4.2	1.1	2.8	4.0	1.1	4.4	
		t_{9-14-}	14	1.1	5.2	1.1	3.8	5.0	1.1	5.4	
Rise Time	(20 to 80%)	t_{2+}	2	1.1	4.7	1.1	2.5	4.5	1.1	5.0	
Fall Time	(20 to 80%)	t_{2-}	2	1.1	4.7	1.1	2.5	4.5	1.1	5.0	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
	TEST VOLTAGE VALUES (Volts)				
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	5 9	5 9				8 8	1, 16 1, 16
		I_{inL}	5		5			8	1, 16
Output Voltage	Logic 1	V_{OH}	2					8	1, 16
Output Voltage	Logic 0	V_{OL}	2	9				8	1, 16
Threshold Voltage	Logic 1	V_{OHA}	2				5	8	1, 16
Threshold Voltage	Logic 0	V_{OLA}	2			5		8	1, 16
Switching Times	(50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay		t_{5+2-}	2			5	2	8	1, 16
		t_{7-4+}	4			7	4	8	1, 16
		t_{10+13+}	13			10	13	8	1, 16
		t_{11-14-}	14			11	14	8	1, 16
		t_{9-14-}	14			9	14	8	1, 16
Rise Time	(20 to 80%)	t_{2+}	2			5	2	8	1, 16
Fall Time	(20 to 80%)	t_{2-}	2			5	2	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

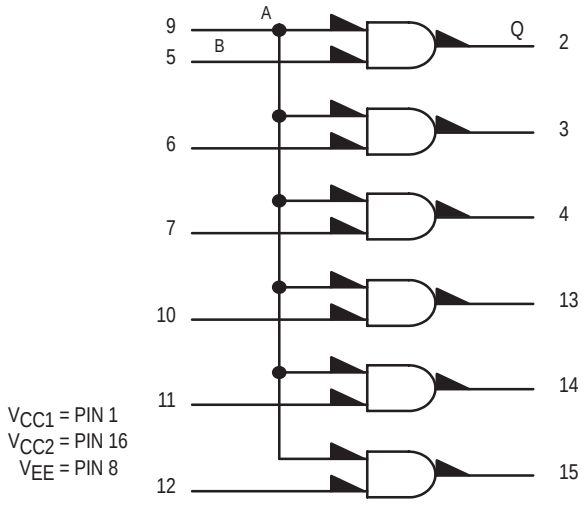
MC10197

Hex AND Gate

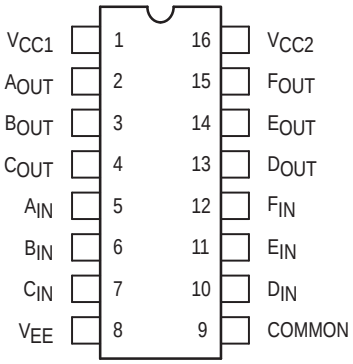
The MC10197 provides a high speed hex AND function with strobe capability.

- P_D = 200 mW typ/pkg (No Load)
- t_{pd} = 2.8 ns typ (B–Q)
- t_{pd} = 3.8 ns typ (A–Q)
- t_r, t_f = 2.5 ns typ (20%–80%)

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

TRUTH TABLE

Inputs		Output
A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

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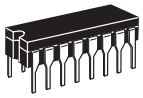
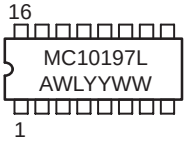
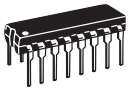
MARKING DIAGRAMS

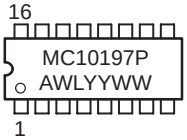


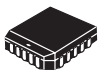
CDIP–16
L SUFFIX
CASE 620



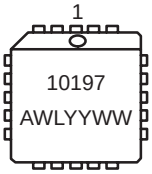


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10197L	CDIP–16	25 Units / Rail
MC10197P	PDIP–16	25 Units / Rail
MC10197FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		54		39	49		54	mAdc
Input Current	I_{inH}	5 9		425 460			265 290		265 290	µAdc
	I_{inL}	5	0.5		0.5		0.3			µAdc
Output Voltage Logic 1	V_{OH}	2	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	Vdc
Output Voltage Logic 0	V_{OL}	2	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2	–1.080		–0.980			–0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2		–1.655			–1.630		–1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{5+2+} t_{9+2+}	2 2	1.1 1.1	4.2 5.3	1.1 1.1	2.8 3.5	4.0 5.0	1.1 1.1	4.4 5.5	
Rise Time (20 to 80%)	t_{2+}	2	1.1	4.7	1.1	2.5	4.5	1.1	5.0	
Fall Time (20 to 80%)	$t_{2–}$	2	1.1	4.7	1.1	2.5	4.5	1.1	5.0	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts)					(V_{CC}) Gnd
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8					8	1, 16
Input Current	I_{inH}	5 9	5 9				8 8	1, 16 1, 16
	I_{inL}	5		5			8	1, 16
Output Voltage Logic 1	V_{OH}	2	5, 9				8	1, 16
Output Voltage Logic 0	V_{OL}	2					8	1, 16
Threshold Voltage Logic 1	V_{OHA}	2	9		5		8	1, 16
Threshold Voltage Logic 0	V_{OLA}	2	9			5	8	1, 16
Switching Times (50Ω Load)				**+1.11V**	**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	t_{5+2+} t_{9+2+}	2 2		9 5	5 9	2 2	8 8	1, 16 1, 16
Rise Time (20 to 80%)	t_{2+}	2		9	5	2	8	1, 16
Fall Time (20 to 80%)	$t_{2–}$	2		9	5	2	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10198

Monostable Multivibrator

The MC10198 is a retriggerable monostable multivibrator. Two enable inputs permit triggering on any combination of positive or negative edges as shown in the accompanying table. The trigger input is buffered by Schmitt triggers making it insensitive to input rise and fall times.

The pulse width is controlled by an external capacitor and resistor. The resistor sets a current which is the linear discharge rate of the capacitor. Also, the pulse width can be controlled by an external current source or voltage (see applications information).

For high–speed response with minimum delay, a hi–speed input is also provided. This input bypasses the internal Schmitt triggers and the output responds within 2 nanoseconds typically.

Output logic and threshold levels are standard MECL 10,000. Test conditions are per Table 2. Each “Precondition” referred to in Table 2 is per the sequence of Table 1.

- P_D = 415 mW typ/pkg (No Load)
- t_{pd} = 4.0 ns typ Trigger Input to Q
- 2.0 ns typ Hi–Speed Input to Q
- Min Timing Pulse Width PW_{Qmin} 10 ns typ[1]
- Max Timing Pulse Width PW_{Qmax} >10 ms typ[2]
- Min Trigger Pulse Width PW_T 2.0 ns typ
- Min Hi–Speed Trigger Pulse Width PW_{HS} 3.0 ns typ
- Enable Setup Time t_{set} 1.0 ns typ
- Enable Hold Time t_{hold} 1.0 ns typ
- [1] C_{Ext} = 0 (Pin 4 open), R_{Ext} = 0 (Pin 6 to V_{EE})
- [2] C_{Ext} = 10 mF, R_{Ext} = 2.7 kW

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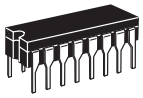
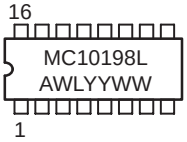
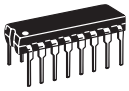
MARKING DIAGRAMS

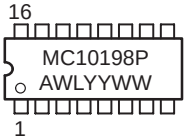


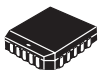
CDIP–16
L SUFFIX
CASE 620



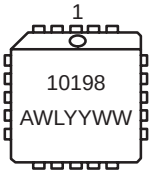


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

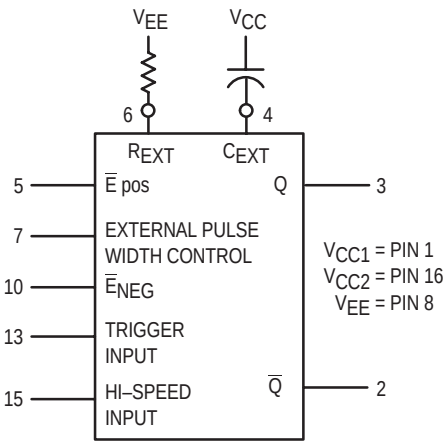


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

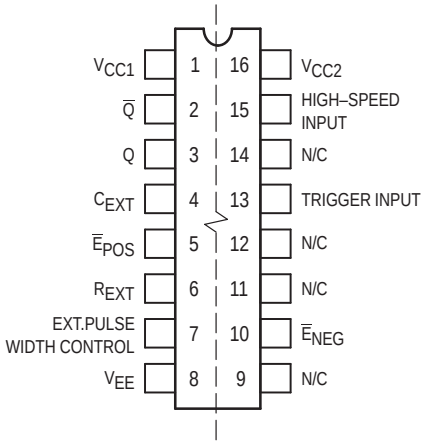
ORDERING INFORMATION

Device	Package	Shipping
MC10198L	CDIP–16	25 Units / Rail
MC10198P	PDIP–16	25 Units / Rail
MC10198FN	PLCC–20	46 Units / Rail

LOGIC DIAGRAM



DIP PIN ASSIGNMENT

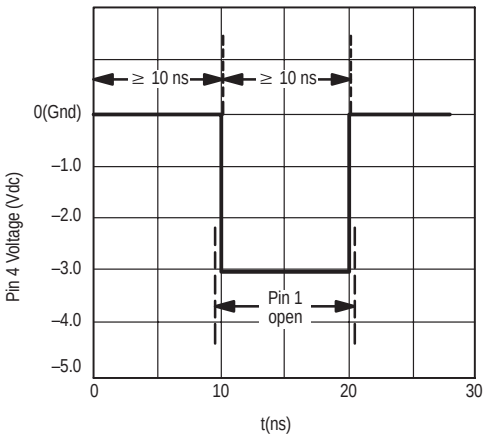


Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

TRUTH TABLE

INPUT		OUTPUT
$\overline{E}_{Pos}$	$\overline{E}_{Neg}$	
L	L	Triggers on both positive & negative input slopes
L	H	Triggers on positive input slope
H	L	Triggers on negative input slope
H	H	Trigger is disabled

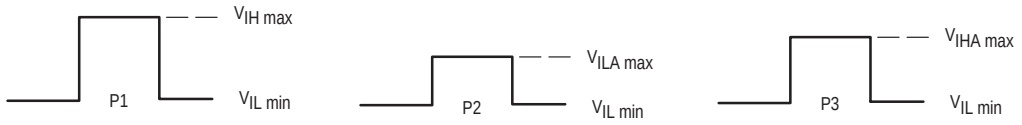
TABLE 1 — PRECONDITION SEQUENCE



1. At t = 0 a.) Apply V_{IHmax} to Pin 5 and 10.
   b.) Apply V_{ILmin} to Pin 15.
   c.) Ground Pin 4.
2. At t ≥ 10 ns a.) Open Pin 1.
   b.) Apply –3.0 Vdc to Pin 4.
   Hold these conditions for ≥10 ns.
3. Return Pin 4 to Ground and perform test as indicated in Table 2.

TABLE 2 — CONDITIONS FOR TESTING OUTPUT LEVELS

(See Table 1 for Precondition Sequence)



Pins 1, 16 = V_{CC} = Ground
Pins 6, 8 = V_{EE} = –5.2 Vdc
Outputs loaded 50 Ω to –2.0 Vdc

Test	P.U.T.	Pin Conditions 5	10	13	15
Precondition					
V_{OH}	2			V_{IL} min	
V_{OH}	3			P1	
Precondition					
V_{OL}	3			V_{IL} min	
V_{OL}	2			P1	
Precondition					
V_{OHA}	2				V_{ILA} max
V_{OHA}	3				V_{IHA} min
Precondition					
V_{OHA}	2			V_{IL} min	
V_{OHA}	3			P3	
Precondition					
V_{OHA}	2			P2	
V_{OHA}	3			P3	
Precondition					
V_{OHA}	2		V_{IH} max	P2	
V_{OHA}	3		V_{IH} max	P3	
Precondition					
V_{OHA}	2		V_{IH} max	P1	
V_{OHA}	3		V_{IH} max	P1	

Test	P.U.T.	Pin Conditions 5	10	13	15
Precondition					
V_{OHA}	2		V_{IHA} min	P1	
V_{OHA}	3		V_{ILA} max	P1	
Precondition					
V_{OLA}	3				V_{ILA} max
V_{OLA}	2				V_{IHA} min
Precondition					
V_{OLA}	2			V_{IL} min	
V_{OLA}	3			V_{IL} min	
Precondition					
V_{OLA}	3			P2	
V_{OLA}	2			P3	
Precondition					
V_{OLA}	3		V_{IH} max	P2	
V_{OLA}	2		V_{IH} max	P3	
Precondition					
V_{OLA}	3	V_{IHA} min	V_{IH} max	P1	
V_{OLA}	2	V_{ILA} max	V_{IH} max	P1	
Precondition					
V_{OLA}	3	V_{IH} max	V_{IHA} min	P1	
V_{OLA}	2	V_{IH} max	V_{ILA} max	P1	

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		110		80	100		110	mAdc
Input Current	I_{inH}	5, 10 13 15		415 350 560			260 220 350		260 220 350	μAdc
	I_{inL}	5	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	2 3	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										
Trigger Input	t_{T+Q+} $t_{T–Q+}$	3 3	2.5 2.5	6.5 6.5	2.5 2.5	4.0 4.0	5.5 5.5	2.5 2.5	6.5 6.5	ns
High Speed Trigger Input	t_{HS+Q+}	3	1.5	3.2	1.5	2.0	2.8	1.5	3.2	ns
Minimum Timing Pulse Width	PW_{Qmin}	3				10.0				ns
Maximum Timing Pulse Width	PW_{Qmax}	3				>10				ms
Min Trigger Pulse Width	PW_T	3				2.0				ns
Min Hi–Spd Trig Pulse Width	PW_{HS}	3				3.0				ns
Rise Time (20 to 80%)		3	1.5	4.0	1.5		3.5	1.5	4.0	ns
Fall Time (20 to 80%)		3	1.5	4.0	1.5		3.5	1.5	4.0	ns
Enable Setup Time	t_{setup} (E)	3				1.0				ns
Enable Hold Time	t_{hold} (E)	3				1.0				ns

1. The monostable is in the timing mode at the time of this test.
2. C_{EXT} = 0 (Pin 4 Open); R_{EXT} = 0 (Pin 6 tied to V_{EE}).
3. C_{EXT} = 10μF (Pin); R_{EXT} = 2.7k (Pin 6).
4. 

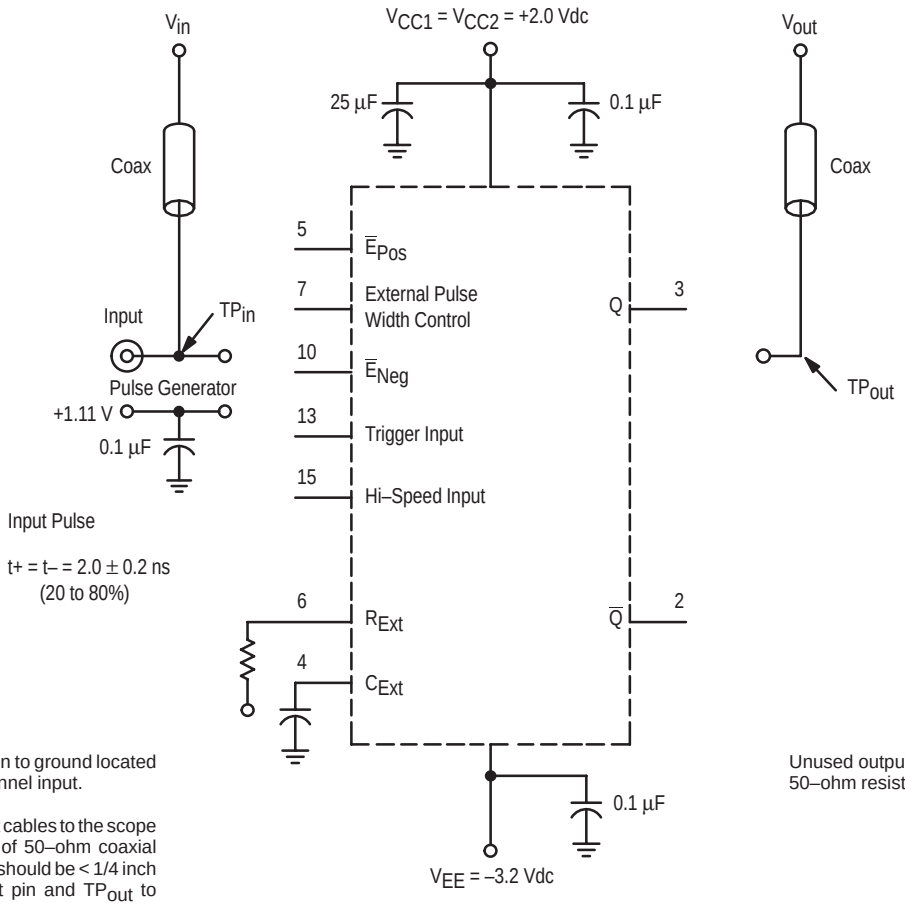
ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C			–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C			–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C			–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					**(V_{CC}) Gnd**
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					6, 8	1, 4, 16
Input Current		I_{inH}	5, 10 13 15	5,10 13 15				6, 8 6, 8 6, 8	1, 4, 16 1, 4, 16 1, 4, 16
		I_{inL}	5		5			6, 8	1, 4, 16
Output Voltage	Logic 1	V_{OH}	2 3	 13 (4.)	13			6, 8 6, 8	1, 4, 16 1, 4, 16
Output Voltage	Logic 0	V_{OL}	2 3	13 (4.)	 13			6, 8 6, 8	1, 4, 16 1, 4, 16
Threshold Voltage	Logic 1	V_{OHA}	2 3			 15	15	6, 8 6, 8	1, 16, 4 1, 16, 4
Threshold Voltage	Logic 0	V_{OLA}	2 3			15	 15	6, 8 6, 8	1, 16, 4 1, 16, 4
Switching Times	(50Ω Load)			**+1.11V**		**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Trigger Input		t_{T+Q+} $t_{T–Q+}$	3 3	10 5		13 13	3 3	6, 8 6, 8	1, 16, 4 1, 16, 4
High Speed Trigger Input		t_{HS+Q+}	3			15	3	6, 8	1, 16, 4
Minimum Timing Pulse Width		PW_{Qmin}	3				Note 2.	6, 8	1, 16, 4
Maximum Timing Pulse Width		PW_{Qmax}	3				Note 3.	6, 8	1, 16, 4
Minimum Trigger Pulse Width		PW_T	3			13	3	6, 8	1, 16, 4
Minimum Hi–Spd Trigger Pulse Width		PW_{HS}	3			15	3	6, 8	1, 16, 4
Rise Time	(20 to 80%)		3					6, 8	1, 16, 4
Fall Time	(20 to 80%)		3					6, 8	1, 16, 4
Enable Setup Time		t_{setup} (E)	3			5	3	6, 8	1, 16, 4
Enable Hold Time		t_{hold} (E)	3			5	3	6, 8	1, 16, 4

1. The monostable is in the timing mode at the time of this test.
2. C_{EXT} = 0 (Pin 4 Open); R_{EXT} = 0 (Pin 6 tied to V_{EE}).
3. C_{EXT} = 10μF (Pin); R_{EXT} = 2.7k (Pin 6).
4. 

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

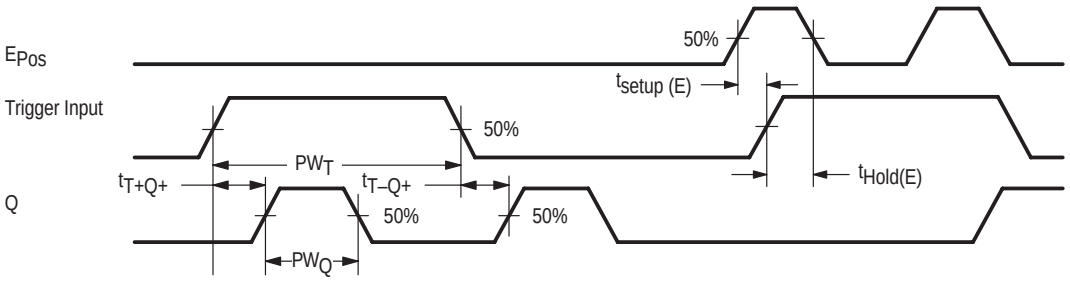
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

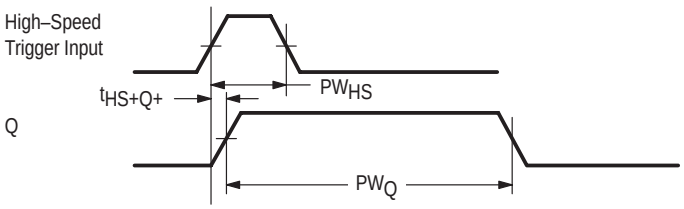


50–ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50–ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs are tied to a 50–ohm resistor to ground.





APPLICATIONS INFORMATION

Circuit Operation:

3. PULSE WIDTH TIMING — The pulse width is determined by the external resistor and capacitor. The MC10198 also has an internal resistor (nominally 284 ohms) that can be used in series with R_{Ext}. Pin 7, the external pulse width control, is a constant voltage node (–3.60 V nominally). A resistance connected in series from this node to V_{EE} sets a constant timing current I_T. This current determines the discharge rate of the capacitor:

where

ΔT = pulse width
ΔV = 1.9 V change in capacitor voltage

Then: $I_T = C_{Ext} \frac{\Delta V}{\Delta T}$

If $R_{Ext} + R_{Int}$ are in series to V_{EE}:

$I_T = [(–3.60\ V) – (–5.2\ V)] \div [R_{Ext} + 284\ \Omega]$
$I_T = 1.6\ V/(R_{Ext} + 284)$

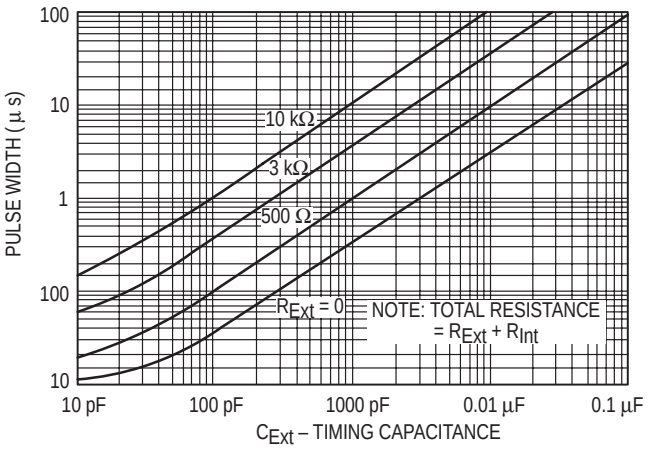
The timing equation becomes: $\Delta T = C_{Ext} \frac{1.9\ V}{I_T}$

$\Delta T = [(C_{Ext})(1.9\ V)] \div [1.6\ V/(R_{Ext} + 284)]$
$\Delta T = C_{Ext}\ (R_{Ext} + 284)\ 1.19$

where ΔT = Sec
R_{Ext} = Ohms
C_{Ext} = Farads

Figure 2 shows typical curves for pulse width versus C_{Ext} and R_{Ext} (total resistance includes R_{Int}). Any low leakage capacitor can be used and R_{Ext} can vary from 0 to 16 k–ohms.

FIGURE 2 – TIMING PULSE WIDTH versus C_{Ext} and R_{Ext}



4. TRIGGERING —The $\overline{E}_{pos}$ and $\overline{E}_{Neg}$ inputs control the trigger input. The MC10198 can be programmed to trigger on the positive edge, negative edge, or both. Also, the trigger input can be totally disabled. The truth table is shown on the first page of the data sheet.

The device is totally retriggerable. However, as duty cycle approaches 100%, pulse width jitter can occur due to the recovery time of the circuit. Recovery time is basically dependent on capacitance C_{Ext}. Figure 3 shows typical recovery time versus capacitance at I_T = 5 mA.

FIGURE 1 —

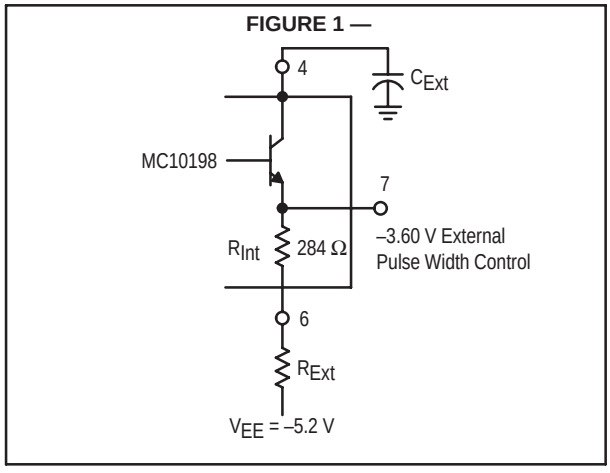
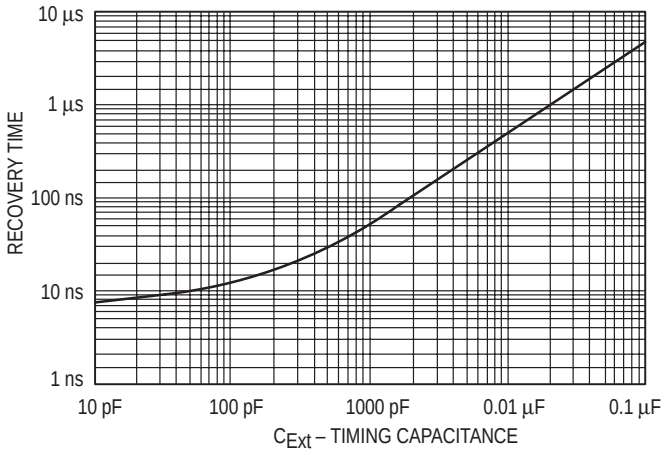


FIGURE 3 — RECOVERY TIME versus C_{Ext} @ I_T = 5 mA



5. HI–SPEED INPUT — This input is used for stretching very narrow pulses with minimum delay between the output pulse and the trigger pulse. The trigger input should be disabled when using the high–speed input. The MC10198 triggers on the rising edge, using this input, and input pulse width should narrow, typically less than 10 nanoseconds.

USAGE RULES:

1. Capacitor lead lengths should be kept very short to minimize ringing due to fast recovery rise times.
2. The $\overline{E}$ inputs should not be tied to ground to establish a high logic level. A resistor divider or diode can be used to establish a –0.7 to –0.9 voltage level.
3. For optimum temperature stability; 0.5 mA is the best timing current I_T. The device is designed to have a constant voltage at the EXTERNAL PULSE WIDTH CONTROL over temperature at this current value.
4. Pulse Width modulation can be attained with the EXTERNAL PULSE WIDTH CONTROL. The timing current can be altered to vary the pulse width. Two schemes are:
   a. The internal resistor is not used. A dependent current source is used to set the timing current as shown in Figure 4. A graph of pulse width versus timing current (C_{Ext} = 13 pF) is shown in Figure 5.
   b. A control voltage can also be used to vary the pulse width using an additional resistor (Figure 6). The current ($I_T + I_C$) is set by the voltage drop across $R_{Int} + R_{Ext}$. The control current IC modifies I_T and alters the pulse width. Current I_C should never force I_T to zero. R_C typically 1 kΩ.

FIGURE 4 —

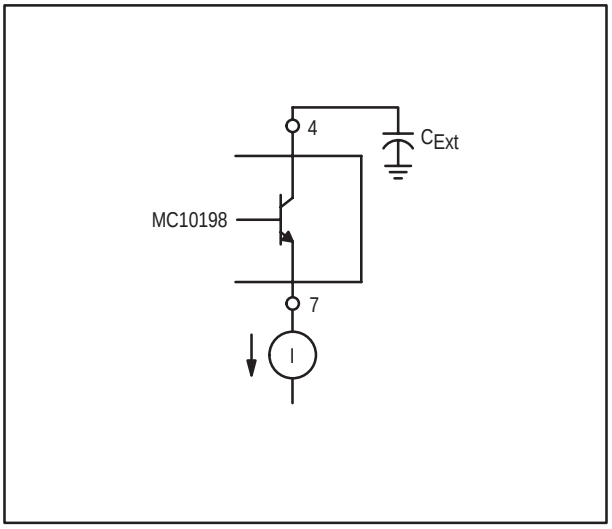


FIGURE 5 — PULSE WIDTH versus I_T @ C_{Ext} = 13 pF

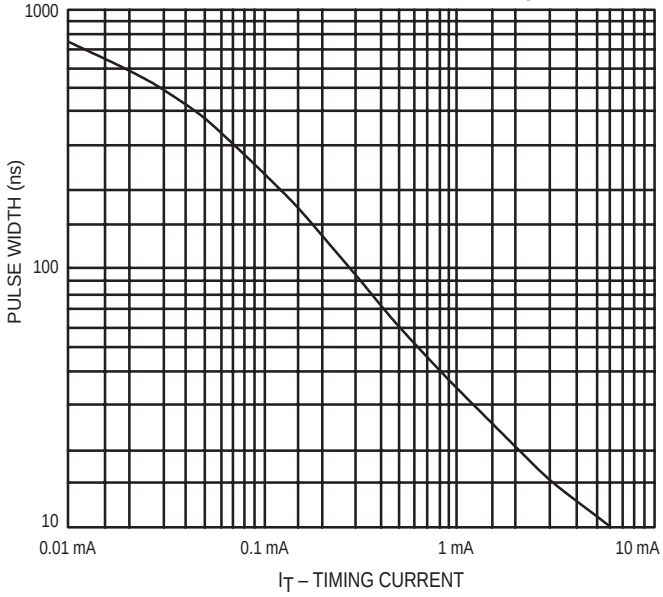
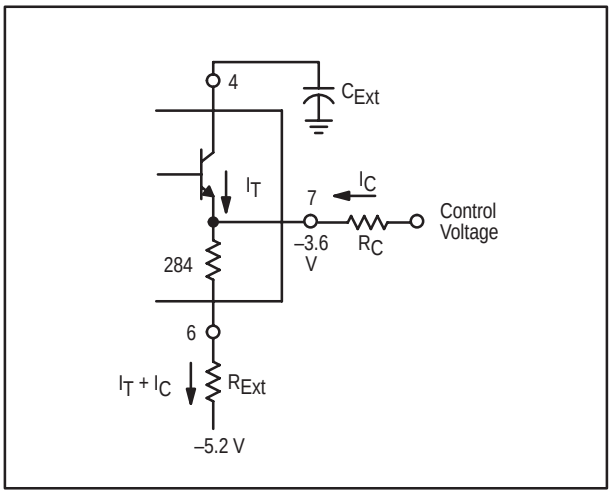
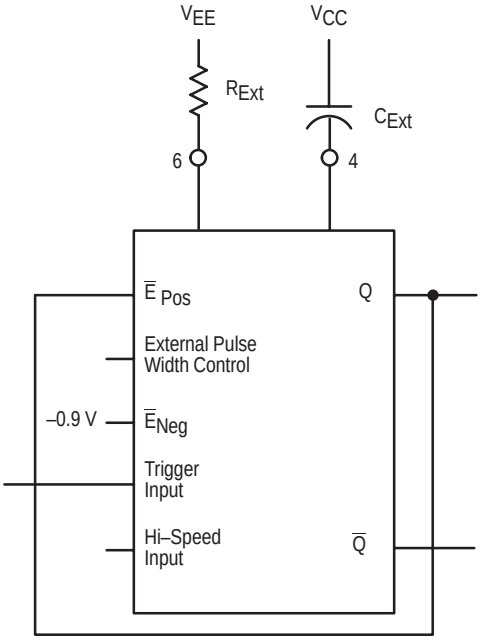


FIGURE 6 —



5. The MC10198 can be made non–retriggerable. The Q output is fed back to disable the trigger input during the triggered state (Logic Diagram). Figure 7 shows a positive triggered configuration; a similar configuration can be made for negative triggering.

FIGURE 7 —



MC10210

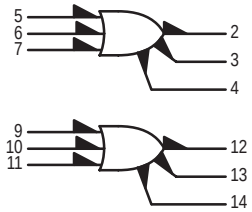
Dual 3-Input/3-Output OR Gate

The MC10210 is designed to drive up to six transmission lines simul– taneously. The multiple outputs of this device also allow the wire "OR"–ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10210 particularly useful in clock distribution applications where minimum clock skew is desired.

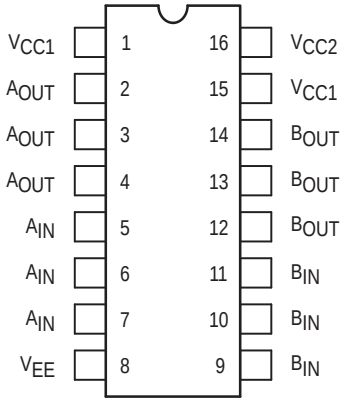
- P_D = 160 mW typ/pkg (No Loads)
- t_{pd} = 1.5 ns typ (All Output Loaded)
- t_r, t_f = 1.5 ns typ (20%–80%)

LOGIC DIAGRAM



V_{CC1} = PIN 1, 15
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP
PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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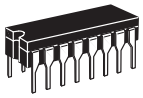
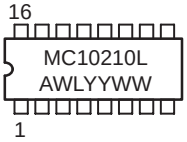
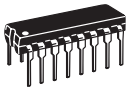
MARKING DIAGRAMS

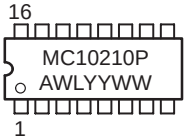


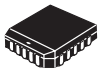
CDIP–16
L SUFFIX
CASE 620



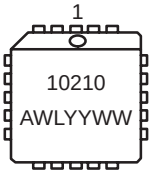


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10210L	CDIP–16	25 Units / Rail
MC10210P	PDIP–16	25 Units / Rail
MC10210FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		42			38		42	mAdc
Input Current	I_{inH}	5, 6, 7		650			410		410	μAdc
	I_{inL}	5, 6, 7	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	2 3 4	–1.060 –1.060 –1.060	–0.890 –0.890 –0.890	–0.960 –0.960 –0.960		–0.810 –0.810 –0.810	–0.890 –0.890 –0.890	–0.700 –0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3 4	–1.890 –1.890 –1.890	–1.675 –1.675 –1.675	–1.850 –1.850 –1.850		–1.650 –1.650 –1.650	–1.825 –1.825 –1.825	–1.615 –1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3 4	–1.080 –1.080 –1.080		–0.980 –0.980 –0.980			–0.910 –0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3 4		–1.655 –1.655 –1.655			–1.630 –1.630 –1.630		–1.595 –1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{5+2+} t_{5-2-} t_{5+3+} t_{5-3-} t_{5+4+} t_{5-4-}	2 2 3 3 4 4	1.0 1.0 1.0 1.0 1.0 1.0	2.6 2.6 2.6 2.6 2.6 2.6	1.0 1.0 1.0 1.0 1.0 1.0	1.5 1.5 1.5 1.5 1.5 1.5	2.5 2.5 2.5 2.5 2.5 2.5	1.0 1.0 1.0 1.0 1.0 1.0	2.8 2.8 2.8 2.8 2.8 2.8	
Rise Time (20 to 80%)	t_{2+} t_{3+} t_{4+}	2 3 4	1.0 1.0 1.0	2.6 2.6 2.6	1.0 1.0 1.0	1.5 1.5 1.5	2.5 2.5 2.5	1.0 1.0 1.0	2.8 2.8 2.8	
Fall Time (20 to 80%)	t_{2-} t_{3-} t_{4-}	2 3 4	1.0 1.0 1.0	2.6 2.6 2.6	1.0 1.0 1.0	1.5 1.5 1.5	2.5 2.5 2.5	1.0 1.0 1.0	2.8 2.8 2.8	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
	TEST VOLTAGE VALUES (Volts)				
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8					8	1, 15, 16
Input Current	I_{inH}	5, 6, 7	*				8	1, 15, 16
	I_{inL}	5, 6, 7		*			8	1, 15, 16
Output Voltage Logic 1	V_{OH}	2 3 4	5 6 7				8 8 8	1, 15, 16 1, 15, 16 1, 15, 16
Output Voltage Logic 0	V_{OL}	2 3 4					8 8 8	1, 15, 16 1, 15, 16 1, 15, 16
Threshold Voltage Logic 1	V_{OHA}	2 3 4			5 6 7		8 8 8	1, 15, 16 1, 15, 16 1, 15, 16
Threshold Voltage Logic 0	V_{OLA}	2 3 4				5 6 7	8 8 8	1, 15, 16 1, 15, 16 1, 15, 16
Switching Times (50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	t_{5+2+} t_{5-2-} t_{5+3+} t_{5-3-} t_{5+4+} t_{5-4-}	2 2 3 3 4 4			5 5 5 5 5 5	2 2 3 3 4 4	8 8 8 8 8 8	1, 15, 16 1, 15, 16 1, 15, 16 1, 15, 16 1, 15, 16 1, 15, 16
Rise Time (20 to 80%)	t_{2+} t_{3+} t_{4+}	2 3 4			5 5 5	2 3 4	8 8 8	1, 15, 16 1, 15, 16 1, 15, 16
Fall Time (20 to 80%)	t_{2-} t_{3-} t_{4-}	2 3 4			5 5 5	2 3 4	8 8 8	1, 15, 16 1, 15, 16 1, 15, 16

* Individually test each input using the pin connections shown.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10211

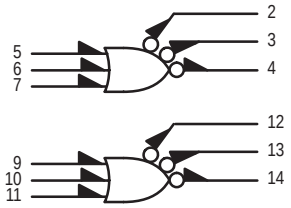
Dual 3-Input/3-Output NOR Gate

The MC10211 is designed to drive up to six transmission lines simul– taneously. The multiple outputs of this device also allow the wire "OR"–ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10211 particularly useful in clock distribution applications where minimum clock skew is desired.

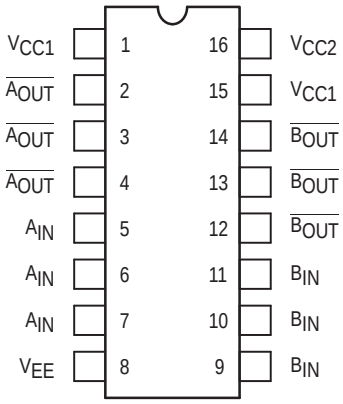
- P_D = 160 mW typ/pkg (No Loads)
- t_{pd} = 1.5 ns typ (All Output Loaded)
- t_r, t_f = 1.5 ns typ (20%–80%)

LOGIC DIAGRAM



V_{CC1} = PIN 1, 15
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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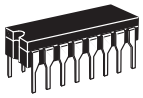
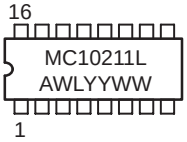
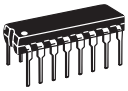
MARKING DIAGRAMS

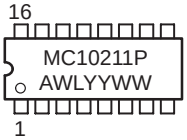


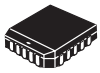
CDIP–16
L SUFFIX
CASE 620





PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10211L	CDIP–16	25 Units / Rail
MC10211P	PDIP–16	25 Units / Rail
MC10211FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		42		30	38		42	mAdc
Input Current	I_{inH}	5, 6, 7		650			410		410	μAdc
	I_{inL}	5, 6, 7	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	2 3 4	–1.060 –1.060 –1.060	–0.890 –0.890 –0.890	–0.960 –0.960 –0.960		–0.810 –0.810 –0.810	–0.890 –0.890 –0.890	–0.700 –0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3 4	–1.890 –1.890 –1.890	–1.675 –1.675 –1.675	–1.850 –1.850 –1.850		–1.650 –1.650 –1.650	–1.825 –1.825 –1.825	–1.615 –1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3 4	–1.080 –1.080 –1.080		–0.980 –0.980 –0.980			–0.910 –0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3 4		–1.655 –1.655 –1.655			–1.630 –1.630 –1.630		–1.595 –1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{5+2-} t_{5-2+} t_{5+3-} t_{5-3+} t_{5+4-} t_{5-4+}	2 2 3 3 4 4	1.0 1.0 1.0 1.0 1.0 1.0	2.6 2.6 2.6 2.6 2.6 2.6	1.0 1.0 1.0 1.0 1.0 1.0	1.5 1.5 1.5 1.5 1.5 1.5	2.5 2.5 2.5 2.5 2.5 2.5	1.0 1.0 1.0 1.0 1.0 1.0	2.8 2.8 2.8 2.8 2.8 2.8	
Rise Time (20 to 80%)	t_{2+} t_{3+} t_{4+}	2 3 4	1.0 1.0 1.0	2.6 2.6 2.6	1.0 1.0 1.0	1.5 1.5 1.5	2.5 2.5 2.5	1.0 1.0 1.0	2.8 2.8 2.8	
Fall Time (20 to 80%)	t_{2-} t_{3-} t_{4-}	2 3 4	1.0 1.0 1.0	2.6 2.6 2.6	1.0 1.0 1.0	1.5 1.5 1.5	2.5 2.5 2.5	1.0 1.0 1.0	2.8 2.8 2.8	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

TEST VOLTAGE VALUES (Volts)

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8					8	1, 15, 16
Input Current	I_{inH}	5, 6, 7	*				8	1, 15, 16
	I_{inL}	5, 6, 7		*			8	1, 15, 16
Output Voltage Logic 1	V_{OH}	2					8	1, 15, 16
		3					8	1, 15, 16
		4					8	1, 15, 16
Output Voltage Logic 0	V_{OL}	2	5				8	1, 15, 16
		3	6				8	1, 15, 16
		4	7				8	1, 15, 16
Threshold Voltage Logic 1	V_{OHA}	2				5	8	1, 15, 16
		3				6	8	1, 15, 16
		4				7	8	1, 15, 16
Threshold Voltage Logic 0	V_{OLA}	2			5		8	1, 15, 16
		3			6		8	1, 15, 16
		4			7		8	1, 15, 16
Switching Times (50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	t_{5+2-}	2			5	2	8	1, 15, 16
	t_{5-2+}	2			5	2	8	1, 15, 16
	t_{5+3-}	3			5	3	8	1, 15, 16
	t_{5-3+}	3			5	3	8	1, 15, 16
	t_{5+4-}	4			5	4	8	1, 15, 16
	t_{5-4+}	4			5	4	8	1, 15, 16
Rise Time (20 to 80%)	t_{2+}	2			5	2	8	1, 15, 16
	t_{3+}	3			5	3	8	1, 15, 16
	t_{4+}	4			5	4	8	1, 15, 16
Fall Time (20 to 80%)	t_{2-}	2			5	2	8	1, 15, 16
	t_{3-}	3			5	3	8	1, 15, 16
	t_{4-}	4			5	4	8	1, 15, 16

* Individually test each input using the pin connections shown.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10212

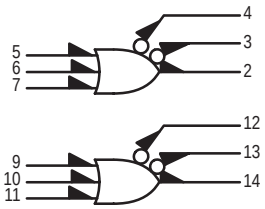
High Speed Dual 3-Input/ 3-Output OR/NOR Gate

The MC10212 is designed to drive up to six transmission lines simul– taneously. The multiple outputs of this device also allow the wire "OR"–ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10212 particularly useful in clock distribution applications where minimum clock skew is desired.

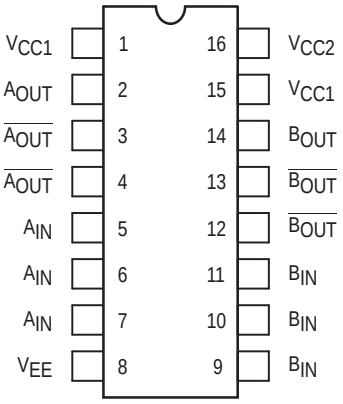
- P_D = 160 mW typ/pkg (No Load)
- t_{pd} = 1.5 ns typ (All Outputs Loaded)
- t_r, t_f = 1.5 ns typ (20%–80%)

LOGIC DIAGRAM



V_{CC1} = PIN 1, 15
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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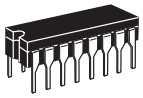
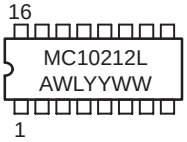
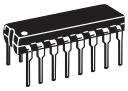
MARKING DIAGRAMS

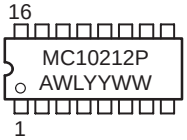


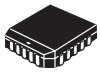
CDIP–16
L SUFFIX
CASE 620





PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10212L	CDIP–16	25 Units / Rail
MC10212P	PDIP–16	25 Units / Rail
MC10212FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		42		30	38		42	mAdc
Input Current	I_{inH}	5, 6, 7		650			410		410	μAdc
	I_{inL}	5, 6, 7	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	2 3 4	–1.060 –1.060 –1.060	–0.890 –0.890 –0.890	–0.960 –0.960 –0.960		–0.810 –0.810 –0.810	–0.890 –0.890 –0.890	–0.700 –0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3 4	–1.890 –1.890 –1.890	–1.675 –1.675 –1.675	–1.850 –1.850 –1.850		–1.650 –1.650 –1.650	–1.825 –1.825 –1.825	–1.615 –1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3 4	–1.080 –1.080 –1.080		–0.980 –0.980 –0.980			–0.910 –0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3 4		–1.655 –1.655 –1.655			–1.630 –1.630 –1.630		–1.595 –1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{5+2+} t_{5-2-} t_{5+3-} t_{5-3+} t_{5+4-} t_{5-4+}	2 2 3 3 4 4	1.0 1.0 1.0 1.0 1.0 1.0	2.6 2.6 2.6 2.6 2.6 2.6	1.0 1.0 1.0 1.0 1.0 1.0	1.5 1.5 1.5 1.5 1.5 1.5	2.5 2.5 2.5 2.5 2.5 2.5	1.0 1.0 1.0 1.0 1.0 1.0	2.8 2.8 2.8 2.8 2.8 2.8	
Rise Time (20 to 80%)	t_{2+} t_{3+} t_{4+}	2 3 4	1.0 1.0 1.0	2.6 2.6 2.6	1.0 1.0 1.0	1.5 1.5 1.5	2.5 2.5 2.5	1.0 1.0 1.0	2.8 2.8 2.8	
Fall Time (20 to 80%)	t_{2-} t_{3-} t_{4-}	2 3 4	1.0 1.0 1.0	2.6 2.6 2.6	1.0 1.0 1.0	1.5 1.5 1.5	2.5 2.5 2.5	1.0 1.0 1.0	2.8 2.8 2.8	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

TEST VOLTAGE VALUES (Volts)

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8					8	1, 15, 16
Input Current	I_{inH}	5, 6, 7	5, 6, 7*				8	1, 15, 16
	I_{inL}	5, 6, 7		5, 6, 7*			8	1, 15, 16
Output Voltage Logic 1	V_{OH}	2	5				8	1, 15, 16
		3					8	1, 15, 16
		4					8	1, 15, 16
Output Voltage Logic 0	V_{OL}	2					8	1, 15, 16
		3	5				8	1, 15, 16
		4	5				8	1, 15, 16
Threshold Voltage Logic 1	V_{OHA}	2			5		8	1, 15, 16
		3				5	8	1, 15, 16
		4				5	8	1, 15, 16
Threshold Voltage Logic 0	V_{OLA}	2				5	8	1, 15, 16
		3			5		8	1, 15, 16
		4			5		8	1, 15, 16
Switching Times (50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	t_{5+2+}	2			5	2	8	1, 15, 16
	t_{5-2-}	2			5	2	8	1, 15, 16
	t_{5+3-}	3			5	3	8	1, 15, 16
	t_{5-3+}	3			5	3	8	1, 15, 16
	t_{5+4-}	4			5	4	8	1, 15, 16
	t_{5-4+}	4			5	4	8	1, 15, 16
Rise Time (20 to 80%)	t_{2+}	2			5	2	8	1, 15, 16
	t_{3+}	3			5	3	8	1, 15, 16
	t_{4+}	4			5	4	8	1, 15, 16
Fall Time (20 to 80%)	t_{2-}	2			5	2	8	1, 15, 16
	t_{3-}	3			5	3	8	1, 15, 16
	t_{4-}	4			5	4	8	1, 15, 16

* Individually test each input using the pin connections shown.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10216

High Speed Triple Line Receiver

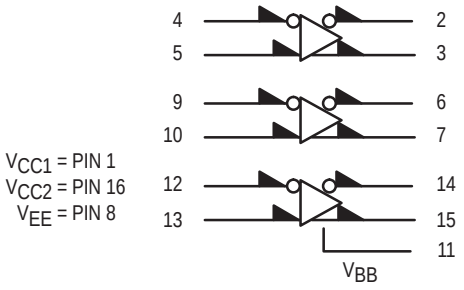
The MC10216 is a high speed triple differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 11 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10216 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 11) to prevent upsetting the current source bias network.

Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to provide complement outputs of the input logic function.

- P_D = 100 mW typ/pkg (No Load)
- t_{pd} = 1.8 ns typ (Single ended)
- = 1.5 ns typ (Differential)
- t_r, t_f = 1.5 ns typ (20%–80%)

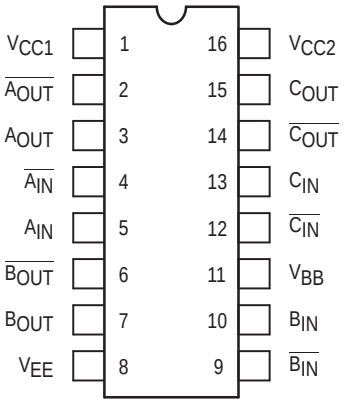
LOGIC DIAGRAM



*V_{BB} to be used to supply bias to the MC10216 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor.

When the input pin with bubble goes positive, it's respective output pin with bubble goes positive.

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

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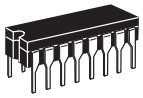
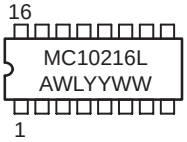
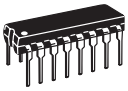
MARKING DIAGRAMS

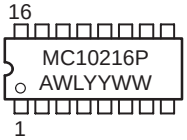


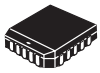
CDIP–16
L SUFFIX
CASE 620





PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10216L	CDIP–16	25 Units / Rail
MC10216P	PDIP–16	25 Units / Rail
MC10216FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		27		20	25		27	mAdc
Input Current	I_{inH}	4		180			115		115	μAdc
	I_{CBO}	4 9		1.5 1.5			1.0 1.0		1.0 1.0	μAdc
Output Voltage Logic 1	V_{OH}	2 3	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Reference Voltage	V_{BB}	11	–1.420	–1.280	–1.350		–1.230	–1.295	–1.150	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{4+2+} t_{4-2-} t_{4+3-} t_{4-3+}	2 2 3 3	1.0 1.0 1.0 1.0	2.6 2.6 2.6 2.6	1.0 1.0 1.0 1.0	1.8* 1.8* 1.8* 1.8*	2.5 2.5 2.5 2.5	1.0 1.0 1.0 1.0	2.8 2.8 2.8 2.8	
Rise Time (20 to 80%)	t_{2+} t_{3+}	2 3	1.0 1.0	2.6 2.6	1.0 1.0	1.5 1.5	2.5 2.5	1.0 1.0	2.8 2.8	
Fall Time (20 to 80%)	t_{2-} t_{3-}	2 3	1.0 1.0	2.6 2.6	1.0 1.0	1.5 1.5	2.5 2.5	1.0 1.0	2.8 2.8	

* Delay is 1.5ns when inputs are driven differentially.
Delay is 1.8ns when inputs are driven single ended.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)						
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{BB}	V_{EE}	
–30°C			–0.890	–1.890	–1.205	–1.500	From Pin 11	–5.2	
+25°C			–0.810	–1.850	–1.105	–1.475		–5.2	
+85°C			–0.700	–1.825	–1.035	–1.440		–5.2	
Characteristic		**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					**(V_{CC}) Gnd**
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{BB}	V_{EE}
Power Supply Drain Current		I_E	8	4, 9, 12				5, 10, 13	8	1, 16
Input Current		I_{inH}	4	4	9, 12			5, 10, 13	8	1, 16
		I_{CBO}	4 9		9, 12 4, 12			5, 10, 13 5, 10, 13	8, 4 8, 9	1, 16
Output Voltage	Logic 1	V_{OH}	2 3	4 9, 12	9, 12 4			5, 10, 13 5, 10, 13	8 8	1, 16 1, 16
Output Voltage	Logic 0	V_{OL}	2 3	9, 12 4	4 9, 12			5, 10, 13 5, 10, 13	8 8	1, 16 1, 16
Threshold Voltage	Logic 1	V_{OHA}	2 3	 9, 12	9, 12	4	 4	5, 10, 13 5, 10, 13	8 8	1, 16 1, 16
Threshold Voltage	Logic 0	V_{OLA}	2 3	 9, 12	9, 12	 4	4	5, 10, 13 5, 10, 13	8 8	1, 16 1, 16
Reference Voltage		V_{BB}	11					5, 10, 13	8	1, 16
Switching Times	(50Ω Load)					**Pulse In**	**Pulse Out**		**–3.2 V**	**+2.0 V**
Propagation Delay		t_{4+2+}	2			4	2	5, 10, 13	8	1, 16
		t_{4-2-}	2			4	2	5, 10, 13	8	1, 16
		t_{4+3-}	3			4	3	5, 10, 13	8	1, 16
		t_{4-3+}	3			4	3	5, 10, 13	8	1, 16
Rise Time	(20 to 80%)	t_{2+}	2			4	2	5, 10, 13	8	1, 16
		t_{3+}	3			4	3	5, 10, 13	8	1, 16
Fall Time	(20 to 80%)	t_{2-}	2			4	2	5, 10, 13	8	1, 16
		t_{3-}	3			4	3	5, 10, 13	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10231

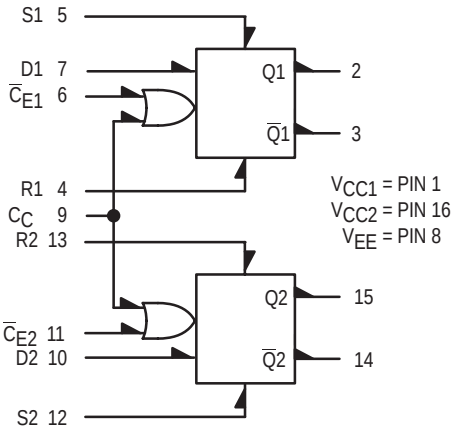
High Speed Dual Type D Master-Slave Flip-Flop

The MC10231 is a dual master–slave type D flip–flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable ($\overline{C}_E$) inputs. Each flip–flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip–flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip–flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master–slave construction.

- P_D = 270 mW typ/pkg (No Load)
- t_{pd} = 2 ns typ
- t_{Tog} = 225 MHz typ
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	X	Q_n
H	L	L
H	H	H

C = $\overline{C_E}$ + C_C. A clock H is a clock transition from a low to a high state.

R–S TRUTH TABLE

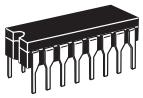
R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

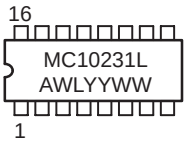
ON Semiconductor

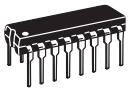
http://onsemi.com

MARKING DIAGRAMS

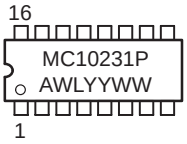


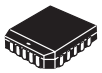
CDIP–16
L SUFFIX
CASE 620



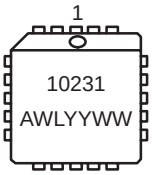


PDIP–16
P SUFFIX
CASE 648



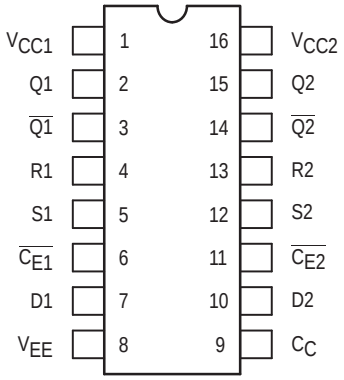


PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ORDERING INFORMATION

Device	Package	Shipping
MC10231L	CDIP–16	25 Units / Rail
MC10231P	PDIP–16	25 Units / Rail
MC10231FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		72		52	65		72	mAdc
Input Current	I_{inH}	4 5 6 7 9		650 650 350 350 460			410 410 220 220 290		410 410 220 220 290	µAdc
	I_{inL}	4, 5* 6, 7, 9*			0.5 0.5					µAdc
Output Voltage Logic 1	V_{OH}	2 2†	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	3 3†	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 2†	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	3 3†		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load) Clock Input										ns
Propagation Delay	t_{9+2-} t_{6+2+}	2 2	1.5 1.5	3.4 3.4	1.5 1.5	2.0 2.0	3.3 3.3	1.6 1.6	3.7 3.7	
Rise Time (20 to 80%)	t_{2+}	2	0.9	3.3	1.0	1.3	3.1	1.0	3.6	
Fall Time (20 to 80%)	t_{2-}	2	0.9	3.3	1.0	1.3	3.1	1.0	3.6	
Set Input										ns
Propagation Delay	t_{5+2+} t_{12+15+} t_{5+3-} t_{12+14-}	2 15 3 14	1.1 1.1 1.1 1.1	3.4 3.4 3.4 3.4	1.1 1.1 1.1 1.1	2.0 2.0 2.0 2.0	3.3 3.3 3.3 3.3	1.2 1.2 1.2 1.2	3.7 3.7 3.7 3.7	
Reset Input										ns
Propagation Delay	t_{4+2-} t_{13+15-} t_{4+3-} t_{13+14+}	2 15 3 14	1.1 1.1 1.1 1.1	3.4 3.4 3.4 3.4	1.1 1.1 1.1 1.1	2.0 2.0 2.0 2.0	3.3 3.3 3.3 3.3	1.2 1.2 1.2 1.2	3.7 3.7 3.7 3.7	
Setup Time	t_{setup}	7	1.5		1.0			1.5		ns
Hold Time	t_{hold}	7	0.9		0.75			0.9		ns
Toggle Frequency (Max)	f_{tog}	2	200		200	225		200		MHz

* Individually test each input; apply V_{ILmin} to pin under test.

† Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ Input (Pin 6)

ELECTRICAL CHARACTERISTICS (continued)

				TEST VOLTAGE VALUES (Volts)					
			@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
			–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
			+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
			+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	4 5 6 7 9	4 5 6 7 9				8 8 8 8 8	1, 16 1, 16 1, 16 1, 16 1, 16
		I_{inL}	4, 5* 6, 7, 9*		* *			8 8	1, 16 1, 16
Output Voltage	Logic 1	V_{OH}	2 2†	5 7				8 8	1, 16 1, 16
Output Voltage	Logic 0	V_{OL}	3 3†	5 7				8 8	1, 16 1, 16
Threshold Voltage	Logic 1	V_{OHA}	2 2†			5 7	 9	8 8	1, 16 1, 16
Threshold Voltage	Logic 0	V_{OLA}	3 3†			5 7	 9	8 8	1, 16 1, 16
Switching Times (50Ω Load) Clock Input				**+1.11Vdc**		**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
	Propagation Delay	t_{9+2-} t_{6+2+}	2 2	 7		9 6	2 2	8 8	1, 16 1, 16
Rise Time	(20 to 80%)	t_{2+}	2	7		9	2	8	1, 16
Fall Time	(20 to 80%)	t_{2-}	2			9	2	8	1, 16
Set Input									
	Propagation Delay	t_{5+2+} t_{12+15+} t_{5+3-} t_{12+14-}	2 15 3 14	 6 9		5 12 5 12	2 15 3 14	8 8 8 8	1, 16 1, 16 1, 16 1, 16
Reset Input									
	Propagation Delay	t_{4+2-} t_{13+15-} t_{4+3-} t_{13+14+}	2 15 3 14	 6 9		4 13 4 13	2 15 3 14	8 8 8 8	1, 16 1, 16 1, 16 1, 16
Setup Time		t_{setup}	7			6, 7	2	8	1, 16
Hold Time		t_{hold}	7			6, 7	2	8	1, 16
Toggle Frequency (Max)		f_{tog}	2	* *		6	2	8	1, 16

* Individually test each input applying V_{IH} or V_{IL} to input under test.

† Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ Input (Pin 6)

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

CHAPTER 4
Carrier Band Modem

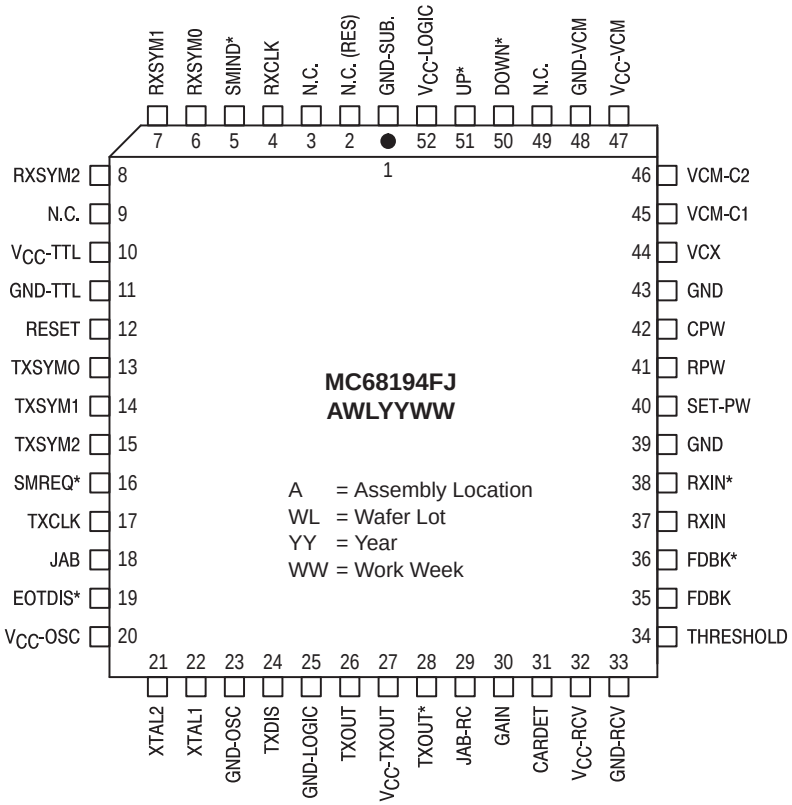
MC68194

Carrier Band Modem (CBM)

The bipolar LSI MC68194 Carrier Band Modem (CBM) when combined with the MC68824 Token Bus Controller provides an IEEE 802.4 single channel, phase–coherent carrier band Local Area Network (LAN) connection. The CBM performs the Physical Layer function including symbol encoding/decoding, signal transmission and reception, and physical management. Features include:

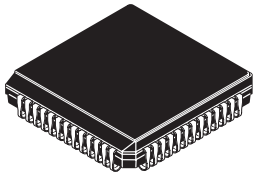
- Implements IEEE 802.4 single channel, phase–coherent Frequency Shift Keying (FSK) physical layer including receiver blanking.
- Provides physical layer management including local loopback mode, transmitter enable, and reset.
- Supports data rates from 1 to 10 Mbps. IEEE 802.4 standard uses 5 or 10 Mbps.
- Interfaces via standard serial interface to MC68824 Token Bus Controller.
- Crystal controlled transmit clock.
- Recovery of clocked data through phase–locked loop.
- RC controlled Jabber Inhibit Timer.
- Single +5.0 volt power supply.
- Available in 52–lead Cerquad package.

PIN ASSIGNMENTS AND DEVICE MARKING



ON Semiconductor

http://onsemi.com



CERQUAD
FJ SUFFIX
CASE 778B

ORDERING INFORMATION

Device	Package	Shipping
MC68194FJ	CERQUAD	20 Units / Rail
MC68194FJR2	CERQUAD	450 Units / Reel

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SECTION 1
GENERAL DESCRIPTION

1.1 TOKEN BUS LAN CARRIER BAND NODE OVERVIEW

The MC68194 Carrier Band Modem (CBM) is part of Motorola's solution for an IEEE 802.4 token bus carrier band Local Area Network (LAN) node. The CBM integrates the function of the single–channel, phase–coherent Frequency Shift Keying (FSK) physical layer. Figure 1–1 illustrates the architecture of a token bus LAN node as commonly used in Manufacturing Automation Protocol (MAP) industrial communications. Based on the ISO–OSI model, the LLC Sublayer and additional upper layers are typically supported by a local MPU subsystem, while the IEEE 802.4 token bus MAC Sublayer and Physical Layer are implemented by the MC68824 Token Bus Controller (TBC) and MC68194 CBM respectively.

The MC68194 provides the three basic functions of the physical layer including data transmission to the coax cable, data reception from the cable, and management of the physical layer. For standard data mode (also called MAC mode), the carrier band modem receives a serial transmit data stream from the MC68824 TBC (called symbols or atomic symbols), encodes, modulates the carrier, and transmits the signal to the coaxial cable. Also in the data mode, the CBM receives a signal from the cable, demodulates the signal, recovers the data, and sends the received data symbols to the TBC. Communication between the TBC and CBM is through a standardized serial interface inconsistent with the IEEE 802.4 DTE–DCE serial interface.

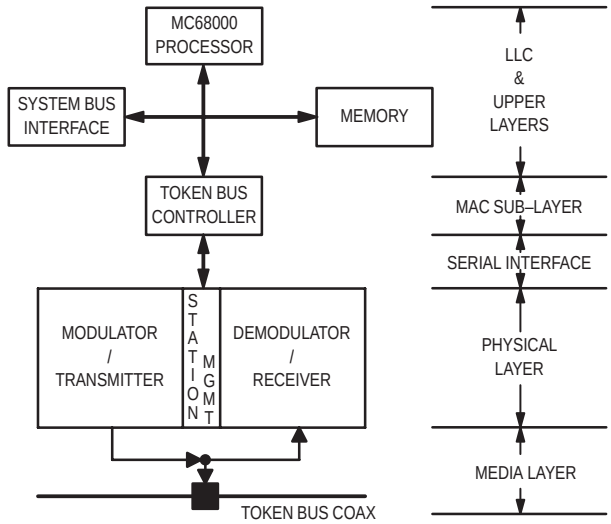


Figure 1–1. IEEE 802.4 Token Bus Carrier Band Node

The physical layer management provides the ability to reset the CBM, control the transmitter, and do loopback testing. Also, an onboard RC timer provides a "jabber" inhibit function to turn off the transmitter and report an error condition if the transmitter has been continuously on for too long. Similar to the data mode, the CBM management mode makes use of the TBC serial interface.

1.2 CARRIER BAND MODULATION TECHNIQUE

The CBM uses phase–coherent frequency shift keying (FSK) modulation on a single channel system. In this modulation technique, the two signaling frequencies are integrally related to the data rate, and transitions between the two signaling frequencies are made at zero crossings of the carrier waveform. Figure 1–2 shows the data rate and signaling frequencies. An {L} is represented as one half cycle of a signal, starting and ending with a nominal zero amplitude, whose period is equal to the period of the data rate, with the phase of one half cycle changing at each successive {L}. An {H} is represented as one full cycle of a signal, starting and ending with a nominal zero amplitude whose period is equal to half the period of the data rate. In a 5 Mbps implementation, the frequency of {L} is 5.0 MHz and for {H} is 10 MHz. For a 10 Mbps implementation, the frequency of {L} is 10 MHz and for {H} is 20 MHz. The other possible physical symbol is when no signal occurs for a period equal to one half of the period of the data rate. This condition is represented by {off}.

Data Rate MBPS	Frequency of Lower Tone MHz {L}	Frequency of Higher Tone MHz {H}
5	5.0	10
10	10	20

Figure 1–2. Data Rate versus Signaling Frequencies

The specified physical symbols ({L}, {H} and {off}) are combined into pairs which are called MAC–symbols. The MAC–symbols are transferred across the serial link. The encodings for the five MAC–symbols are shown in Figure 1–3. Figure 1–4 shows the phase coherent FSK modulation scheme for ONE, ZERO, and NON–DATA. The IEEE 802.4 document does not specify the polarity used to transmit data on the physical cable. The receiver must operate without respect to polarity.

Mac–Symbol	Encoding
Silence	{off off}
Pad–Idle Pairs	{L L} {H H}
Zero	{H H}
One	{L L}
Non–Data	
ND1	{H L}
ND2	{L H}

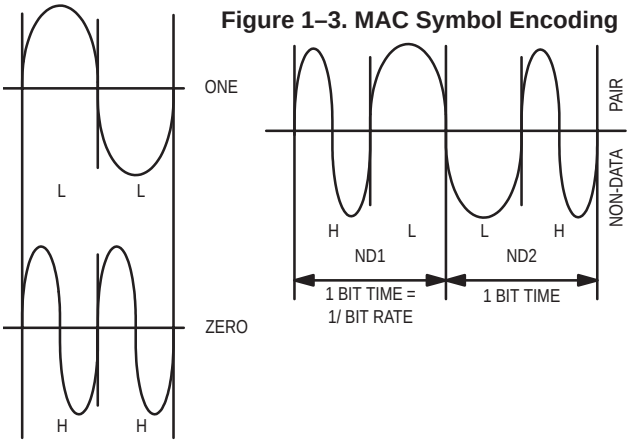


Figure 1–3. MAC Symbol Encoding

Figure 1–4. Phase–Coherent Modulation Scheme

1.3 MESSAGE (FRAME) FORMAT

Although the CBM only uses MAC symbols one–at–a–time, the MAC or TBC is responsible for combining the above defined MAC symbols into messages (more correctly called frames). For the purposes of the CBM, a simplified frame format can be used consisting of:

SILENCE || PAD–IDLE | START DELIMITER | DATA | END DELIMITER || SILENCE

where:

PAD–IDLE = alternating {LL} {HH} pairs which must occur in octets or groups of eight symbols. Pad–idle provides a training signal for the receiver and occurs at the beginning of every transmission (and between frames in a multiple frame transmission).

START DELIMITER = a unique pattern of eight symbols (one octet) that marks the beginning of a frame. The pattern is:
ND1 ND2 0 ND1 ND2 0 0 0
where ND1 is the first symbol transmitted.

DATA = octets of ZERO/ONE patterns that are the actual data or “information” contained within the frame.

END DELIMITER = a unique pattern of symbols that marks the end of a frame. The pattern is:
ND1 ND2 1 ND1 ND2 1 {I=0/1} {0/1}
where ND1 is the first symbol transmitted. Note that unlike the Start Delimiter, the last two bits of the End Delimiter octet are not always the same. The seventh bit of the octet is called the I Bit or Intermediate bit which = 1 when there is more to transmit and = 0 at the end of a transmission.

A single transmission can consist of one or more frames. In a multi–frame transmission, Pad–Idle is sent between consecutive frames to separate them. If an End Delimiter occurs **within** a multi–frame transmission its I Bit will = 1, and the **last** end delimiter will have its I Bit = 0.

The CBM accepts a stream of MAC symbols from the TBC and modulates the phase–coherent transmit signal accordingly. Conversely, the CBM receives a phase–coherent signal stream from the cable, decodes the MAC symbols, and reports them. On transmission there is a direct one–to–one correlation between MAC symbols requested and the modulated signal; however, during reception exceptions can occur. The CBM is allowed to report Silence or the actual Zero/One pattern during preamble which is done to allow the receiver to “train” to the incoming signal. Also, if noise in the system has corrupted the data, it may show up as an incorrect MAC symbol or the CBM can report a BAD SIGNAL symbol if an incorrect combination of ND symbols is detected (ND2 without an ND1, ND2 followed by ND2, etc.)

1.4 SYSTEM CONFIGURATION

Figure 1–5 illustrates the CBM and peripheral circuitry required for an IEEE 802.4 carrierband 5 Mbps or 10 Mbps data rate phase–coherent FSK physical layer. The CBM communicates with the MAC or TBC through a TTL compatible serial interface that is consistent with the IEEE 802.4 exposed DTE–DCE interface. Management and transmission symbol requests are accepted via the CBM physical data request channel (TXSYM0–TXSYM2, SMREQ*, and TXCLK). The physical data indication channel (RXSYM0–RXSYM2, SMIND*, and RXCLK) is used to send received symbols and management responses to the MAC.

The periphery circuitry is primarily associated with interface to the LAN coaxial cable and data recovery. An external crystal or clock source is required (20 MHz for 5 Mbps data rate or 40 MHz for 10 Mbps data rate) for onboard timing and transmit clock. Also, an RC timing network sets the jabber timeout period.

The coaxial cable interface combines the transmit and receive signal functions. For transmission, the CBM provides differential drive signals (TXOUT and TXOUT*) whose signaling is ECL levels referenced to V_{CC} (logic high $\approx$ +4.1 V, logic low $\approx$ + 3.3 V) and a gate signal called TXDIS. The IEEE 802.4 standard puts specific requirements on the signal transmitted to the cable:

Between +63 dB and +66 dB (1.0 mV, 75 Ω) [dBmV] output voltage level.

Transmitter–off leakage not to exceed –20 dB (1.0 mV, 75 Ω) [dBmV].

Signal transition time window (eye pattern) dependent on data rate.

Because of this, an external amplifier with waveshaping is required. The CBM TXOUT/TXOUT* outputs provide complementary signals with virtually no slew, and the TXDIS is an enable signal helpful for turning the external amp off “hard” to meet the low level leakage.

On the reception side, the CBM requires a pre–amplifier to receive the low level signal from the cable. The signal available at the “F”–connector can range from +10 dB to +66 dB (1.0 mV, 75 Ω) [dBmV]. The signal required at the CBM is about 12 dB above this (net gain through the transformer, pre–amp, and any filtering). The receiver can be used in full differential or single–ended mode.

A second part of the receiver function is the signal detect or carrier detect function. The IEEE 802.4 requires that the receiver detect a signal of +10 dBmV or above (i.e., be turned “on”) and report Silence for a signal of +4.0 dBmV or below (i.e., be turned “off”). Therefore, a 6.0 dB (2:1 voltage ratio) range or window is defined in which the signal detect must switch. The CBM is optimized for this range (including the pre–amp gain), although it is trimmed via an external THRESHOLD.

The remaining external components are associated with clock recovery. A capacitor and resistor (internal R also provided) set one–shot timing, and an active filter for a PLL used in clock and data recovery is required. The active filter can be implemented via an op amp, or if 5.0 volt operation is required, an alternate charge pump design can be used.

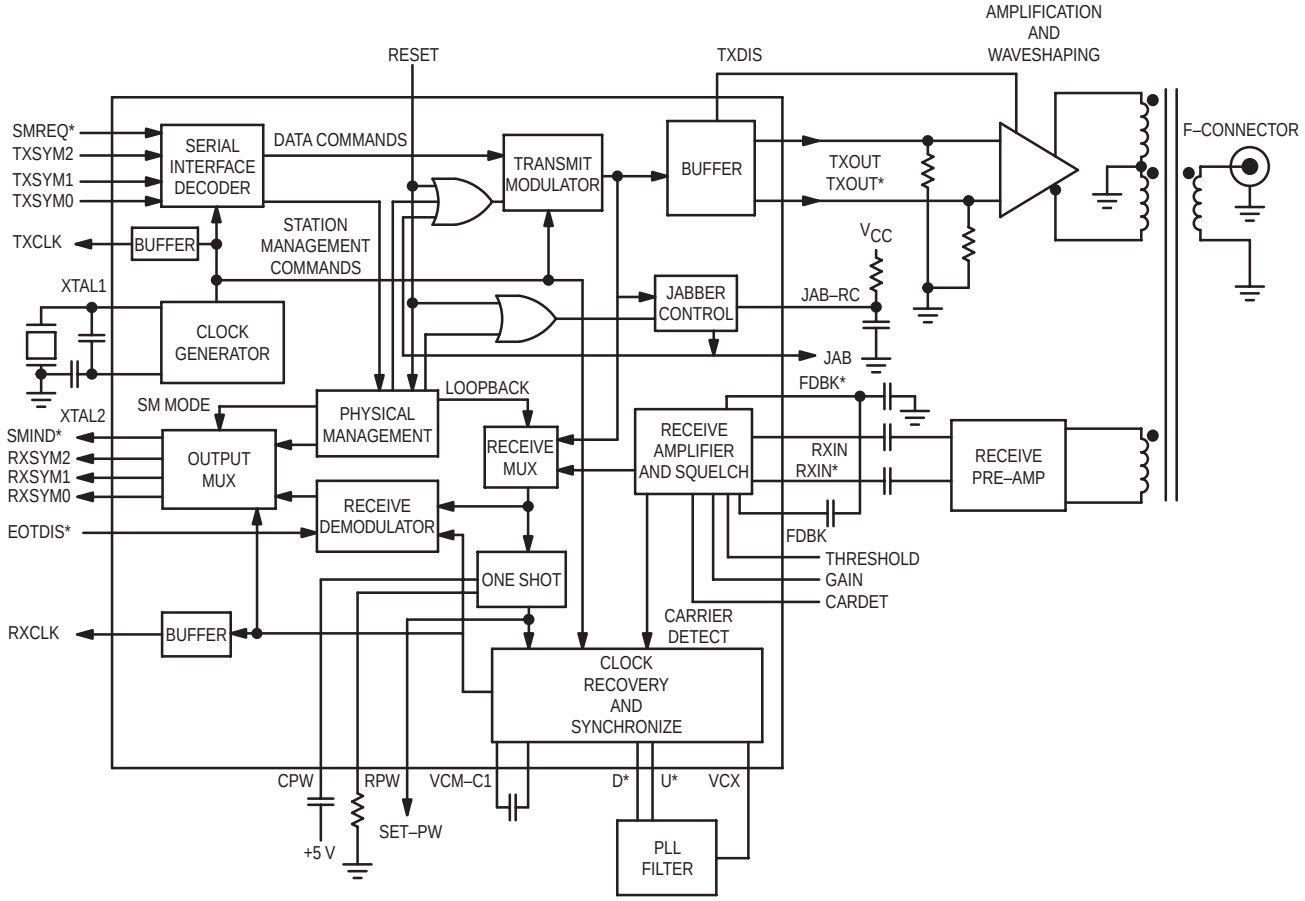


Figure 1–5. Functional Block Diagram

The clock recovery and data decoder is a synchronous design which provides superior performance minimizing clock jitter.

Although primarily intended for the IEEE 802.4 carrier band, the CBM is also an excellent device for point–to–point data links, fiberoptic modems, and proprietary LANs. The MC68194 can be used over a wide range of frequencies and interfaces easily into different kinds of media.

SECTION 2
SIGNAL DESCRIPTION

Symbol	Type	Name/Description
TXSYM0–TXSYM2	**TTL/I***	**TRANSMIT SYMBOLS** — These TTL inputs are request channel signals used to send either serial transmission symbols in the MAC mode or commands in station management mode. They are synchronized to TXCLK and are normally connected to the TXSYMX outputs of the MC68824. SMREQ* selects the meaning of these signals as either MAC mode or management mode.
SMREQ*	**TTL/I***	**STATION MANAGEMENT REQUEST** — A TTL input that selects the mode of the request channel signals TXSYMX. Synchronized to TXCLK, SMREQ* is equal to one for MAC mode and equal to zero for management mode. It is normally driven by the SMREQ* output of the MC68824.
TXCLK	**TTL/O**	**TRANSMIT CLOCK** — A TTL clock output generated from the crystal oscillator (it is 1/4 of the oscillator frequency) used to receive request channel symbols from the MC68824. TXCLK is equal to the data rate of the application (5.0 MHz or 10 MHz for IEEE 802.4). TXSYMX and SMREQ* are synchronized to the **positive** edge of TXCLK which is supplied to the MC68824.
RXSYM0–RXSYM2	**TTL/O**	**RECEIVE SYMBOLS** — These TTL outputs are indication channel signals used to provide either serial receive symbols in MAC mode or command confirmation/indication in station management mode. They are synchronized to RXCLK and are normally connected to the RXSYMX inputs of the MC68824. SMIND* selects the meaning of these signals as either MAC mode or management mode.
SMIND*	**TTL/O**	**STATION MANAGEMENT INDICATION** — A TTL output that indicates the mode of the CBM and RXSYMX lines. Synchronized to RXCLK, SMIND* is equal to one for MAC mode and equal to zero for management mode. It is normally connected to the SMIND* input of the MC68824.
RXCLK	**TTL/O**	**RECEIVE CLOCK** — A TTL clock output used to send indication channel symbols to the MC68824. Its frequency is nominally equal to the data rate (5.0 MHz or 10 MHz for IEEE 802.4). RXCLK is generated from a PLL that is locked to the local oscillator during loopback, station management, or the absence of received data. During frame reception the PLL is locked to the incoming received data. RXSYMX and SMIND* are synchronized to **negative** edge of RXCLK.
EOTDIS*	**TTL/I***	**END–OF–TRANSMISSION DISABLE** — When low, this TTL input disables the end–of–transmission receiver blanking required by the IEEE 802.4 Spec, Section 12.7.6.3. When high the blanking works in accordance with the spec requirements.
TXOUT,TXOUT*	**ECL/O**	**TRANSMIT OUTPUTS** — A differential output signal pair (MECL level referenced to V_{CC}) used to drive the transmitter circuitry. The silence or “off” state is both outputs one (high). The output data stream is phase–coherent FSK encoded.
TXDIS	**OC**	**TRANSMIT DISABLE** — An open collector output used to disable transmitter circuitry. This output is high when the transmitter is off (TXOUT and TXOUT* both high).
JAB	**TTL/O**	**JABBER** — A TTL output signal generated from the jabber–inhibit timer. When equal to one, JAB indicates the timer has timed–out and an error has occurred.
RESET	**TTL/I***	**RESET** — A TTL input signal that when high asynchronously resets the CBM.

*All TTL inputs include a 15 kΩ pullup resistor to V_{CC}.

Signal Description (Cont.)

Symbol	Type	Name/Description
RXIN, RXIN*	**I**	**RECEIVER INPUTS** — A differential input signal pair for the receiver amplifier/limiter. These inputs may be used differentially or single ended.
FDBK, FDBK*		**DC FEEDBACK BYPASS** — These two points are provided to bypass dc feedback around the receiver amplifier.
THRESHOLD	**I**	**THRESHOLD ADJUST** — The receiver threshold detect is trimmed with this pin.
GAIN	**O**	**GAIN** — This output can be used to monitor the receiver amplifier output signal. Used only for test purposes.
CARDET	**O**	**CARRIER DETECT** — This output can be used to filter the internal signal that is sampled to sense carrier detect.
RPW, CPW	**I**	**PULSE–WIDTH RESISTOR/CAPACITOR** — A resistor and capacitor set a one–shot pulse width used in the clock recovery circuitry.
SET–PW	**O**	**PULSE WIDTH TEST POINT** — Output test point used for adjusting clock recovery one–shot pulse width.
UP*, DOWN*	**ECL/O**	**PLL PHASE DETECTOR OUTPUTS** — UP* and DOWN* are the pump–up and pump–down outputs, respectively, of the PLL digital phase detector. They are MECL levels referenced to +5.0 volts and are used to drive inputs to an active filter or charge pump for the PLL.
VCX	**I**	**VCM CONTROL** — The control voltage applied to the PLL voltage controlled multivibrator.
VCM–C1, VCM–C2	**I**	**VCM CAPACITOR** — VCM capacitor inputs. VCM frequency is 4X RXCLK.
JAB–RC	**I**	**JABBER–INHIBIT RC** — A resistor–capacitor network connected to this pin sets the jabber–inhibit time constant.
XTAL,1 XTAL2	**I**	**CLOCK CRYSTAL** — Oscillator circuit inputs may be used with a crystal or an external clock source. Oscillator frequency is 4X data rate.
V_{CC}–VCM		**VCM POWER** — 5.0 ± 5% volts for VCM.
V_{CC}–TXOUT		**TXOUT POWER** — 5.0 ± 5% volts for TXOUT/TXOUT*.
V_{CC}–OSC		**OSCILLATOR POWER** — 5.0 ± 5% volts for oscillator.
V_{CC}–RCV		**RECEIVER POWER** — 5.0 ± 5% volts for receiver amplifier/limiter.
V_{CC}		**LOGIC POWER** — 5.0 ± 5% volts for remaining logic.
V_{CC}–TTL		**TTL POWER** — 5.0 ± 5% volts for TTL output buffers.
GND–TTL, GND–VCM, GND–LOGIC, GND–OSC, GND–RCV, GND–SUBS, GND		**GROUND** — Reference voltage for TTL buffers, VCM, internal logic, oscillator, receiver/ limiter, substrate respectively. Two additional grounds are used to isolate signals.

SECTION 3
TRANSMITTER

3.1 OVERVIEW

The transmitter function includes the serial interface decoder, transmit modulator, transmit buffer, jabber inhibit, and clock generator. (Although the clock generator is not used exclusively by the transmit function, the generator will be discussed here.) The MC68194 receives request channel symbols on the TXSYMX pins which are synchronized to TXCLK. As is described in the Serial Interface discussion, MAC transmit symbols are input serially (CBM in MAC mode), decoded, and used to modulate an output signal. The Serial Interface Decoder is used both for MAC mode to decode data transmit commands (symbols) and management mode to decode management commands. The decoded transmit commands or symbols are used by the Transmit Modulator to generate phase–coherent signaling as discussed in the CBM General Description. The transmit buffer receives the modulated signal and drives differential output signals.

The clock generator provides TXCLK and internal clocks of 2 times (2X) and 4 times (4X) TXCLK. The 4X clock is actually the oscillator frequency. These clocks are used to receive the TX symbols and generate the modulated signal.

3.2 TRANSMIT BUFFER

The modulated transmit data stream drives the TXOUT and TXOUT* pins of the MC68194. These pins are complementary outputs with closely matched edge transitions. This is useful in helping meet the IEEE 802.4 carrierband requirement for a transmit jitter of less than ±1% of the data rate. TXOUT and TXOUT* are generally used to drive a differential amplifier which is used to achieve the necessary output level at the cable and meet the rise/fall time window (or “eye” pattern) of the IEEE 802.4. A third output called TXDIS is available to gate the amplifier circuitry on or off.

The TXTOUT and TXTOUT* have ECL levels referenced to V_{CC} (Figure 3–1). Levels are typically 4.11 V for a high and 3.25 for a low. Pulldown resistors are required with the outputs specified to drive a maximum load of 220 Ω to ground reference.

Operation of the transmit outputs is controlled in the following manner:

6. Management mode — The TX outputs are always disabled while the CBM is in management mode. When leaving management mode the TX outputs remain disabled if a RESET command has been issued and an ENABLE TRANSMITTER and DISABLE LOOPBACK commands have **not** been issued. Resetting the CBM enables internal loopback and disables the transmitter.
7. MAC (data) mode — After leaving management mode, the CBM can function in internal loopback (for test) with the transmitter disabled, out of loopback with transmitter disabled (receive only), or in standard data mode with the TX outputs controlled by the modulator.

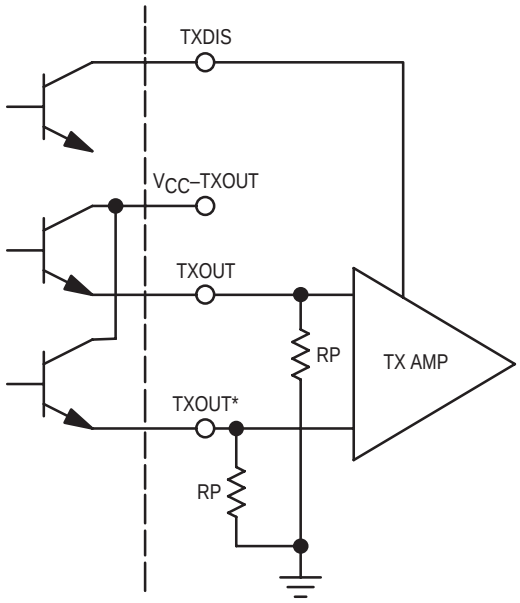


Figure 3–1. Transmitter Outputs

8. Jabber inhibit activated — If the jabber inhibit fires, it forces the CBM into management mode and disables the TX outputs. This condition can only be cleared by a reset condition.

The TXDIS output is an open collector switched current source. TXDIS sinks a nominal 0.5 mA when the TXOUT/TXOUT* outputs are enabled. TXDIS is off or high impedance when the transmitter is disabled.

The signaling on the TX outputs and TXDIS is shown in Figure 3–2. The “off” or silence condition is both TXOUT outputs high and TXDIS also high. The figure shows an example of the signal pattern for both leaving and entering a silence condition.

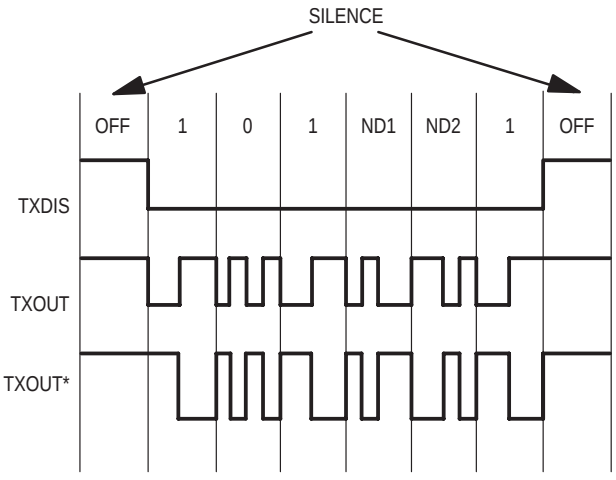


Figure 3–2. Transmitter Output Signaling

3.3 JABBER INHIBIT

The jabber inhibit function prevents the transmitter from transmitting indefinitely. An external resistor and capacitor pair tied to the CBM JAB–RC pin set the maximum time that the transmitter is allowed to transmit. When transmission is attempted for a period longer than the specified time, the jabber inhibit function forces the transmitter to shut down and alerts the system that this has been done by generating a PHYSICAL ERROR indication on the serial interface indication channel. The error indication is removed only after a reset has occurred on the RESET pin or after a RESET command has been received on the station management interface. The ENABLE TRANSMITTER and DISABLE LOOPBACK commands can then be used to re–enable the transmitter outputs. While the PHYSICAL ERROR indication is present, the normally–low JAB pin of the MC68194 will be high. This TTL output may be used to turn off external transmitter circuitry or an isolation relay.

A block diagram of the jabber inhibit function is shown in Figure 3–3. When edges are present on the TXDATA line, the jabber capacitor is allowed to charge. When the transmitter stops transmitting, the capacitor is discharged. The circuit looks for any edges in the previous 16 TXCLKs before deciding whether to charge or discharge the capacitor. When the capacitor voltage reaches the reference threshold, the comparator switches and the jabber output is latched. The jabber output is fed back internally and disables the transmitter. This signal is also brought out to the JAB pin for use in disabling external transmitter circuitry.

For the IEEE 802.4 spec, the jabber timeout must be 0.5 sec ± 25%. An RC time constant of 265 millisec. will give about a 0.5 sec timeout. The maximum resistor size is 125 kΩ. Components should be 10% tolerance or better. Common values are R = 120 kΩ and C = 2.2 μF.

3.4 CLOCK GENERATOR

The clock generator is used to generate all of the transmit timing, TXCLK, and internal CBM timing for station management and loopback. The generator consists of a crystal oscillator/buffer that drives ÷2 and ÷4 stages. The oscillator frequency must be four times (4X) the serial data rate. As an example, the IEEE 802.4 5 Mbps carrier band (TXCLK = 5.0 MHz) requires an oscillator frequency of 20 MHz. The basic circuit is a single transistor Colpitts oscillator as shown in Figure 3–4.

The oscillator is used in one of three modes depending on the data rate and the application:

1. With a parallel–resonant, fundamental mode crystal.
2. With a parallel–resonant, overtone mode crystal.
3. With an external clock source.

The fundamental mode can typically be used up to frequencies of about 20 MHz; this is crystal dependent and some crystal types can be used as high as 40 MHz. Beyond the fundamental mode upper limit, an overtone mode crystal is used. An alternative to a crystal is an external clock source such as an integrated crystal clock to drive the CBM.

3.4.1 Parallel–Resonant, Fundamental Mode Crystal

Figure 3–4 shows the external crystal and capacitors C1 and C2 used for fundamental mode operation. The crystal must be parallel resonant with a maximum series resistance of 30 Ω.

This configuration is normally used for the IEEE 802.4 5 Mbps carrierband standard. The required transmit frequency stability is ± 100 ppm (0.01%). It is suggested that a crystal with a total frequency tolerance (calibration tolerance, temperature variation, plus aging) of ± 50 ppm to ± 60 ppm be used. The remaining frequency budget is reserved for the CBM and other components over temperature and power supply variation.

The series combination of C1 and C2 should be equal to the specified crystal load (typically 20 pF or 32 pF). Additionally, C1 and C2 should be large enough to swamp out the CBM device capacitance. The XTAL1 input capacitance is typically 1.5 pF to 2.0 pF, and C1 should be at least an order of magnitude greater (C1 > 20 pF). Also, C1 must be greater than the crystal load capacitance because of the series combination of C1 and C2. Generally the ratio C1:C2 is from 1:1 to 3:1.

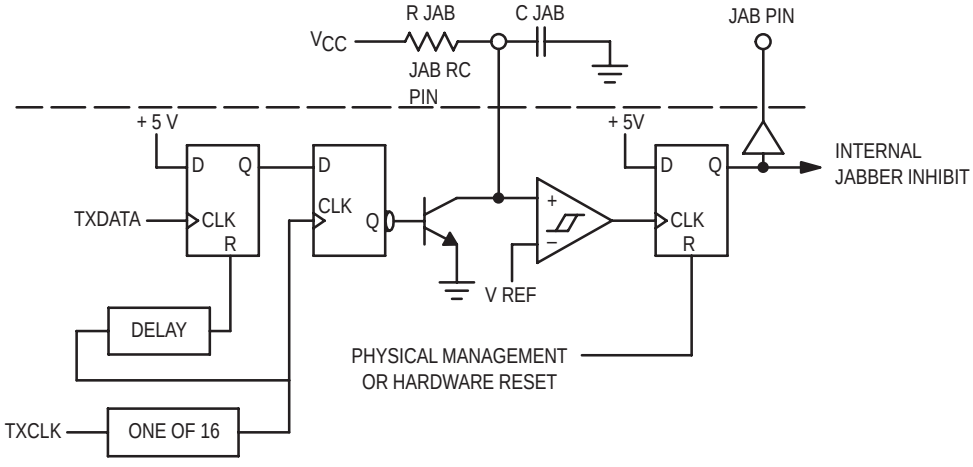


Figure 3–3. Jabber Inhibit Block Diagram

For a 20 pF crystal load:

$$20\ pF = C1C2/(C1 + C2)$$

and

$$C2 = 20\ pF\ [C1/(C1 – 20\ pF)]$$

Typical values are C1 = 60 pF and C2 = 30 pF.

It is suggested that best results will be had with close tolerance (5%) NPO ceramic capacitors — trimming should not be required. If trimming is necessary, a third trimming capacitor C3 can be placed in series with the crystal. Capacitors C1 and C2 will have to be increased in value because the crystal load now becomes C1 and C2 and C3 in series. For help in designing the capacitor network the user is directed to the *Design of Crystal and Other Harmonic Oscillators*, B. Parzen, Wiley, 1983.

3.4.2 Parallel–Resonant, Overtone Mode Crystal

Figure 3–4 also shows the network used for overtone mode operation. The crystal is still parallel resonant, but must be specified for overtone (harmonic) operation at the desired frequency. A low series resistance of less than 30 Ω is recommended.

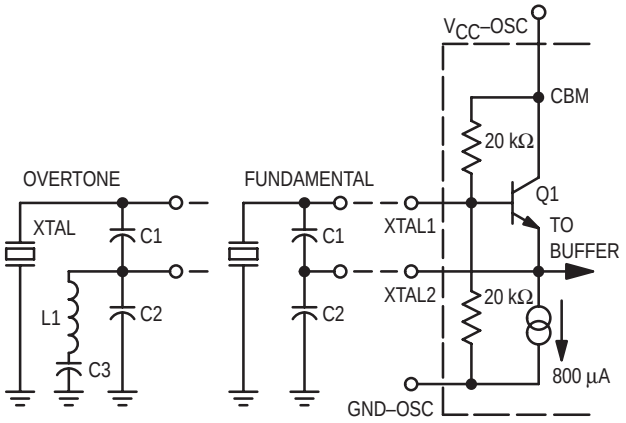


Figure 3–4. Crystal Oscillator Schematic Shows Configurations For Both Overtone and Fundamental Modes

Inductor L1 and capacitor C2 form a tank circuit that is parallel resonant at a frequency **lower** than the desired crystal harmonic but above the next lower odd harmonic. C3 = 0.01 µF is a dc blocking capacitor to ground. At the operating frequency the tank circuit impedance will appear capacitive; therefore, the load to the crystal is C1 in series with the capacitive reactance of the tank circuit.

This series combination should be equal to the desired crystal load. Typically, C2 will increase in value as compared to the fundamental mode situation because of the cancelling effects of L1. Again the user is directed to the above reference for optimum selection of components.

3.4.3 External Clock Source

Figure 3–5 shows the connection used for a TTL compatible external clock source. XTAL1 and XTAL2 are tied together defeating transistor Q1. External resistor R1 = 2.0 kΩ assures a high level greater than 3.0 V at an input current of 800 µA. The TTL driver must be capable of sinking 2.5 mA.

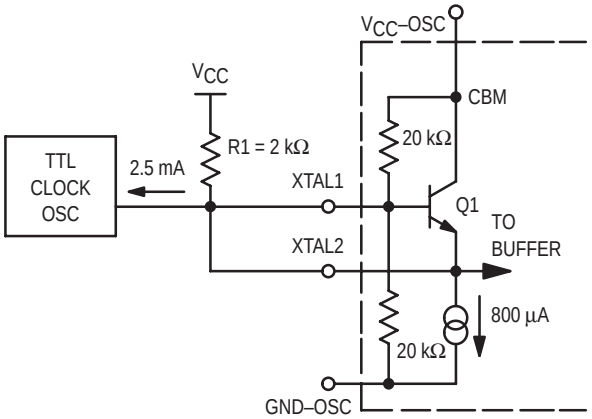


Figure 3–5. TTL Compatible Clock Source Driving CBM

The IEEE 802.4 for 5 Mbps or 10 Mbps data rate carrier band requires a transmit frequency stability of ± 100 ppm (0.01%). The external clock source must be specified for this stability over temperature.

SECTION 4
RECEIVER AMPLIFIER/LIMITER WITH CARRIER DETECT

4.1 OVERVIEW

The IEEE 802.4 spec provides that the incoming signal range for good signal is +10 dB (1.0 mV, 75 Ω) [dBmV] to +66 dB (1.0 mV, 75 Ω) [dBmV] available at the modem connector. The IEEE 802.4 further specifies that the modem will report silence for any signal below +4.0 dB (1.0 mV, 75 Ω) [dBmV]. Therefore, the receiver function must amplify any signal of +10 dBmV and above to limiting for good data recovery, and the signal detect must switch within the +4.0 dBmV to +10 dBmV window, that is, it must be “off” for +4.0 dBmV and below, and be “on” for +10 dBmV and above. The MC68194 requires a pre–amplifier of about 12 dB in front of the onboard amplifier and carrier detect function. Clock and data recovery are extracted from the amplified/limited incoming signal, and the carrier detect is used to control the clock and data recovery function based on presence of good signal.

4.2 AMPLIFIER

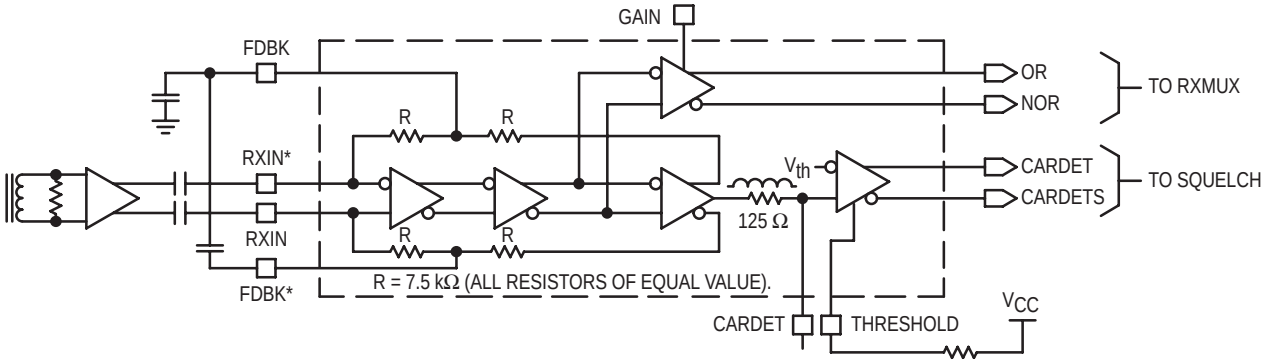
Figure 4–1 shows a simple block diagram of the receiver amplifier. Internally, dc feedback is used to bias the amplifier, and connection points FDBK and FDBK* are provided to ac bypass the feedback. With both receiver inputs RXIN and RXIN* available, the device can be wired either for differential or single–ended operation. Differential is preferred for low noise.

An external preamplifier with gain of about 12 dB is used with the onboard amplifier. The pre–amp can drive the CBM either single–ended or differentially. The onboard amplifier output signal is used in two ways. One path adds an additional limiter stage and is used to drive the clock and data recovery stages. The second path is used to develop carrier detect.

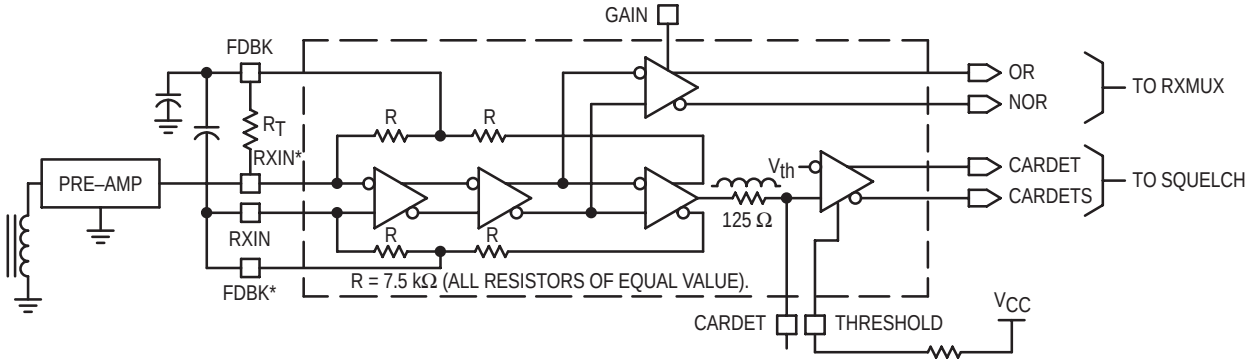
In the signal window where carrier detect must be active, the internal amplifier remains in the linear (non–limiting) range. Its output is fullwave rectified, and the rectified signal is compared to an onboard threshold that is temperature and voltage compensated. The rectified signal is also brought out to an external lead called CARDET. A capacitor can be added at this pin which combines with the series 125 Ω resistor to form a low pass filter. This filtering is used to knock any high frequency noise off of the signal. The output of the comparator is a series of pulses (when the signal amplitude is sufficiently large) which are digitally integrated in the internal squelch signal.

4.3 CARRIER DETECTION THRESHOLD

The carrier detect threshold is internally generated and compensated for power supply and temperature variation. The THRESHOLD pin is provided to adjust the threshold via an external resistor tied to V_{CC}.



(A) Receiver Used in Differential Mode



(B) Receiver Used in Single–Ended Mode

Figure 4–1. Receiver Amplifier With Carrier Detect

SECTION 5 – CLOCK RECOVERY

5.1 OVERVIEW

The clock recovery circuitry is a key part of the receive function providing RX clock, a 2 times (2X) RX clock, and a 4 times (4X) RX clock for data recovery and to send receive symbols to the MAC. Figure 5–1 is a simplified functional schematic of the clock recovery logic. The clock recovery is fed by the output stage of the receive amplifier. The phase–coherent signal contains frequency components equal to 1X and 2X the serial data rate. Figure 5–2 shows an example of timing for a 5 Mb/s serial data rate. The RXOUT signal drives a one–shot with a time period of 75% of 1/2 bit time; this locks out edges caused by the higher frequency component. The one–shot is non–retriggerable and is triggered on both positive and negative going edges. This produces a pulse for every edge of the lower frequency.

The output of the one–shot is divided by 2 to produce a 50% duty cycle signal equal in frequency to the lower frequency of the phase–coherent signal. In turn, the ÷2 flip–flop output runs through a multiplexer to a phase–locked loop (PLL) system. The multiplexer selects the RXOUT signal when carrier detect is present; otherwise the local oscillator divided by 4 is selected.

The PLL system consists of a digital phase detector, an active loop filter, a voltage–controlled multivibrator (VCM), and a divide–by–4 feedback counter. When in phase lock, the output of the divide–by–4 feedback counter is locked to the reference clock. In turn, the VCM 4 times clock is also aligned with the reference clock as shown in Figure 5–2.

The 4 times clock from the VCM, the 2 times clock, and the 1 times clock are all in phase (when the PLL is phase–locked) with the reference clock, and are used to do data recovery. Note that the reference clock can be 180° out of phase with the bit time boundaries (Figure 5–2). This does not affect the 2X and 4X clocks which are used to sample the data. However, RXCLK can be out of sync with the bit time boundaries and special circuitry in the data recovery logic detects and corrects this condition.

When no valid input signal is available from the receive amplifier (carrier detect is not asserted), the multiplexer selects the local clock as a reference. This has the advantages of:

1. Supply a RXCLK when no data is present.
2. Holding the PLL in frequency lock so that only phase–lock must be achieved when switching to the RX signal.
3. Providing a smooth transition for RXCLK when moving from the local oscillator (at the beginning of a frame) and vice versa (at the end of a frame). The PLL acts as an integrator.

The IEEE 802.4 provides a PAD–IDLE or training signal at the beginning of any transmission. The PAD–IDLE for phase–coherent FSK is an alternating one and zero pattern, and the PLL is capable of being locked–in well within the 24 bit times (3 octets). The design goal is to be locked–in within 12–16 bit times. Data recovered during this lockup time at the

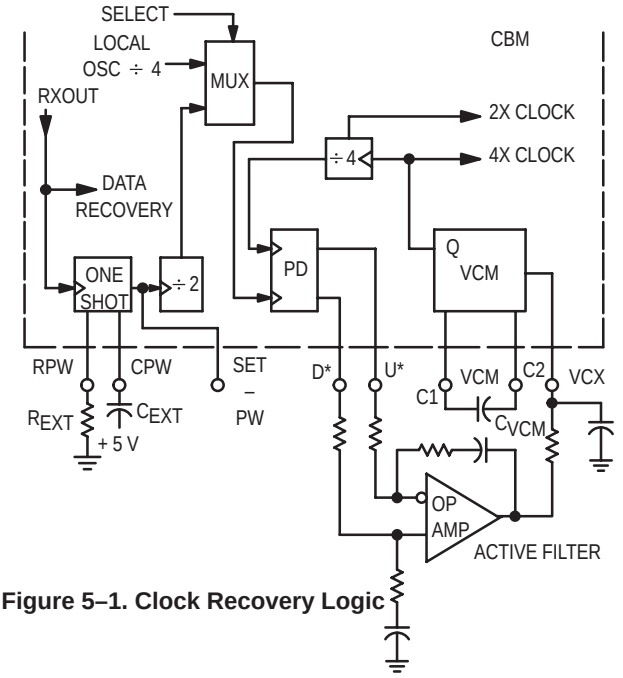
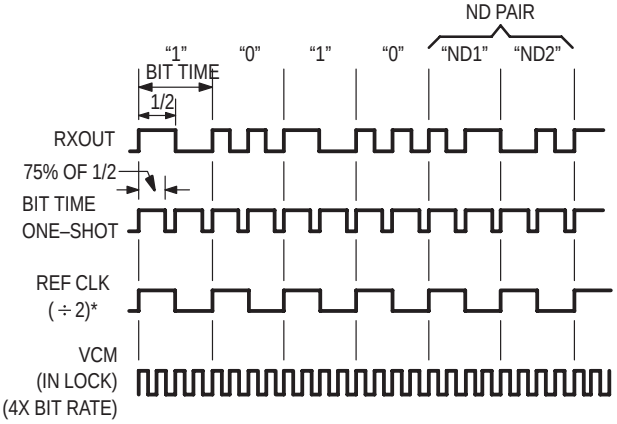


Figure 5–1. Clock Recovery Logic

beginning of a transmission can be invalid because the PLL clocks are not sync'ed. As a result the data recovery logic forces silence for 17–18 bit times after the carrier detect switches the reference clock (via the multiplexer) at the beginning of a received transmission.

5.2 ONE–SHOT

As previously stated, the one–shot is used to lock out the transitions due to the higher frequency component of the phase–coherent signal. The one–shot is non–retriggerable and fires off both edges of the incoming RXOUT signal. The time period should be set to 75% of half the bit time. As an example, the 5 Mb/s data rate has a 200 nsec bit time and the one–shot period then has a period of 75 nsec.



*NOTE: Ref clock can also be 180° out of phase with bit time.

Figure 5–2. Clock Recovery Timing Signals

Figure 5–3 shows the arrangement of the external timing capacitor and resistor. The internal resistor R_{INT} may be used with or without an external resistor. A test pin is also provided (SET–PW) to monitor the pulse width.

For 5 Mbps operation, typically R_{PW} = 1.5 kΩ and C_{PW} = 33 pF.

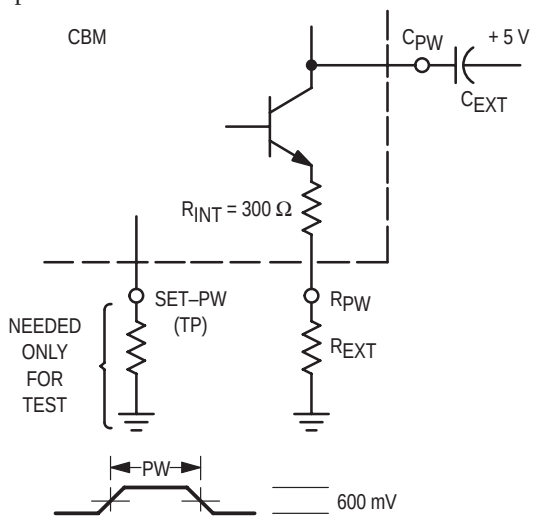
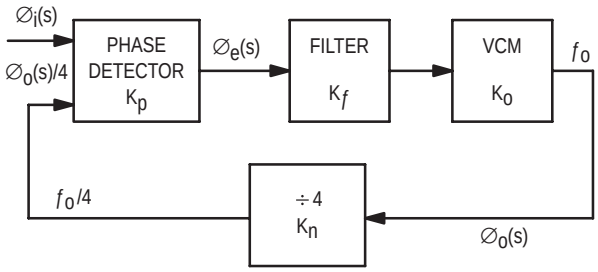


Figure 5–3. One–Shot Timing Components

5.3 PHASE–LOCKED LOOP (PLL) COMPONENTS

The PLL consists of a digital phase detector (PD), an active loop filter, a VCM, and a divide–by–4 feedback path. Figure 5–4 shows the fundamental elements of the PLL with their gain constants. The basic PLL allows the output frequency f_o to be "locked–on" to the input frequency f_i with a fixed phase relationship and to track it in frequency. When "in lock" the inputs to the phase detector have zero phase error. The input frequency is referenced to f_o/4.

A PLL follows classic servo theory and equations. In the following discussion a working knowledge of a PLL is assumed. For more background and applications information on PLL, the user is directed to Motorola Application Note AN535.



$\varnothing_e(s) = (1 / [1 + G(s) H(s)]) \varnothing_i(s)$

$\varnothing_o(s) = (G(s) / [G(s) H(s)]) \varnothing_i(s)$

where:

$G(s) = K_p K_f K_o$ $H(s) = Kn$ $Kn = 1 / N = 1/4$

Reference: App Note AN535

Figure 5–4. PLL Elements and Loop Equations

5.3.1 Phase Detector (PD)

The phase detector produces a voltage proportional to the phase difference between $\varnothing_i(s)$ and $\varnothing_o(s)/4$. This voltage after filtering is used as the control signal for the VCM. The PD has pump–up UP* and pump–down DOWN* outputs with a typical 800 mV logic swing. UP* produces a low level pulse equal in width to the amount of time the positive edge of $\varnothing_i$ (REF CLOCK) leads the positive edge of $\varnothing_o/4$ (VCM/4). DOWN* produces a low level pulse equal in width to the amount of time the positive edge of $\varnothing_i$ lags $\varnothing_o/4$. Both pulses will not occur on the same clock cycle as $\varnothing_o/4$ must either lead or lag $\varnothing_i$ when the PLL is out of lock. When in–lock, both outputs produce a very narrow pulse or negative spike.

The gain of the phase detector is equal to (reference app note AN532A):

K_p = (Logic swing)/2π = 800 mV/2π = 0.127 V/radian

5.3.2 Voltage Controlled Multivibrator (VCM)

The operating frequency range of the VCM is determined by the capacitor tied to pins VCM–C1 and VCM–C2. The capacitor should be selected to put the desired operating frequency in the center of the VCM tuning range.

The transfer function of the VCM is given by:

$$K_o = K_V/s$$

where K_V is the sensitivity in radians per second per volt. K_V is found by:

$$K_V = \frac{[(\text{Upper frequency limit}) - (\text{Lower frequency limit})]2\pi}{(\text{Control voltage tuning range})}$$

$$= 2\pi\,(\Delta f)/\Delta V_{CX} \text{ rad/s/V}$$

then

$$K_o = 2\pi\,(\Delta f)/(\Delta V_{CX})\text{s rad/s/V}$$

5.3.3 Loop Filter

Since a Type 2 system is required (phase coherent output, see reference AN535), the loop transfer function of Figure 5–4 takes the form:

$G(s)\,H(s) = [K\,(s+a)] / s^2$

Writing the loop transfer function (from Figure 5–4) and relating it to the above form:

$G(s)\,H(s) = [K_p K_V K_n K_f] / s = [K\,(s+a)] / s^2$

Having determined K_p, K_o, and that K_n = 1/4 then K_f (filter transfer function) must take the form:

$K_f = (s+a) / s$

An active filter of the form shown in Figure 5–5A gives the desired results, where:

K_f = (R2 C s+1) / R1 C s (for large A)

The active filter can also be implemented as shown in Figure 5–5B using an alternate approach of a charge pump. The advantage of the charge pump design is that it can be implemented using only a single 5.0 volt supply. Its transfer function is:

$K_f = (RC\,s + 1) / C\,s$

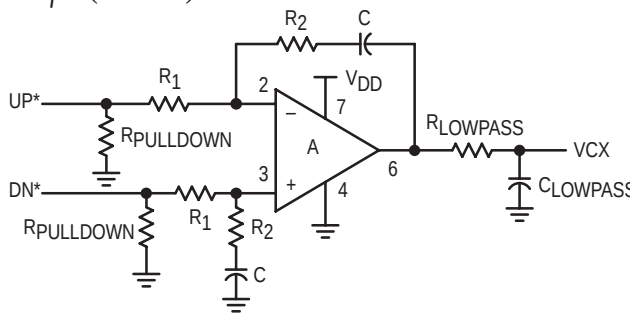


Figure 5–5A. Active Filter Using Op Amp

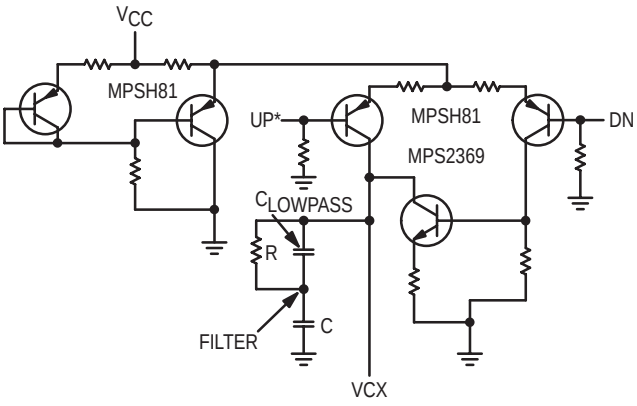


Figure 5–5B. Charge Pump/Filter

5.3.4 Loop Characteristics

If an active filter as shown with an op amp is used, the general PLL loop transfer function now becomes:

$$G(s)\,H(s) = K_p\,K_f\,K_o\,K_n$$
$$= K_p\,[(R2\,C\,s+1) / R1\,C\,s]\,(K_v/s)\,(1 / N)$$

Its characteristic equation is set to the form:

$$C.E. = 1 + G(s)\,H(s) = 0$$
$$= s^2 + (K_p\,K_v\,R2)\,s / (R1\,N) + K_p\,K_v) / (R1\,C\,N)$$

Relating to the standard form ($s^2 + 2\xi\omega_n s + \omega_n 2$) and solving:

$$\omega_n^2 = (K_p\,K_v) / R1\,C\,N \quad 2\xi\omega_n = (K_p\,K_v R2) / R1\,N$$

where

ω_n = Natural frequency
ξ = damping factor.

If a change pump loop filter is used, the general PLL loop transfer function alternately becomes:

$$G(s)\,H(s) = K_p\,K_f\,K_o\,K_n$$
$$= K_p[(R\,C\,s + 1) / C\,s]\,(K_v / s)\,(1 / N)$$

Its characteristics equation is set to the form:

$$C.E. = 1 + (Gs)\,(Hs) = 0$$
$$= s^2 + (K_p\,K_v\,R)\,s / (N) + (K_p\,K_v) / (C\,N)$$

Relating to the standard form ($s2 + 2\xi\omega_n s + \omega_n^2$) and solving:

$$\omega_n^2 = (K_p\,K_v) / C\,N \quad 2\xi\omega_n = (K_p\,K_v\,R) / N$$

SECTION 6 – DATA RECOVERY

6.1 OVERVIEW

The RXOUT signal from the receive amplifier and clocks generated by the clock recovery logic are used by the data recovery logic. The MC68194 recovers the data from the encoded receive signal by opening sampling windows around the 1/4 and 3/4 bit time positions and looking for edges in the received signal (refer to Figure 6–1 for the encoded data representations). A data ONE has transitions only at the 0 and 1/2 bit time positions. A data ZERO has transitions at the 0, 1/4, 1/2, and 3/4 bit time positions. A NON–DATA symbol has transitions at the 0, 1/4, and 1/2 bit time positions (ND1) or at the 0, 1/2, and 3/4 bit time positions (ND2). NON–DATA symbols should always occur in pairs; each pair is made up of one of each type of NON–DATA encoded symbols as shown in Figure 6–2 (ND1 followed by ND2).

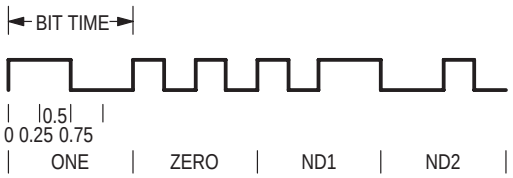


Figure 6–1. Encoded Data Representation

ONEs, ZEROs, and NON–DATA pairs can be easily decoded by keeping track of the 1/4 and 3/4 bit time position transitions. The ONEs, ZEROs, and NON–DATA pairs are then reported on the RXSYMX pins as described in the serial interface discussion. Two other conditions can also be reported while receiving in MAC mode — BAD SIGNAL and SILENCE. BAD SIGNAL is reported when a ND1 symbol is not followed immediately by a ND2 symbol or when a ND2 symbol is received and not immediately preceded by a ND1 symbol.

SILENCE is reported when one of four conditions occurs:

1. When the amplitude of the received signal is not large enough to trigger the on–chip carrier detect circuit. Reporting SILENCE when the carrier detect signal is not asserted prevents the chip from responding to low level noise.
2. When in internal loopback mode and SILENCE is being requested on the TXSYMX pins, SILENCE will be reported on the RXSYMX pins. An internal digital carrier detect is used during loopback and this signal is negated when SILENCE is requested on the request channel.
3. During the PLL training period at the beginning of a transmission. When an incoming signal first triggers the

carrier detect in the amplifier, the PLL must lock to the new reference clock (generated from the data stream). During the lockup time, recovered data may not be valid. The data recovery logic forces SILENCE for a fixed period of time (17–18 bit times).

4. During end–of–transmission blanking. See Section 6.2.

The PAD–IDLE at the beginning of a transmission is used as a training signal as described in the clock recovery section. After the PLL has achieved lock, the recovered clock at this point may be in phase or 180° out of phase with the bit time clock at the sending end. This creates a problem for RXCLK and the data recovery logic because symbols would be decoded as the wrong combination of 1/2 bit time transitions.

Logic in the data recovery circuitry corrects for this situation. If the clock is 180° out of phase, the PAD–IDLE sequence (ONE, ZERO, ONE, ZERO, ONE, ...) will be decoded as a sequence of NON–DATA symbols. Refer to Figure 6–2. In normal data reception, NON–DATA symbols occur only in pairs; there are never three or more in a row. Therefore, three or more NON–DATA symbols occurring in a row indicate that the bit time clock is 180° out of phase and the bit time clock (RXCLK) must be slipped as shown in Figure 6–3. The clock frequency and phase have now been recovered and symbol decode proceeds as described below.

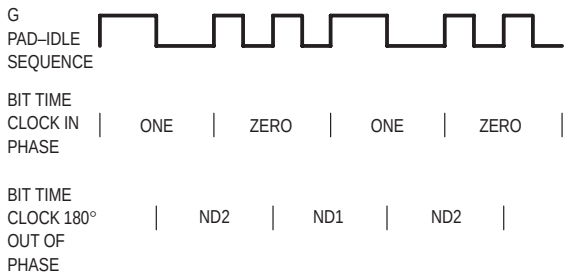


Figure 6.2 Training Sequence Decoded With In–Phase and Out–Of Phase Clocks

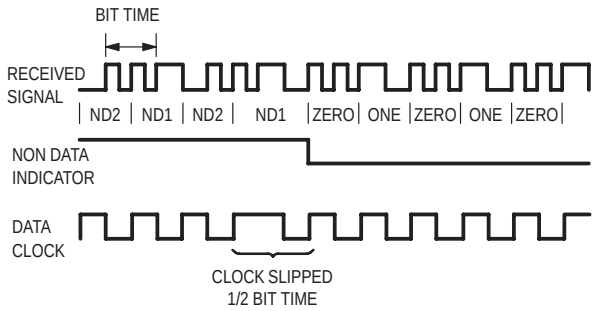


Figure 6–3. Clock Slip To Bring In Phase With Data Stream

6.2 RECEIVER END–OF–TRANSMISSION BLANKING

The IEEE 802.4 requires that the physical layer recognize the end of a transmission and report silence to the MAC for a period thereafter. This period of silence is referred to as blanking and must meet the following conditions:

1. Blanking must begin no later than 4 MAC–symbol times after the last MAC–symbol of the End Delimiter (i.e., the last End Delimiter of the transmission).
2. Blanking must continue to a point at least 24 MAC–symbol times but not more than 32 MAC–symbol times from the last MAC–symbol of the End Delimiter.

The MC68194 provides this function by recognizing the last End Delimiter of a transmission (I Bit = 0, see Section 1.3). The CBM reports silence for 32 symbols after the last symbol of the End Delimiter.

The blanking function can be disabled for test purposes or non–IEEE 802.4 applications via the EOTDIS* input.

SECTION 7 – SERIAL INTERFACE

7.1 OVERVIEW

The serial interface is composed of the Physical Data Request Channel and the Physical Data Indication Channel. The serial interface is used to pass commands and data frames to and from the CBM.

7.2 PHYSICAL DATA REQUEST CHANNEL

Five signals comprise the physical data request channel. Three of these signals (TXSYM2, TXSYM1 and TXSYM0) are multiplexed and have different meanings depending on the mode of SMREQ*. When SMREQ* is equal to one, the MAC mode is selected. When SMREQ* is equal to zero, the physical layer management mode is selected.

7.2.1 TXCLK — Transmit Clock

The transmit clock can be from 1.0 to 10 MHz. TXSYM2, TXSYM1, TXSYM0 and SMREQ* are synchronized to TXCLK. The IEEE 802.4 standard for carrier band allows for 5.0 or 10 MHz clocks.

7.2.2 SMREQ* — Station Management Request

SMREQ* directs the physical layer to be in MAC or physical layer management mode. In MAC mode SMREQ* = 1 and in management mode SMREQ* = 0.

7.2.3 TXSYM0, TXSYM1, and TXSYM2 — Transmit Symbols

In physical layer management mode TXSYM2, TXSYM1 and TXSYM0 have the meanings shown in Figure 7–1.

State	TXSYM2	TXSYM1	TXSYM0
RESET	1	1	1
DISABLE LOOPBACK	1	0	1
ENABLE TRANSMITTER	0	1	1
SERIAL SM DATA/IDLE	0	0	0/1

Figure 7–1. Request Channel Encoding for Physical Management Mode (SMREQ* = 0)

The CBM supports only four station management commands (RESET, LOOPBACK DISABLE, ENABLE TRANSMITTER and IDLE) encoded on lines TXSYM2, TXSYM1 and TXSYM0. The CBM does not support the SMDATA commands, but responds with a **"NACK"**. In MAC mode, the encoding for TXSYM2, TXSYM1, and TXSYM0 are shown in Figure 7–2.

Symbol	TXSYM2	TXSYM1	TXSYM0
ZERO	0	0	0
ONE	0	0	1
NON–DATA	1	0	X
PAD–IDLE	0	1	X
SILENCE	1	1	X

Where:

ZERO is binary zero.
ONE is binary one.
NON–DATA is a delimiter flag and is always present in pairs.
PAD–IDLE is one symbol of preamble/interframe idle.
SILENCE is silence or no signal.

Figure 7–2. Request Channel Encoding For MAC Mode (SMREQ* = 1)

7.3 PHYSICAL DATA INDICATION CHANNEL

Five signals comprise the physical data indication channel. Three of these signals (RXSYM2, RXSYM1 and RXSYM0) are multiplexed and have different meanings depending on the state of SMIND*. When SMIND* is equal to one, the physical layer is in MAC mode and when SMIND* is equal to zero, the physical layer is in management mode or an error has occurred.

7.3.1 RCXLK — Receive Clock

The receive clock can be from 1.0 to 10 MHz. RXSYM2, RXSYM1, RXSYM0, and SMIND* are synchronized to RXCLK. The IEEE 802.4 standard for carrier band networks allows 5.0 or 10 MHz clocks.

7.3.2 SMIND* — Station Management Indication

SMIND* indicates whether the physical layer is in MAC mode (SMIND* = 1) or management mode (SMIND* = 0) of operation. When in MAC mode of operation, the physical layer has RXSYM2, RXSYM1, and RXSYM0 encoded indicating data reception. When in management mode of operation, the physical layer RXSYM2, RXSYM1 and RXSYM0 are encoded to confirm response to received commands or to indicate a physical error (jabber inhibit).

7.3.3 RXSYM0, RXSYM1 and RXSYM2 — Receive Symbols

The encoding for RXSYM2, RXSYM1, and RXSYM0 in physical management mode is shown in Figure 7–3:

State	RXSYM2	RXSYM1	RXSYM0
NACK (non–acknowledgement)	1	0	*
ACK (acknowledgement)	0	1	*
IDLE	0	0	1
Physical Layer Error	1	1	1

*Indicates RXSYM0 contains the SM RX data when responding to a serial data command.

Figure 7–3. Indication Channel Encoding For Physical Management Mode (SMIND* = 0)

The encoding of RXSYM2, RXSYM1, and RXSYM0 in MAC mode is shown in Figure 7–4.

Symbol	RXSYM2	RXSYM1	RXSYM0
ZERO	0	0	0
ONE	0	0	1
NON–DATA	1	0	X
SILENCE	1	1	X
BAD SIGNAL	0	1	X

Where:

ZERO is the received data zero.
ONE is the received data one.
NON–DATA is a delimiter flag and is always present in pairs.
SILENCE is silence or no signal.
BAD SIGNAL is received bad signal.
X = Don't care.

Figure 7–4. Indication Channel Encoding For MAC Mode (SMIND* = 1)

SECTION 8
PHYSICAL MANAGEMENT

8.1 OVERVIEW

The MC68194 supports four physical management commands on the request channel: RESET, DISABLE LOOPBACK, ENABLE TRANSMITTER, and IDLE. The serial data station management commands are not implemented in the MC68194. These unimplemented commands are typically used to set up and read registers or control bits within a more complex modem. The CBM does not have registers and does not require the SMDATA commands. Upon reception of a SMDATA command, the CBM will respond with a NONACKNOWLEDGEMENT (NACK) and a response byte in accordance with the IEEE DTE–DCE Interface Standard. The data in the response byte is all ZEROs. Receipt of a RESET, DISABLE LOOPBACK, or ENABLE TRANSMITTER command will abort the SMDATA response.

8.2 RESET

The RESET command performs the same function as the RESET pin; the internal loopback mode is enabled, the transmitter outputs are disabled and TXDIS is enabled, and the jabber inhibit timeout is cleared. In addition the RESET command will generate an ACKNOWLEDGEMENT response (ACK) on the RXSYMx pins.

The RESET pin is an asynchronous function. When taken high it resets the CBM as described above leaving the CBM ready to respond to the physical data request channel.

NOTE: For the MC68194 to respond properly to commands after a hardware reset, the request channel must either be in MAC mode upon exiting the hardware reset or the request channel must go to MAC mode briefly before going to management mode. If the MC68194 is in management mode upon exiting the hardware reset, it remains reset and does not recognize the command because it is waiting for a MAC mode to management mode transition. This situation can be corrected by either exiting hardware reset with the request channel in MAC mode or putting the request channel in MAC mode briefly before issuing any management commands. See Section 8.6 for command response timing.

8.3 INTERNAL LOOPBACK

The internal loopback mode is provided for testing the CBM. In this mode a multiplexer selects the internal transmitter signal to drive the clock recovery and data recovery portions of the receive circuitry. This transmit signal is taken just prior to the output buffer stages of the transmitter circuit.

The loopback mode can only be selected via RESET (management command or external pin). Loopback mode is exited upon receipt of the management command DISABLE LOOPBACK. The CBM will respond with ACK to this command.

A normal sequence of events to test the CBM then would be:

1. Initialize the CBM via a RESET command or hardware reset.
2. Return to MAC mode and send test data. The CBM is full duplex.
3. In management mode, send DISABLE LOOPBACK command to exit loopback.

Following the test the modem can be setup for standard operation.

8.4 STANDARD OPERATION

Standard operation requires that the transmitter be enabled as well as disabling loopback. The transmitter is automatically disabled on RESET. Three things must happen after a RESET before transmissions can begin:

1. Loopback mode must be exited with the DISABLE LOOPBACK command. The MC68194 responds to this command with the ACK management response.
2. The transmitter must be activated with the ENABLE TRANSMITTER command. The MC68194 responds to this command with the ACK management response.
3. The MC68194 must exit the management mode and enter the MAC data mode.

The CBM is now ready to send and receive data, i.e., the CBM is in MAC or data mode, loopback is disabled, and the transmitter is enabled.

8.5 IDLE

The CBM provides the IDLE response when an IDLE management command is received. In addition, the IDLE response is returned for all invalid, as opposed to unimple–mented (SMDATA) commands.

8.6 COMMAND RESPONSE TIMING

The MC68194's management command/response operation is:

1. ACK response to RESET, DISABLE LOOPBACK, and ENABLE TRANSMITTER within 2 clock periods. As shown in Figure 8–1, the precise response time depends on the relative phase of the TXCLK and the RXCLK signals. If they are in phase, the response will be available at the RXSYMx pins 1.5 clocks after the command is latched. If the clocks are 180° out of phase, the delay will be 2 clocks. The command should be held on the TXSYMX pins until the response is received on the RXSYMX pins.
2. The IDLE command and all invalid commands will produce the IDLE response with the same delay as described above.
3. The SMDATA command response timing is shown in Figure 8–2. The NACK response to the SMDATA command is available on the RXSYMX pins in 2.5 or 3

clock periods depending on the relative phases of the TXCLK and RXCLK signals. When NACK becomes valid, RXSYM0 is low creating a start bit for the response byte. NACK is held for 9 clock periods with RXSYM0 low (start bit plus 8 ZERO data bits). NACK is held for one additional clock with RXSYM0 high. This is the stop bit and mark the end of the SMDATA response byte. 12.5 or 13 clock periods after receiving the SMDATA command the NACK response is removed.

In management mode, RXCLK is always locked to TXCLK. These clocks may be in phase or 180° out of phase as discussed above. This uncertainty exists because the clock recovery PLL can lock to either phase of the local clock. The response delays relative to TXCLK may therefore differ by 1/2 clock period. The MC68194 must leave management mode, enter MAC mode, and return to management mode for a phase change to occur. The relative phase of the two clocks will not change while in management mode.

Because the clock recovery PLL requires a training period when first entering management mode, the PLL must have sufficient time to lock to the new clock source (TXCLK) before being required to provide a response. To provide enough time for the PLL to lock up, the MC68194 delays 16.5 to 17 clock periods before entering station management mode (SMIND* = 0) after the station management mode is selected (SMREQ* = 0). Refer to Figure 8–3 for the timing diagram. During this delay, the MAC mode SILENCE response will be present on the RXSYMX pins.

Users must be aware that when first requesting management mode there will be this added delay before the mode is entered and a response is available. If a management command is sent along with the station management mode request (SMREQ* = 0) and held on the TXSYMX pins until the CBM enters station management mode, the proper response will be available on the RXSYMX pins immediately except in the case of SMDATA commands. SMDATA commands must not be requested on the TXSYMX pins until after SMIND* indicates that station management mode has been entered.

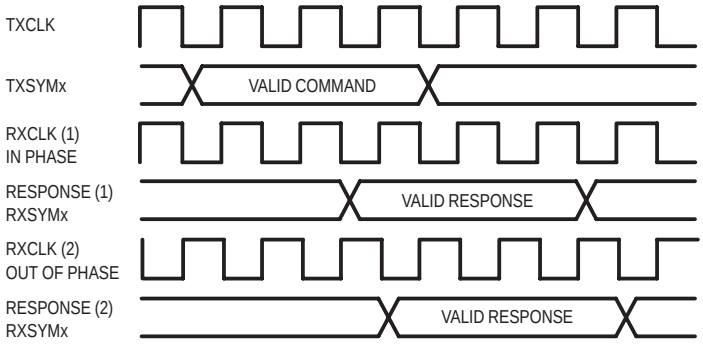


Figure 8–1. Parallel Command Response Time

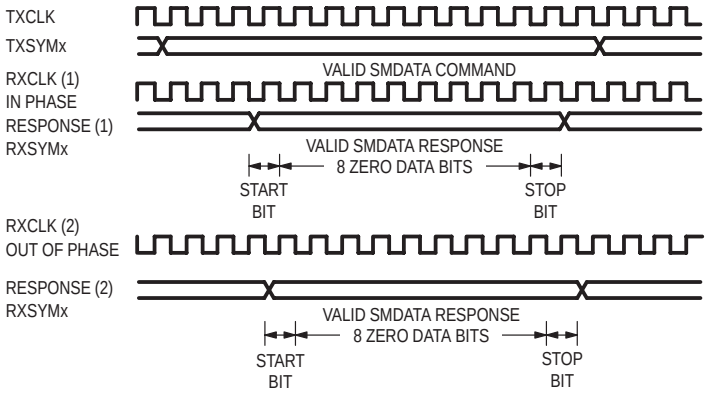


Figure 8–2. SMDATA Command Response Time

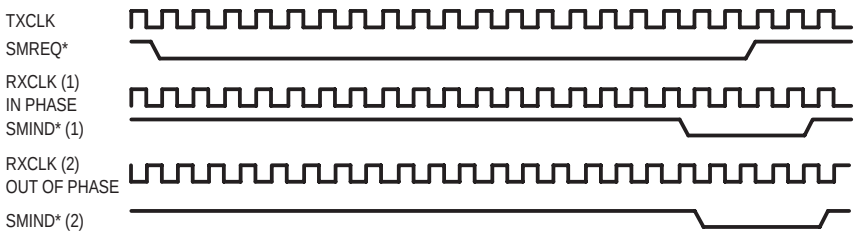


Figure 8–3. Station Management Request Response Time

SECTION 9
MC68194 CARRIER BAND MODEM
ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS (Limits Beyond Which Device Life May Be Impaired)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	0 to +7.0	Vdc
TTL Input Voltage	V_{IN}	0 to +5.5	Vdc
TTL Output Voltage (Applied to output HIGH)	V_{OUT}	0 to +5.5	Vdc
ECL Output Source Current	I_{out}	50	mAdc
Storage Temperature Cerquad	T_{stg}	–55 to +165	°C
Junction Temperature Cerquad	T_J	165	°C

GUARANTEED OPERATING RANGES

Characteristic	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Operating Temperature (Cerquad in still air)	T_A	0	25	70	°C

DC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
TTL INPUTS (TXSYM0–TXSYM2, SMREQ*, RESET, EOTDIS)† (T_A = 0–70°C, V_{CC} = 5.0 Vdc ±5%)						
Input HIGH Voltage	V_{IH}	2.0			Vdc	
Input LOW Voltage	V_{IL}			0.8	Vdc	
Input HIGH Current	I_{IH}			20	μA	V_{CC} = MAX, V_{IN} = 2.7 Vdc
Input LOW Current	I_{IL}			–0.7	mA	V_{CC} = MAX, V_{IN} = 0.4 Vdc
†All TTL inputs include a 15 k–ohm pullup resistor to V_{CC}.						
TTL OUTPUTS (TXCLK, RXSYM0–RXSYM2, SMIND*, RXCLK, JAB) (T_A = 0–70°C, V_{CC} = 5.0 Vdc ±5%)						
Output HIGH Voltage	V_{OH}	2.7			Vdc	V_{CC} = MIN, I_{OH} = MAX
Output LOW Voltage	V_{OL}			0.5	Vdc	V_{CC} = MIN, I_{OL} = MAX
Output HIGH Current	I_{OH}			–0.4	mA	
Output LOW Current	I_{OL}			8.0	mA	
ECL OUTPUTS (TXOUT, TXOUT*) (T_A = 25°C, V_{CC} = 5.0 Vdc)						
Output HIGH Voltage	V_{OH}		4.10		Vdc	$R_{pulldown}$ = 220 Ω
Output LOW Voltage	V_{OL}		3.28		Vdc	$R_{pulldown}$ = 220 Ω
OPEN COLLECTOR OUTPUT (TXDIS) (T_A = 25°C, V_{CC} = 5.0 Vdc)						
Output LOW Current	I_{OL}	450		550	μA	V_{OL} = 3.0 Vdc
Output HIGH Leakage Current	I_{OH}			50	μA	V_{OH} = 5.0 Vdc
RECEIVER (SINGLE–ENDED OPERATION)						
GAIN Output Voltage HIGH	G_{VOH}		4.2		Vdc	I_{OH} = 5.0 mA
GAIN Output Voltage LOW	G_{VOL}		3.6		Vdc	I_{OL} = 5.0 mA
Input Signal (for limiting)	RV_{IN}		+17		dBmV	GAIN output = 600 mV
Detected Threshold	V_{thres}		+18		dBmV	R_{THRES} = 120 kΩ to V_{CC}
PHASE DETECTOR OUTPUTS (UP*, DOWN*)						
Phase Detector Output Voltage HIGH	PD_{VOH}		4.0		Vdc	I_{OH} = 10 mA
Phase Detector Output Voltage LOW	PD_{VOL}		3.3		Vdc	I_{OL} = 10 mA

DC ELECTRICAL CHARACTERISTICS (cont.)– OTHER PARAMETERS – (T_A = 25°C, V_{CC} = 5.0 Vdc)

POWER SUPPLY DRAIN CURRENT

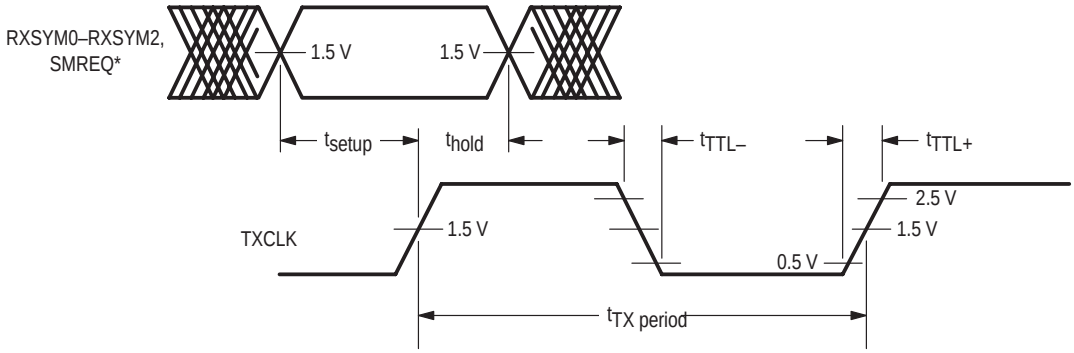
Characteristic	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Power Supply Drain Current	I_{CC}		220	270	mA	No outputs loaded, TTL inputs open.
VCM						
VCM Oscillator	F_{osc1}		40		MHz	C_{vcm} = 24 pF, RXCLK = 5.0 MHz, VCX = 3.6 Vdc
Frequency	F_{osc2}		20		MHz	C_{vcm} = 68 pF, RXCLK = 10 MHz, VCX = 3.6 Vdc
VCM Tuning Ratio	TR		4.0			
VCX Tuning Range	V_{CX} V_{CX}	2.6		4.6	Vdc	
ONE–SHOT						
SET–PW Output Voltage HIGH	PW_{VOH}		4.2		Vdc	I_{OH} = 5.0 mA
SET–PW Output Voltage LOW	PW_{VOL}		3.6		Vdc	I_{OL} = 5.0 mA
Timing Current	IT		0.8	4.0	mA	
Internal Resistor	R_{int}		300		Ohms	
Timing Reference Voltage (measured at RPW pin)	V_{ref}	1.2	1.3	1.4	Vdc	IT = 0.8 mA
External Timing Resistor	R_{EXT}		1.5		kΩ	For 5.0 Mb/s data rate.
External Timing Capacitor	C_{EXT}		33		pF	For 5.0 Mb/s data rate.
JABBER TIMER						
RC Threshold High	JAB_{VIH}		4.25		Vdc	I_{IN} = 5.0 μA Max
RC Output V_{OL}	JAB_{VOL}		0.4		Vdc	I_{OL} = 10 mA
Jabber Resistor	R_{JAB}		120	125	kΩ	For 0.5 sec timing
Jabber Capacitor	C_{JAB}		2.2		μF	For 0.5 sec timing
CRYSTAL OSCILLATOR						
Input HIGH Voltage	V_{IH}	3.0			Vdc	XTAL1 & XTAL2 tied together
Input LOW Voltage	V_{IL}			2.0	Vdc	XTAL1 & XTAL2 tied together

AC ELECTRICAL CHARACTERISTICS††

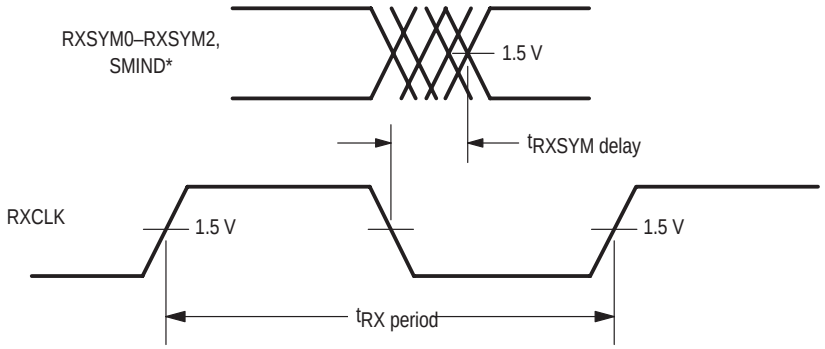
(T_A = 0–70°C, V_{CC} = 5.0 Vdc ±5%)

Characteristic	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
TXCLK Period	$t_{TXperiod}$	180	200	220		@ 5.0 MHz, Figure 9–1A.
RXCLK Period	$t_{RXperiod}$	180	200	220		@ 5.0 MHz, PLL locked to TXCLK, Figure 9–1B.
TTL Rise/Fall Time	$t_{TTL\pm}$		4.0		ns	Figure 9–1A.
TXSYMX, SMREQ* Setup Time (to TXCLK)	t_{setup}		15	25	ns	Figure 9–1A.
TXSYMX, SMREQ* Hold Time (to TXCLK)	t_{hold}		–9.0	0	ns	Figure 9–1A.
RXSYMX, SMIND* Delay Time (to RXCLK)	$t_{RXSYM\ delay}$	0	2.5	5.0	ns	Figure 9–1B.
XTAL1,2 to TXCLK Delay	$t_{TXCLK\ delay}$		18		ns	Figure 9–1C. XTAL1 and XTAL2 tied together and driven with external source.
TXOUT, TXOUT* Rise/Fall Time	$t_{TXOUT\pm}$		1.5		ns	$R_{pulldown}$ = 500 Ω
UP*, DOWN* Rise/Fall Time	$t_{PD\pm}$		1.5		ns	$R_{pulldown}$ = 500 Ω
TXDIS Rise/Fall Time	$t_{TXDIS\pm}$		35		ns	2.0 kΩ pullup to V_{CC}. **Do not use Figure 9–2 test load.**

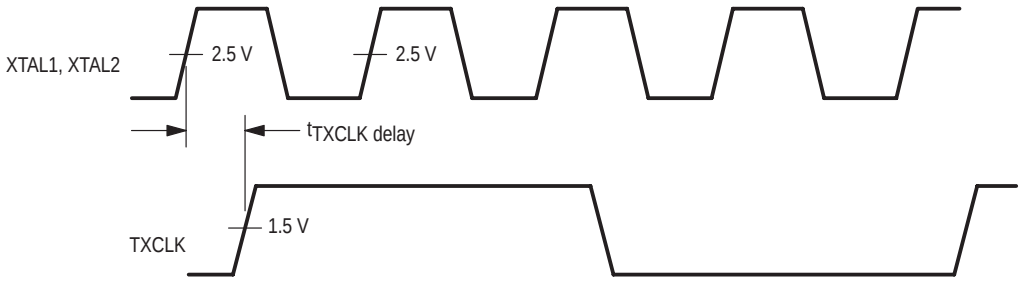
†† See Figure 9–2 for AC test load.



(A) TXSYMX, SMREQ* Setup and Hold Timing to TXCLK



(B) RXSYMX, SMIND* Delay Timing to RXCLK



(C) TXCLK Delay Timing to XTAL1, XTAL2

Figure 9–1. AC Test Waveforms

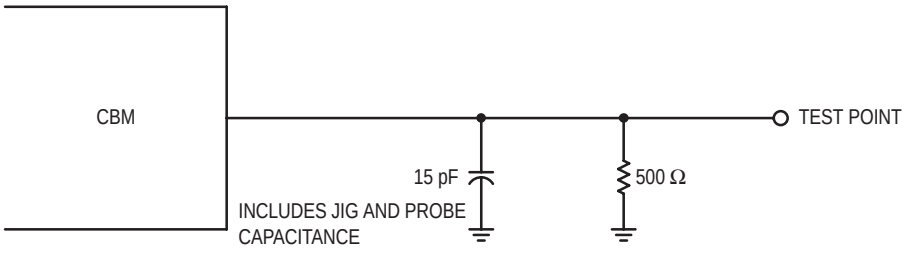


Figure 9–2. TTL, TXOUT, TXOUT*, Up* & Down* AC Test Load

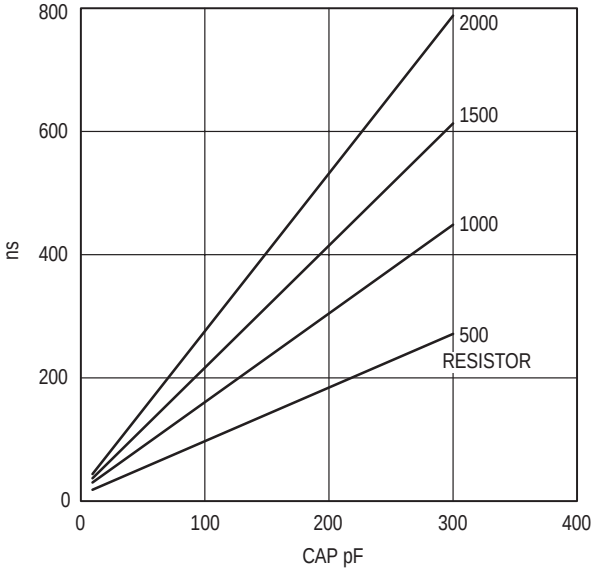


Figure 9–3. One Shot Pulse Width versus Rext/Cext

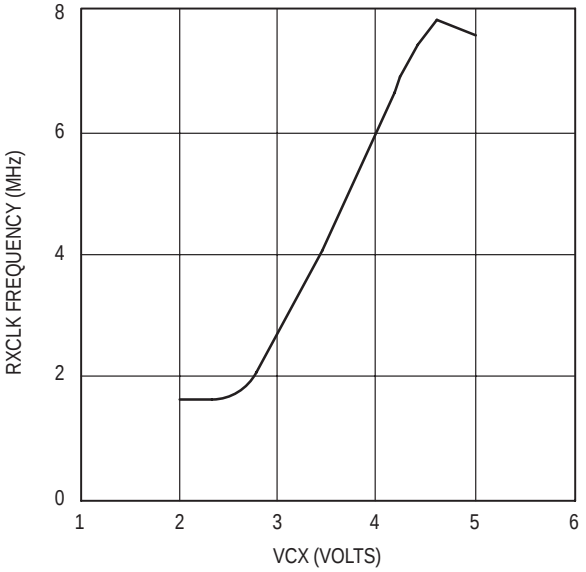


Figure 9–4. VCM Frequency versus Control Voltage (V_{CC} = 5.0 Vdc & C = 68 pF)

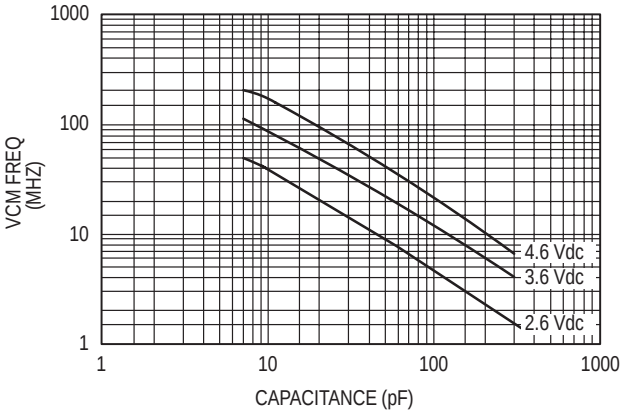


Figure 9–5. VCM Frequency versus Capacitance

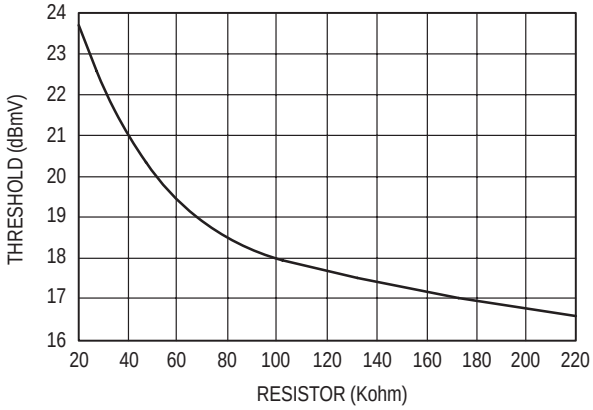


Figure 9–6. Detected Threshold versus Threshold Resistor

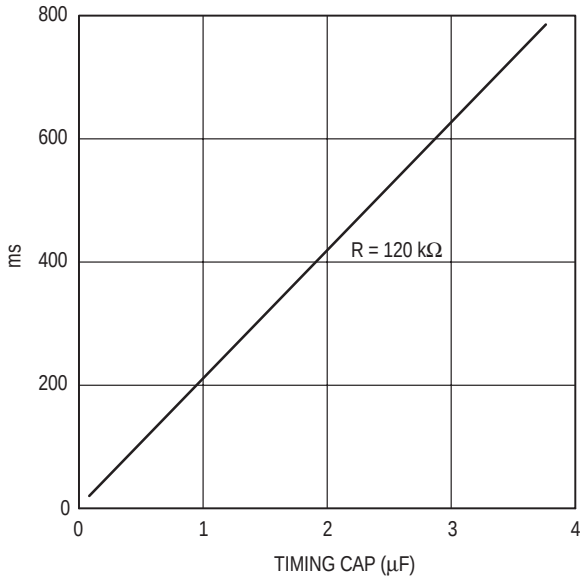
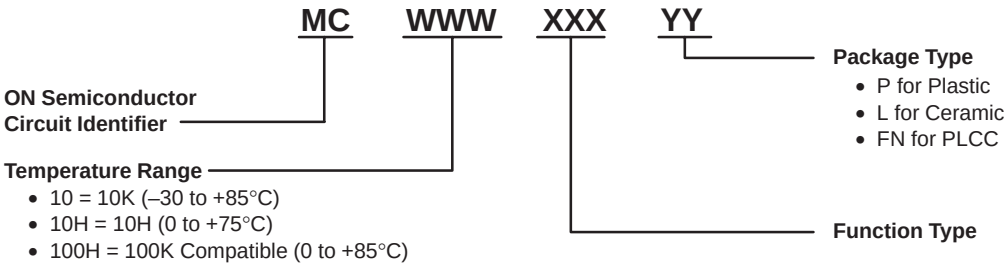


Figure 9–7. Jabber Time Constant versus Capacitance

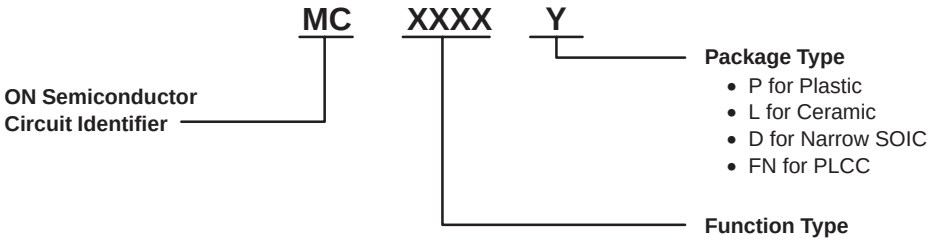
CHAPTER 5
Ordering Information

MECL Family
Device Nomenclatures

MECL 10K, MECL 10H/100H



MECL III

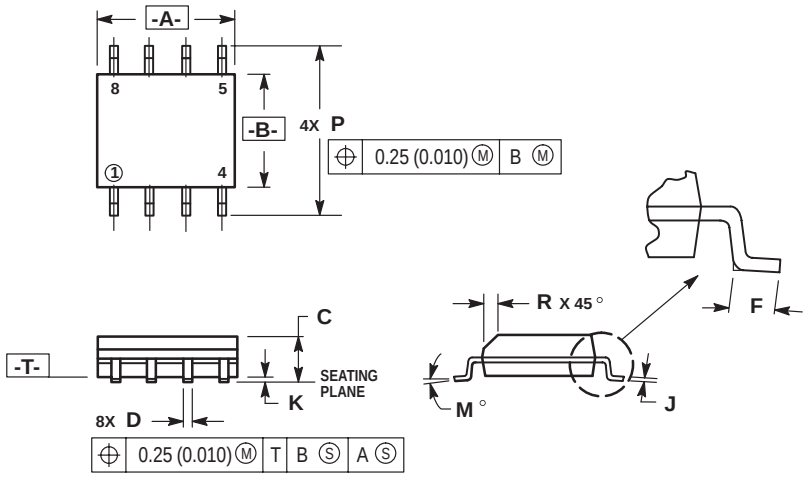


Case Outlines

A letter suffix to the MECL logic function part number is used to specify the package style (see drawings below). See appropriate selector guide for specific packaging available for a given device type.

8-Pin Package

SO–8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-05
ISSUE M

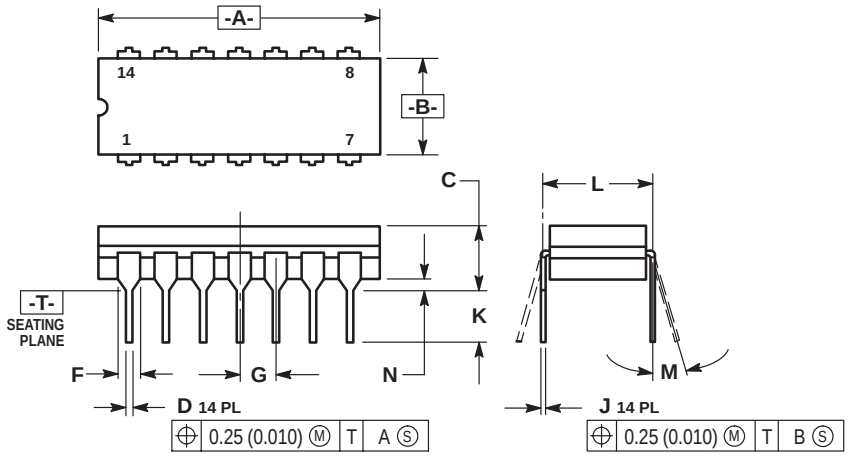


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

14-Pin Packages

CDIP–14
L SUFFIX
CERAMIC PACKAGE
CASE 632–08
ISSUE Y

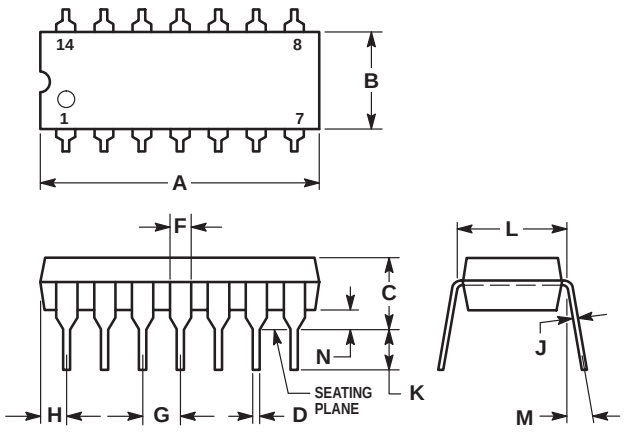


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMESNION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.94
B	0.245	0.280	6.23	7.11
C	0.155	0.200	3.94	5.08
D	0.015	0.020	0.39	0.50
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

14-Pin Packages (continued)

PDIP–14
P SUFFIX
PLASTIC PACKAGE
CASE 646–06
ISSUE L

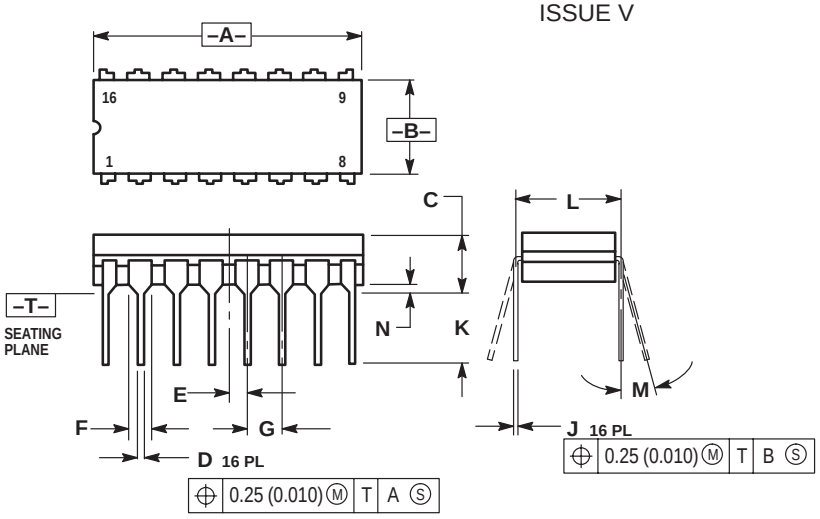


NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

16-Pin Packages

CDIP–16
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V

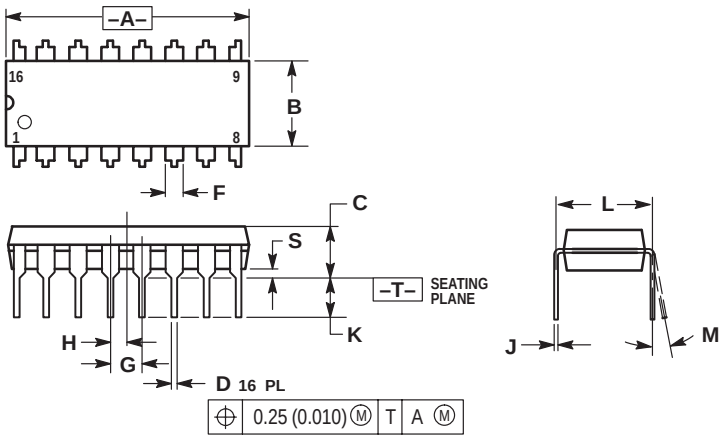


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

16-Pin Packages (continued)

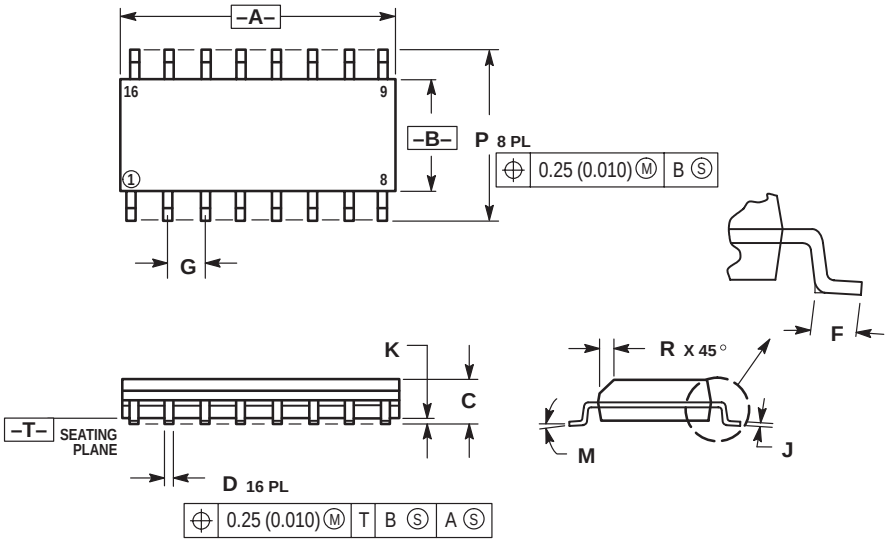
PDIP–16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

SO–16
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J

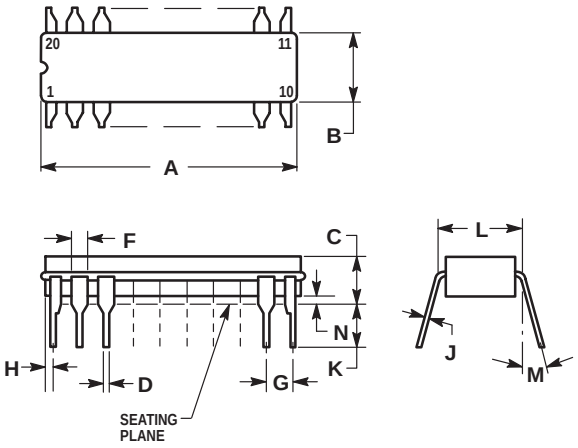


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

20-Pin Packages

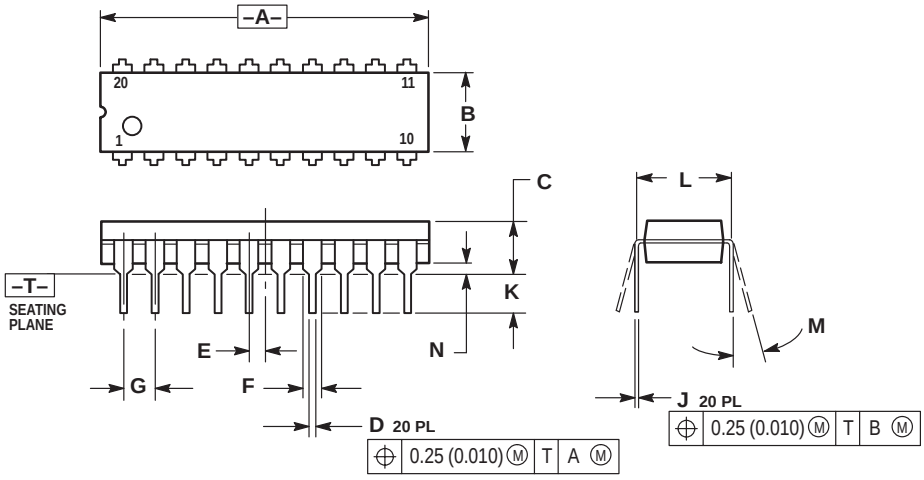
CDIP–20
L SUFFIX
CERAMIC DIP PACKAGE
CASE 732–03
ISSUE E



NOTES:
1. LEADS WITHIN 0.010 DIAMETER, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS A AND B INCLUDE MENISCUS.

	INCHES	
DIM	MIN	MAX
A	0.940	0.990
B	0.260	0.295
C	0.150	0.200
D	0.015	0.022
F	0.055	0.065
G	0.100 BSC	
H	0.020	0.050
J	0.008	0.012
K	0.125	0.160
L	0.300 BSC	
M	0°	15°
N	0.010	0.040

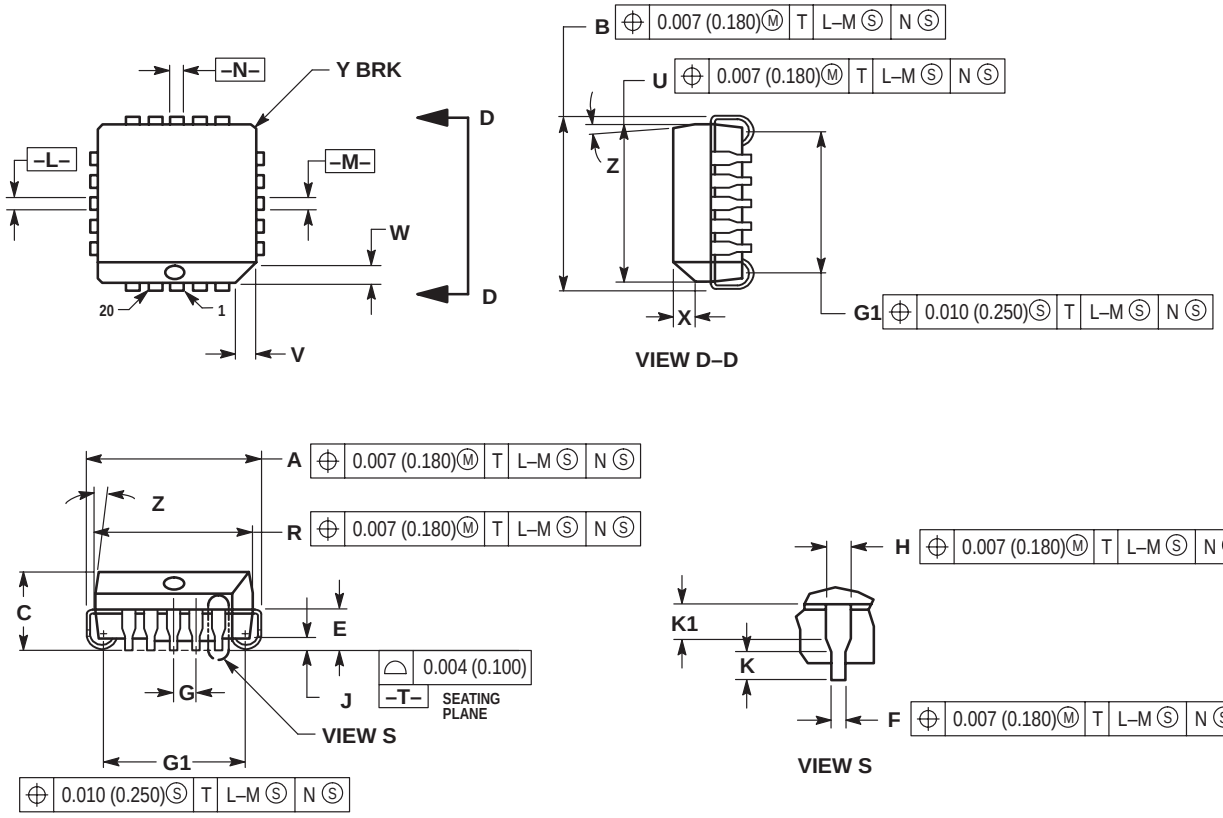
PDIP–20
P SUFFIX
PLASTIC DIP PACKAGE
CASE 738–03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

PLCC–20
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775–02
ISSUE C

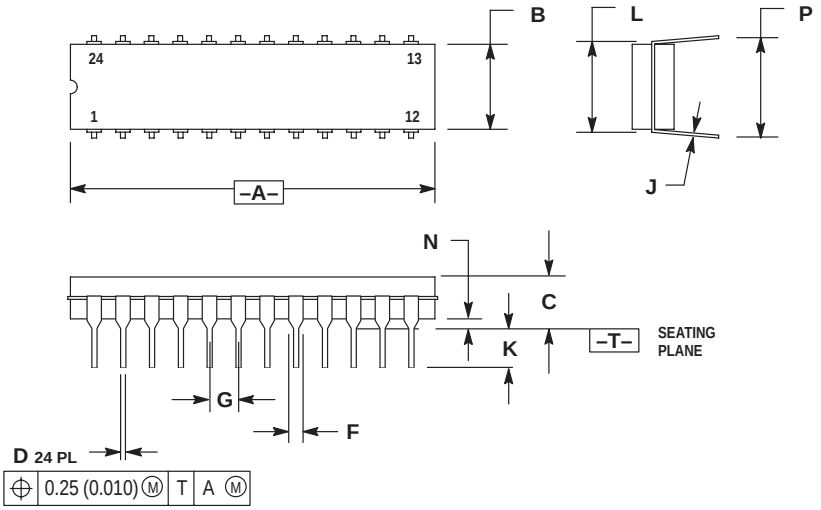


NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

24-Pin Packages

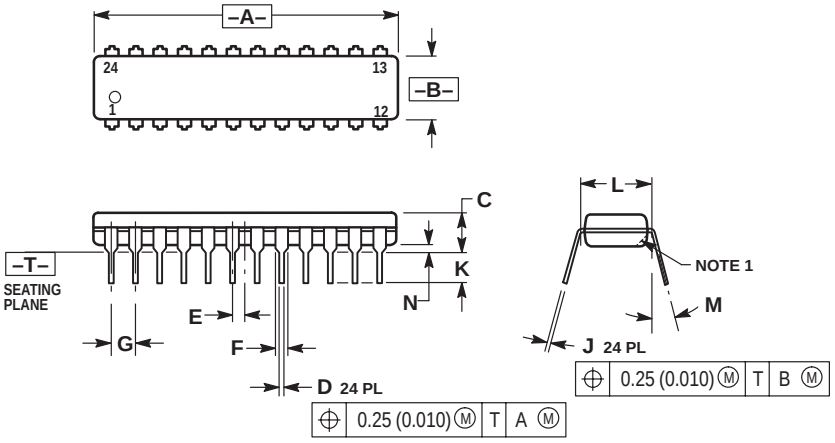
CDIP–24
L SUFFIX
CERAMIC DIP PACKAGE
CASE 758–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.240	1.285	31.50	32.64
B	0.285	0.305	7.24	7.75
C	0.160	0.200	4.07	5.08
D	0.015	0.021	0.38	0.53
F	0.045	0.062	1.14	1.57
G	0.100 BSC		2.54 BSC	
J	0.008	0.013	0.20	0.33
K	0.100	0.165	2.54	4.19
L	0.300	0.310	7.62	7.87
N	0.020	0.050	0.51	1.27
P	0.360	0.400	9.14	10.16

PDIP–24
P SUFFIX
PLASTIC DIP PACKAGE
CASE 724–03
ISSUE D

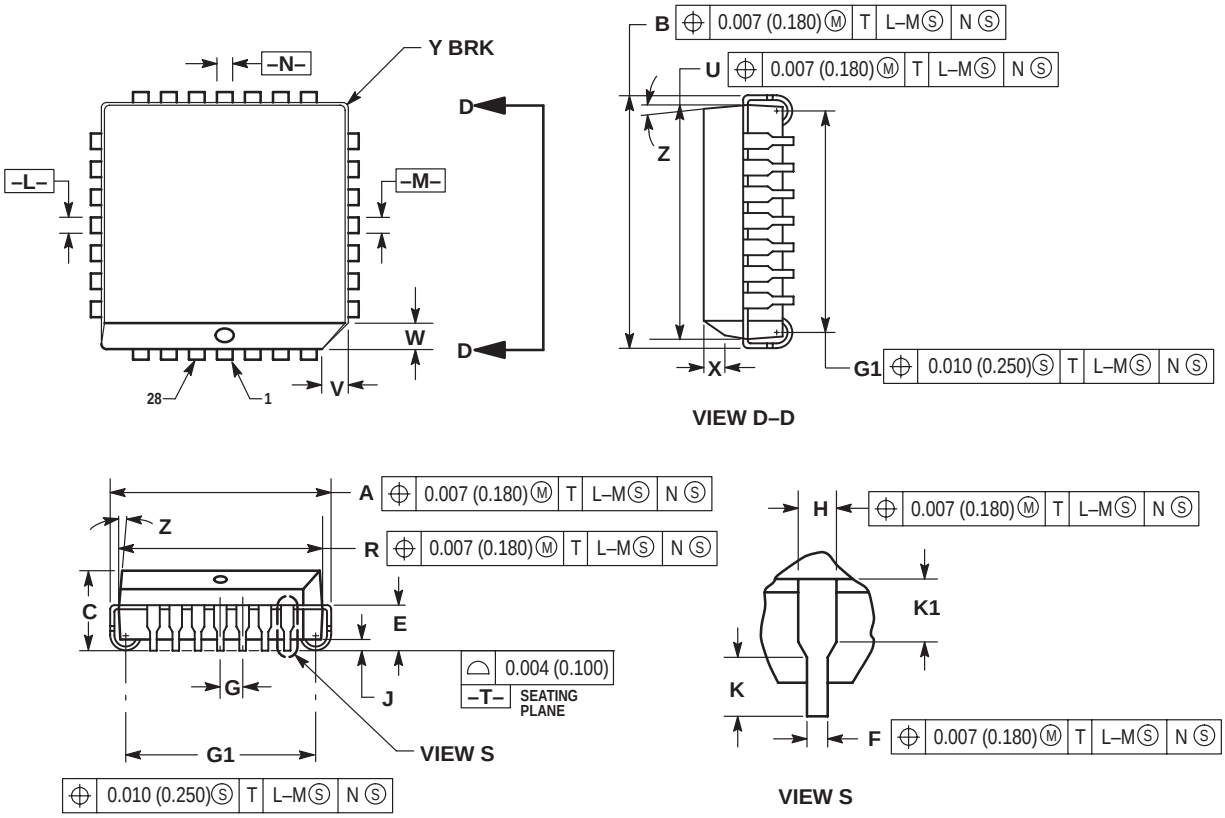


NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

28-Pin Package

PLCC–28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE D

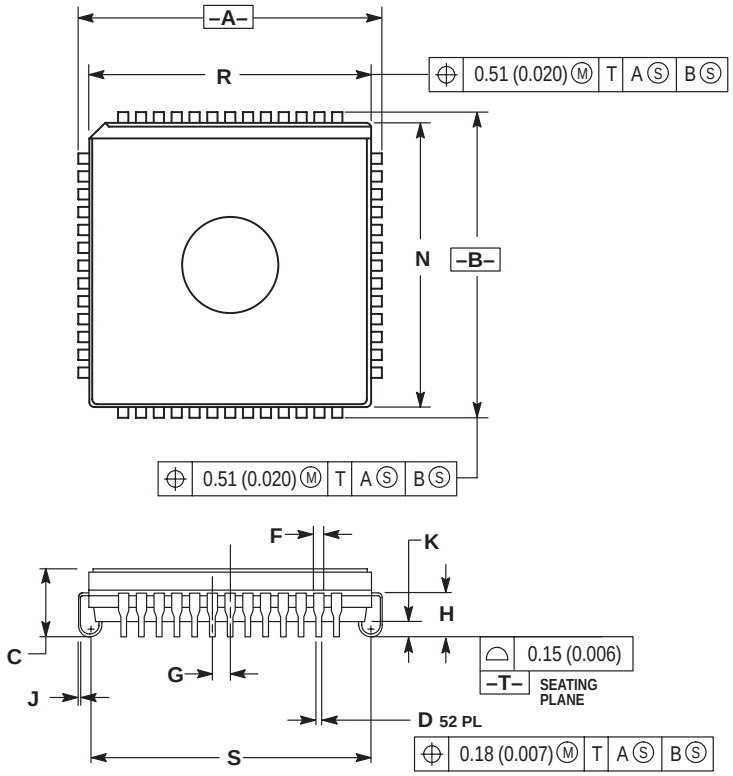


NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2 °	10 °	2 °	10 °
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

52-Pin Package

FJ SUFFIX
J–LEAD CERQUAD PACKAGE
CASE 778B–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION R AND N DO NOT INCLUDE GLASS PROTRUSION. GLASS PROTRUSION TO BE 0.25 (0.010) MAXIMUM.
4. ALL DIMENSIONS AND TOLERANCES INCLUDE LEAD TRIM OFFSET AND LEAD FINISH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.785	0.795	19.94	20.19
B	0.785	0.795	19.94	20.19
C	0.165	0.200	4.20	5.08
D	0.017	0.021	0.44	0.53
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
H	0.090	0.130	2.29	3.30
J	0.006	0.010	0.16	0.25
K	0.035	0.045	0.89	1.14
N	0.735	0.756	18.67	19.20
R	0.735	0.756	18.67	19.20
S	0.690	0.730	17.53	18.54

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A User's Guide contains procedural, task–oriented instructions for using or running a device or product. A User's Guide differs from a Reference Manual in the following respects:

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* Volume of information is typically less than for Reference Manuals
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